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Oki, Network Solutions for a Global Society

PEUL86410-02

Preliminary

ML86410 User's Manual

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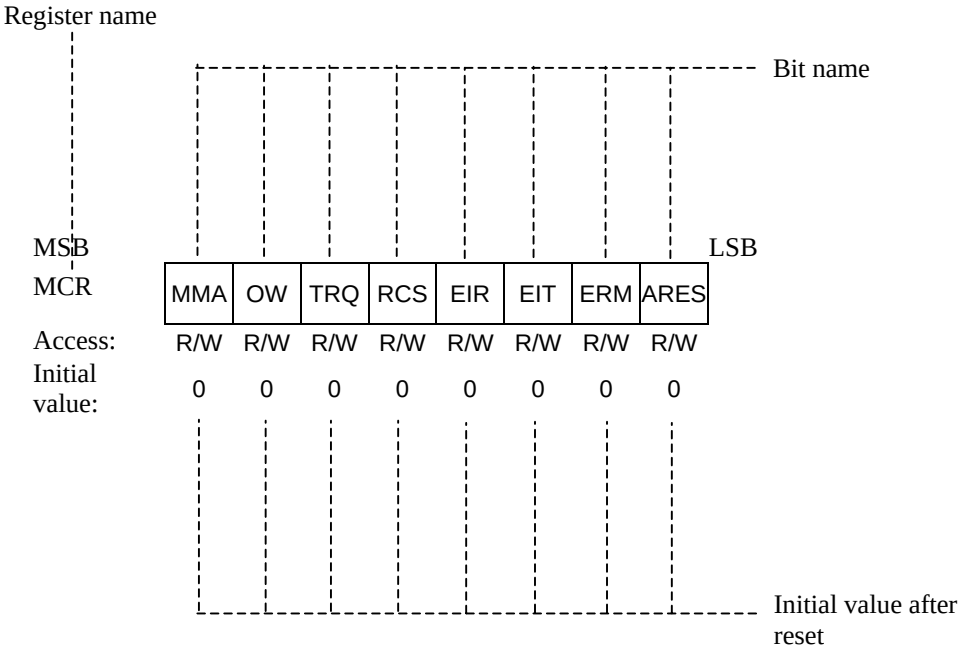
Preface

This manual describes the operation of the ML86410.

Notation

Classification	Notation	Description
♦ Numeric value	0xnn	Indicates a hexadecimal number.
♦ Address	00xnnnn_nnnn	Indicates a hexadecimal number (indicates 0xnnnnnnnn).
♦ Unit	word, WORD	1 word = 32 bits
	byte, BYTE	1 byte = 8 bits
	maga-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, µ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1"	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0"	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description
Read/write attribute: R indicates a readable bit and W indicates a writable bit.
MSB: Most significant bit of an 8-bit register (memory)
LSB: Least significant bit of an 8-bit register (memory)



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1. Overview

The ML86410 is an LSI that encodes YUV (YCbCr) format digital video signals into MPEG-4-ASP format ones in real time.
The LSI achieves high picture quality by a unique high-speed high-quality motion search method and a unique coding rate control method. For video input, the LSI supports progressive video output from camera modules and interlaced video output from NTSC/PAL digital video decoders.

1.1 Features

- Image encoding:
  - Encoding format
    - · MPEG-4 Simple Profile@Level 3
    - · MPEG-4 Advanced Simple Profile@Level 5
  - Supported image
    - · Progressive QVGA, 30 fps
    - · Progressive VGA, 30 fps
    - · Interlaced NTSC, 29.97 fps
    - · Interlaced PAL, 25 fps
  - Output frame (with a frame skipping function)
    - · QVGA/ VGA : 30/15/1/0.5 fps
    - · NTSC : 29.97/14.985/0.999/0.4995 fps
    - · PAL : 25/12.5/1/0.5 fps
  - Coding type
    - · IIII
    - · IPPP
  - Encoding mode
    - · CBR (Up to 6 Mbps)
    - · VBR
  - Supports interlaced images (NTSC/PAL)
  - Unique high-speed high-quality motion search method
  - Unique coding rate control method
  - 4MV motion estimation
  - Detectes abnormality such as:
    - · Camera input abnormality
    - · Stream data readout abnormality
    - · Set bit rate exceeded
  - Can suspend/restart encoding

- Video interface:
  - QVGA (320 × 240 pixels) / VGA (640 × 480 pixels) : YCbCr (8-bit (YCbCr) (4:2:2)) + sync, 27 MHz
    YUV (8-bit (YUV)(4:2:2)) + sync, 27 MHz
  - NTSC (720 × 480 pixels)) / PAL (720 × 576 pixels) : ITU-R BT.656, 27 MHz

Note:
Although signals are input in 4:2:2 format, they are converted to 4:2:0 format before encoding processing.
Can choose the order in which fields are loaded during interlacing (Top first/Bottom first)
Can choose between the positive polarity and the negative polarity of CLKCAM when loading YUVDATA, VSYNC, or HSYNC
Clipping can be specified as no clipping or clipping in the range of 16≤Y,U,V≤240
For the interface, a 3.3 V I/O interface is used.

- Host CPU interface:
  - General-purpose 8-/16-bit data bus (can be connected directly with Oki's ARM microcontroller series)
  - Operable as an I/O device in DMA mode from the host CPU

- External SDRAM interface:
  - 32-bit data bus, 2 MWords × 32 bits, 81 MHz (equivalent to PC133)
  - Automatic initialization sequence
  - Column address: 8/9/10 bits selectable

- Input clock:
  - System clock : 27 MHz
  - Video interface : 27 MHz

- Power management
  - No power management function is provided

- Power supply voltage:
  - Core section : 1.35 to 1.65 V
  - I/O section : 3.0 to 3.6 V
  - PLL section : 1.35 to 1.65 V

- Operating frequency:
  - Internal : 81 MHz
  - Video interface section : 27 MHz

- Operating temperature (ambient temperature):
  - -20 to +85°C

- Package:
  - 144-pin plastic LQFP (LQFP144-P-2020-0.50-ZK)

1.2 Block Diagram

Figure 1-1 shows the block diagram of the ML86410.

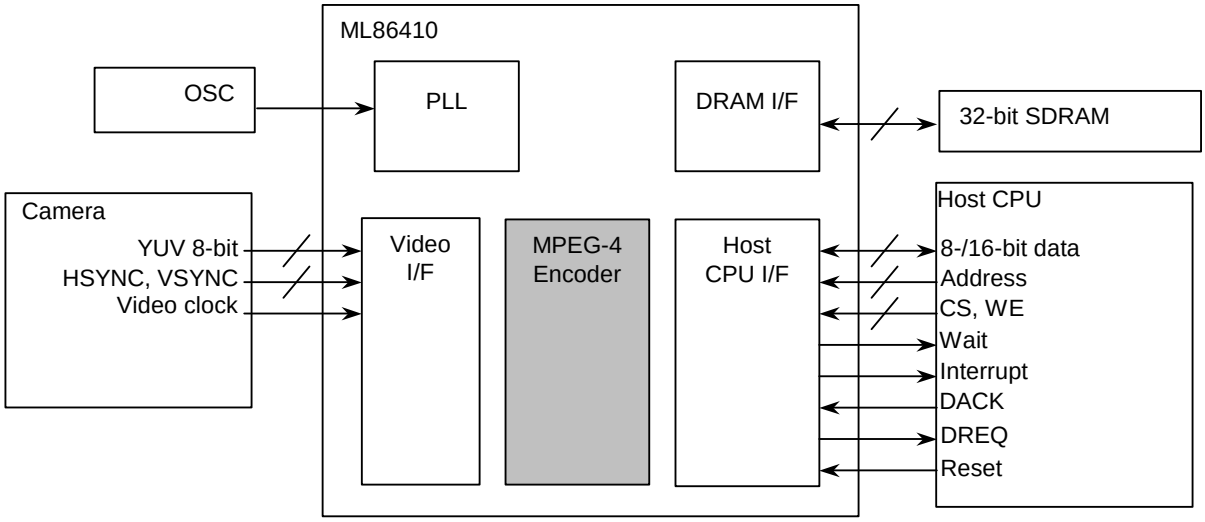


Figure 1-1 Block Diagram

1.3 Pins

1.3.1 Pin Configuration

Figure 1-2 shows the pin configuration of the 144-pin LQFP.

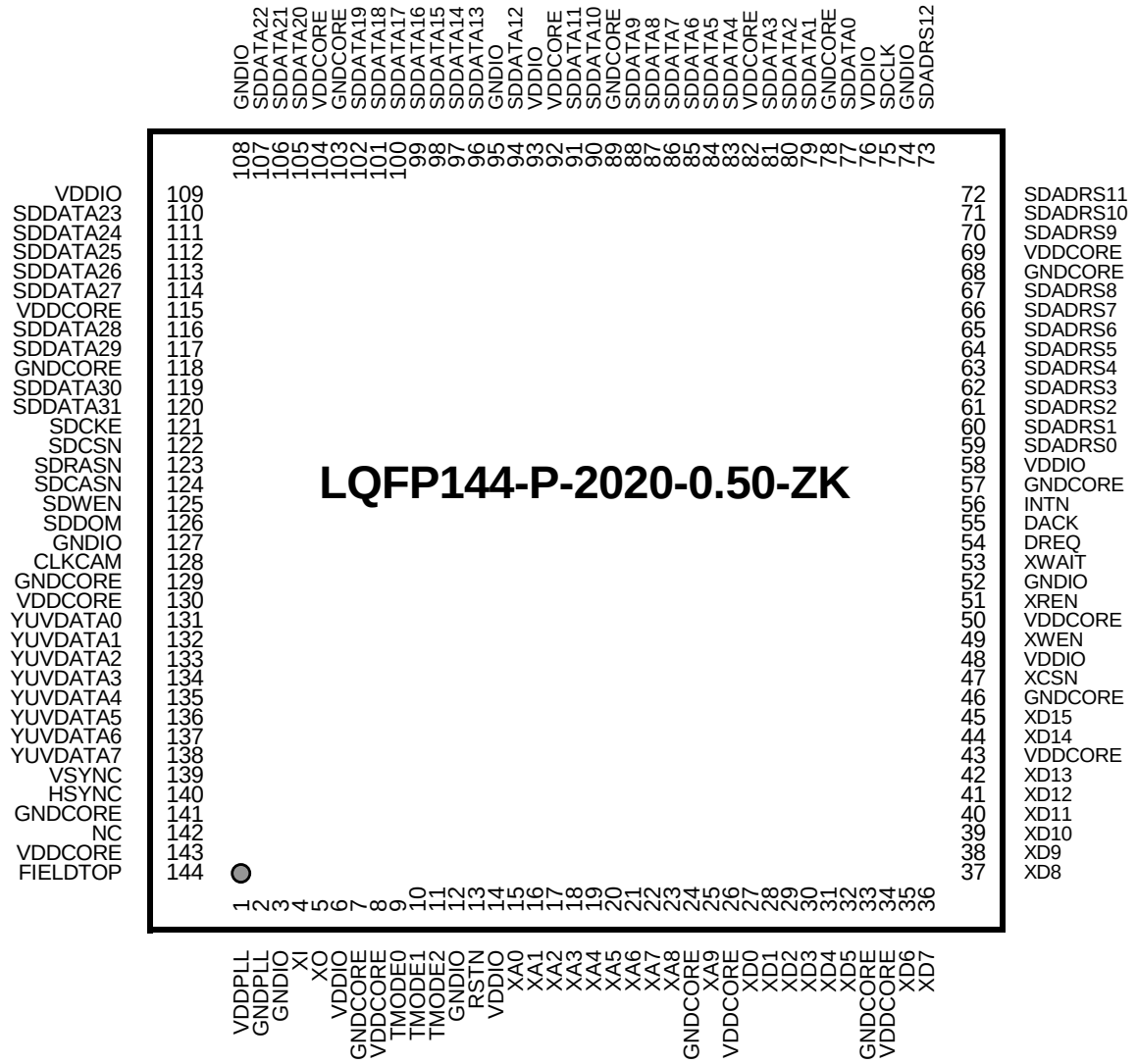


Figure 1-2 144-Pin LQFP Pin Configuration

1.3.2 List of Pins

Pin No.	Symbol	I/O	Description
1	VDDPLL	VDD	PLL power supply
2	GNDPLL	GND	PLL GND
3	GNDIO	GND	I/O GND
4	XI	—	Input clock (27 MHz)
5	XO	—	Input clock (27 MHz)
6	VDDIO	VDD	I/O power supply
7	GNDCORE	GND	Core GND
8	VDDCORE	VDD	Core power supply
9	TMODE0	I	Test mode 0
10	TMODE1	I	Test mode 1
11	TMODE2	I	Test mode 2
12	GNDIO	GND	I/O GND
13	RSTN	I	Reset
14	VDDIO	VDD	I/O power supply
15	XA0	I	External bus address input signal 0
16	XA1	I	External bus address input signal 1
17	XA2	I	External bus address input signal 2
18	XA3	I	External bus address input signal 3
19	XA4	I	External bus address input signal 4
20	XA5	I	External bus address input signal 5
21	XA6	I	External bus address input signal 6
22	XA7	I	External bus address input signal 7
23	XA8	I	External bus address input signal 8
24	GNDCORE	GND	Core GND
25	XA9	I	External bus address input signal 9
26	VDDCORE	VDD	Core power supply
27	XD0	I/O	External bus input/output data 0
28	XD1	I/O	External bus input/output data 1
29	XD2	I/O	External bus input/output data 2
30	XD3	I/O	External bus input/output data 3
31	XD4	I/O	External bus input/output data 4
32	XD5	I/O	External bus input/output data 5
33	GNDCORE	GND	Core GND
34	VDDCORE	VDD	Core power supply
35	XD6	I/O	External bus input/output data 6
36	XD7	I/O	External bus input/output data 7
37	XD8	I/O	External bus input/output data 8
38	XD9	I/O	External bus input/output data 9
39	XD10	I/O	External bus input/output data 10
40	XD11	I/O	External bus input/output data 11
41	XD12	I/O	External bus input/output data 12
42	XD13	I/O	External bus input/output data 13
43	VDDCORE	VDD	Core power supply
44	XD14	I/O	External bus input/output data 14
45	XD15	I/O	External bus input/output data 15
46	GNDCORE	GND	Core GND
47	XCSN	I	Chip enable signal
48	VDDIO	VDD	I/O power supply
49	XWEN	I	Write enable signal
50	VDDCORE	VDD	Core power supply

Pin No.	Symbol	I/O	Description
51	XREN	I	Read enable signal
52	GNDIO	GND	I/O GND
53	XWAIT	O	Wait signal
54	DREQ	O	DMA request
55	DACK	I	DMA acknowledge
56	INTN	O	Interrupt signal output
57	GNDCORE	GND	Core GND
58	VDDIO	VDD	I/O power supply
59	SDADRS0	O	SDRAM address 0
60	SDADRS1	O	SDRAM address 1
61	SDADRS2	O	SDRAM address 2
62	SDADRS3	O	SDRAM address 3
63	SDADRS4	O	SDRAM address 4
64	SDADRS5	O	SDRAM address 5
65	SDADRS6	O	SDRAM address 6
66	SDADRS7	O	SDRAM address 7
67	SDADRS8	O	SDRAM address 8
68	GNDCORE	GND	Core GND
69	VDDCORE	VDD	Core power supply
70	SDADRS9	O	SDRAM address 9
71	SDADRS10	O	SDRAM address 10
72	SDADRS11	O	SDRAM address 11
73	SDADRS12	O	SDRAM address 12
74	GNDIO	GND	I/O GND
75	SDCLK	O	SDRAM clock
76	VDDIO	VDD	I/O power supply
77	SDDATA0	I/O	SDRAM data 0
78	GNDCORE	GND	Core GND
79	SDDATA1	I/O	SDRAM data 1
80	SDDATA2	I/O	SDRAM data 2
81	SDDATA3	I/O	SDRAM data 3
82	VDDCORE	VDD	Core power supply
83	SDDATA4	I/O	SDRAM data 4
84	SDDATA5	I/O	SDRAM data 5
85	SDDATA6	I/O	SDRAM data 6
86	SDDATA7	I/O	SDRAM data 7
87	SDDATA8	I/O	SDRAM data 8
88	SDDATA9	I/O	SDRAM data 9
89	GNDCORE	GND	Core GND
90	SDDATA10	I/O	SDRAM data 10
91	SDDATA11	I/O	SDRAM data 11
92	VDDCORE	VDD	Core power supply
93	VDDIO	VDD	I/O power supply
94	SDDATA12	I/O	SDRAM data 12
95	GNDIO	GND	I/O GND
96	SDDATA13	I/O	SDRAM data 13
97	SDDATA14	I/O	SDRAM data 14
98	SDDATA15	I/O	SDRAM data 15
99	SDDATA16	I/O	SDRAM data 16
100	SDDATA17	I/O	SDRAM data 17
101	SDDATA18	I/O	SDRAM data 18
102	SDDATA19	I/O	SDRAM data 19

Pin No.	Symbol	I/O	Description
103	GNDCORE	GND	Core GND
104	VDDCORE	VDD	Core power supply
105	SDDATA20	I/O	SDRAM data 20
106	SDDATA21	I/O	SDRAM data 21
107	SDDATA22	I/O	SDRAM data 22
108	GNDIO	GND	I/O GND
109	VDDIO	VDD	I/O power supply
110	SDDATA23	I/O	SDRAM data 23
111	SDDATA24	I/O	SDRAM data 24
112	SDDATA25	I/O	SDRAM data 25
113	SDDATA26	I/O	SDRAM data 26
114	SDDATA27	I/O	SDRAM data 27
115	VDDCORE	VDD	Core power supply
116	SDDATA28	I/O	SDRAM data 28
117	SDDATA29	I/O	SDRAM data 29
118	GNDCORE	GND	Core GND
119	SDDATA30	I/O	SDRAM data 30
120	SDDATA31	I/O	SDRAM data 31
121	SDCKE	O	SDRAM CKE pin control (Clock Enable)
122	SDCSN	O	SDRAM CS pin control (Chip Select)
123	SDRASN	O	SDRAM RAS pin control (Row Address Strobe)
124	SDCASN	O	SDRAM CAS pin control (Column Address Strobe)
125	SDWEN	O	SDRAM WE pin control (Write Enable)
126	SDDQM	O	SDRAM DQM pin control (DQ Mask)
127	GNDIO	GND	I/O GND
128	CLKCAM	I	Pixel clock
129	GNDCORE	GND	Core GND
130	VDDCORE	VDD	Core power supply
131	YUVDATA0	I	YUV data input 0
132	YUVDATA1	I	YUV data input 1
133	YUVDATA2	I	YUV data input 2
134	YUVDATA3	I	YUV data input 3
135	YUVDATA4	I	YUV data input 4
136	YUVDATA5	I	YUV data input 5
137	YUVDATA6	I	YUV data input 6
138	YUVDATA7	I	YUV data input 7
139	VSYNC	I	Vertical sync signal
140	HSYNC	I	Horizontal sync signal
141	GNDCORE	GND	Core GND
142	NC	I	Unused pin
143	VDDCORE	VDD	Core power supply
144	FIELDTOP	I	Field signal

1.3.3 Pin Description

Pin No.	Symbol	I/O	Description	At reset	Active level	Type of I/O	Drive performance
SDRAM interface (52 pins)							
75	SDCLK	out	SDRAM clock	Low	—		6 mA
59	SDADRS0	out	SDRAM address 0	Low	—		4 mA
60	SDADRS1	out	SDRAM address 1	Low	—		4 mA
61	SDADRS2	out	SDRAM address 2	Low	—		4 mA
62	SDADRS3	out	SDRAM address 3	Low	—		4 mA
63	SDADRS4	out	SDRAM address 4	Low	—		4 mA
64	SDADRS5	out	SDRAM address 5	Low	—		4 mA
65	SDADRS6	out	SDRAM address 6	Low	—		4 mA
66	SDADRS7	out	SDRAM address 7	Low	—		4 mA
67	SDADRS8	out	SDRAM address 8	Low	—		4 mA
70	SDADRS9	out	SDRAM address 9	Low	—		4 mA
71	SDADRS10	out	SDRAM address 10	Low	—		4 mA
72	SDADRS11	out	SDRAM address 11	Low	—		4 mA
73	SDADRS12	out	SDRAM address 12	Low	—		4 mA
77	SDDATA0	in/out	SDRAM data 0	Hi-Z	—	Pull-down	4 mA
79	SDDATA1	in/out	SDRAM data 1	Hi-Z	—	Pull-down	4 mA
80	SDDATA2	in/out	SDRAM data 2	Hi-Z	—	Pull-down	4 mA
81	SDDATA3	in/out	SDRAM data 3	Hi-Z	—	Pull-down	4 mA
83	SDDATA4	in/out	SDRAM data 4	Hi-Z	—	Pull-down	4 mA
84	SDDATA5	in/out	SDRAM data 5	Hi-Z	—	Pull-down	4 mA
85	SDDATA6	in/out	SDRAM data 6	Hi-Z	—	Pull-down	4 mA
86	SDDATA7	in/out	SDRAM data 7	Hi-Z	—	Pull-down	4 mA
87	SDDATA8	in/out	SDRAM data 8	Hi-Z	—	Pull-down	4 mA
88	SDDATA9	in/out	SDRAM data 9	Hi-Z	—	Pull-down	4 mA
90	SDDATA10	in/out	SDRAM data 10	Hi-Z	—	Pull-down	4 mA
91	SDDATA11	in/out	SDRAM data 11	Hi-Z	—	Pull-down	4 mA
94	SDDATA12	in/out	SDRAM data 12	Hi-Z	—	Pull-down	4 mA
96	SDDATA13	in/out	SDRAM data 13	Hi-Z	—	Pull-down	4 mA
97	SDDATA14	in/out	SDRAM data 14	Hi-Z	—	Pull-down	4 mA
98	SDDATA15	in/out	SDRAM data 15	Hi-Z	—	Pull-down	4 mA
99	SDDATA16	in/out	SDRAM data 16	Hi-Z	—	Pull-down	4 mA
100	SDDATA17	in/out	SDRAM data 17	Hi-Z	—	Pull-down	4 mA
101	SDDATA18	in/out	SDRAM data 18	Hi-Z	—	Pull-down	4 mA
102	SDDATA19	in/out	SDRAM data 19	Hi-Z	—	Pull-down	4 mA
105	SDDATA20	in/out	SDRAM data 20	Hi-Z	—	Pull-down	4 mA
106	SDDATA21	in/out	SDRAM data 21	Hi-Z	—	Pull-down	4 mA
107	SDDATA22	in/out	SDRAM data 22	Hi-Z	—	Pull-down	4 mA
110	SDDATA23	in/out	SDRAM data 23	Hi-Z	—	Pull-down	4 mA
111	SDDATA24	in/out	SDRAM data 24	Hi-Z	—	Pull-down	4 mA
112	SDDATA25	in/out	SDRAM data 25	Hi-Z	—	Pull-down	4 mA
113	SDDATA26	in/out	SDRAM data 26	Hi-Z	—	Pull-down	4 mA
114	SDDATA27	in/out	SDRAM data 27	Hi-Z	—	Pull-down	4 mA
116	SDDATA28	in/out	SDRAM data 28	Hi-Z	—	Pull-down	4 mA
117	SDDATA29	in/out	SDRAM data 29	Hi-Z	—	Pull-down	4 mA
119	SDDATA30	in/out	SDRAM data 30	Hi-Z	—	Pull-down	4 mA
120	SDDATA31	in/out	SDRAM data 31	Hi-Z	—	Pull-down	4 mA
121	SDCKE	out	SDRAM CKE pin control (Clock Enable)	High	High		4 mA

Pin No.	Symbol	I/O	Description	At reset	Active level	Type of I/O	Drive performance
122	SDCSN	out	SDRAM CS pin control (Chip Select)	High	Low		4 mA
123	SDRASN	out	SDRAM RAS pin control (Row Address Strobe)	High	Low		4 mA
124	SDCASN	out	SDRAM CAS pin control (Column Address Strobe)	High	Low		4 mA
125	SDWEN	out	SDRAM WE pin control (Write Enable)	High	Low		4 mA
126	SDDQM	out	SDRAM DQM pin control (DQ Mask)	High	High		4 mA
Video interface (12 pins)							
131	YUVDATA0	in	YUV data input 0	—	High		—
132	YUVDATA1	in	YUV data input 1	—	High		—
133	YUVDATA2	in	YUV data input 2	—	High		—
134	YUVDATA3	in	YUV data input 3	—	High		—
135	YUVDATA4	in	YUV data input 4	—	High		—
136	YUVDATA5	in	YUV data input 5	—	High		—
137	YUVDATA6	in	YUV data input 6	—	High		—
138	YUVDATA7	in	YUV data input 7	—	High		—
139	VSYNC	in	Vertical sync signal	—	High		—
140	HSYNC	in	Horizontal sync signal	—	High		—
144	FIELDTOP	in	Field signal by interlacing 0 : Bottom Field 1 : Top Field	—	High		—
128	CLKCAM	in	Pixel clock	—	High	Schmitt	—
Host CPU interface (33 pins)							
15	XA0	in	External bus address output signal 0	—	—		—
16	XA1	in	External bus address output signal 1	—	—		—
17	XA2	in	External bus address output signal 2	—	—		—
18	XA3	in	External bus address output signal 3	—	—		—
19	XA4	in	External bus address output signal 4	—	—		—
20	XA5	in	External bus address output signal 5	—	—		—
21	XA6	in	External bus address output signal 6	—	—		—
22	XA7	in	External bus address output signal 7	—	—		—
23	XA8	in	External bus address output signal 8	—	—		—
25	XA9	in	External bus address output signal 9	—	—		—
27	XD0	in/out	External bus input/output data 0	Hi-Z	—		4 mA
28	XD1	in/out	External bus input/output data 1	Hi-Z	—		4 mA
29	XD2	in/out	External bus input/output data 2	Hi-Z	—		4 mA
30	XD3	in/out	External bus input/output data 3	Hi-Z	—		4 mA
31	XD4	in/out	External bus input/output data 4	Hi-Z	—		4 mA
32	XD5	in/out	External bus input/output data 5	Hi-Z	—		4 mA

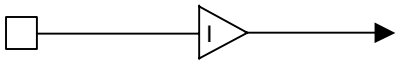
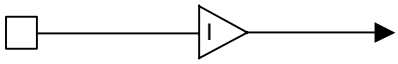
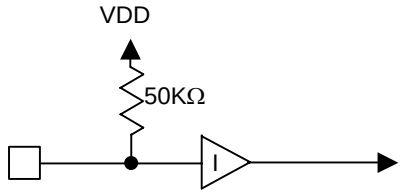
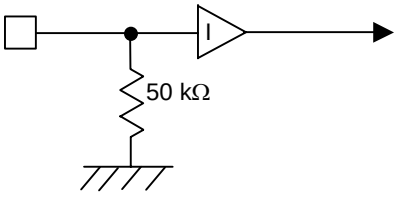
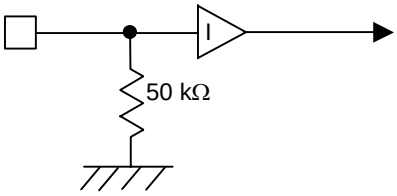
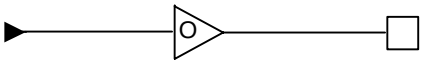
Pin No.	Symbol	I/O	Description	At reset	Active level	Type of I/O	Drive performance
35	XD6	in/out	External bus input/output data 6	Hi-Z	—		4 mA
36	XD7	in/out	External bus input/output data 7	Hi-Z	—		4 mA
37	XD8	in/out	External bus input/output data 8	Hi-Z	—		4 mA
38	XD9	in/out	External bus input/output data 9	Hi-Z	—		4 mA
39	XD10	in/out	External bus input/output data 10	Hi-Z	—		4 mA
40	XD11	in/out	External bus input/output data 11	Hi-Z	—		4 mA
41	XD12	in/out	External bus input/output data 12	Hi-Z	—		4 mA
42	XD13	in/out	External bus input/output data 13	Hi-Z	—		4 mA
44	XD14	in/out	External bus input/output data 14	Hi-Z	—		4 mA
45	XD15	in/out	External bus input/output data 15	Hi-Z	—		4 mA
47	XCSN	in	Chip enable signal	—	Low		—
49	XWEN	in	Write enable signal	—	Low		—
51	XREN	in	Read enable signal	—	Low		—
53	XWAIT	out	Wait signal	Low	High		4 mA
54	DREQ	out	DMA request 0/1= no request / request	Low	High		4 mA
55	DACK	in	DMA acknowledge 0/1= no clear / clear Connect this pin to GND when performing program transfer using the DMA signal control register.	—	High	Pull-down	—
56	INTN	out	Interrupt signal output	High	Low		2 mA
Clock/Reset (3 pins)							
13	RSTN	in	Reset 0: active	—	Low	Schmitt, pull-up	—
4	XI	—	Input clock (27 MHz)	—	—		—
5	XO	—	Input clock (27 MHz)	—	—		—
Test mode related (3 pins)							
9	TMODE0	in	Test mode signal 0	—	—	Schmitt, pull-down	—
10	TMODE1	in	Test mode signal 1	—	—	Schmitt, pull-down	—
11	TNODE2	in	Test mode signal 2	—	—	Schmitt, pull-down	—
Unused signal (1 pin)							
142	NC	in	Unused pin Connect this pin to GND.	—	—		—
Power supply/GND (40 pins)							
6,14,48, 58,76,93, 109	VDDIO	in	Digital power supply (I/O)	—	—		—
3,12, 52, 74, 95, 108, 127	GNDIO	in	Digital GND (I/O)	—	—		—
8, 26, 34,	VDDCORE	in	Digital power supply (CORE)	—	—		—

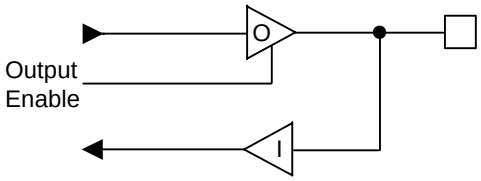
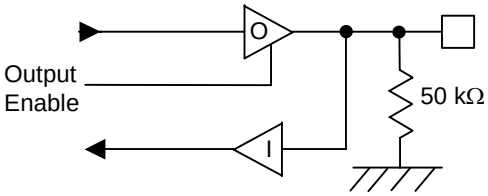
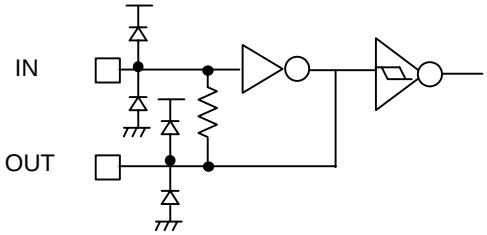
Pin No.	Symbol	I/O	Description	At reset	Active level	Type of I/O	Drive performance
43, 50, 69, 82, 92, 104,115, 130, 143							
7, 24, 33, 46, 57, 68, 78, 89, 103, 118, 129, 141	GNDCORE	in	Digital GND (CORE)	—	—		—
1	VDDPLL	in	Analog (PLL) power supply	—	—		—
2	GNDPLL	in	Analog (PLL) GND	—	—		—

1.3.4 Pin Structure

Table 1-1 shows the simplified pin structures of this LSI.

Table 1-1 Type of Pin Structure

Type of pin	Pin name (symbol)	Pin structure
Input Pin	XA 9-0, XCSN, XWEN, XREN, YUVDATA7-0, VSYNC, HSYNC, FIELDTOP	 TTL input
	CLKCAM	 TTL Schmitt input
	RSTN	 TTL Schmitt input, with 50 kΩ pull-up resistor
	DACK	 TTL input, with 50 kΩ pull-down resistor
	TMODE1, TMODE2, TMODE3	 TTL Schmitt input, with 50Ω pull-down resistor
Output Pin	DREQ, INTN, SDADRS 12-0 SDCLK, SDCKE, SDCSN, SDCASN, SDWEN, SDDQM, SDRASN,XWAIT	 Output

Type of pin	Pin name (symbol)	Pin structure
Input/output Pin	XD15–0	 TTL input and output
	SDDATA31–0	 TTL input, with 50 kΩ pull-down resistor
Oscillator pin	XI, XO	 Oscillator pins

1.3.5 Handling of Unused Pins

Table 1-2 shows how unused pins of this LSI should be handled. The other input pins must also be connected with signal lines according to their purposes.

Table 1-2 Handling of Unused Pins

Pin name (symbol)	Pin handling (connection)
NC	GND

[Note]
- If any digital input pin is left open, current consumption may increase substantially.
- Never leave the power supply pins or the GND pins open.

2. Description of Software

2.1 Register Description

2.1.1 List of Registers

Use	Address	Register name	Symbol	R/W	Size	Initial value
LSI control	0x000	LSI status register	STATUS	R/W	8/16	0x0000
	0x004	Interrupt status register	INTSTS	R/W	8/16	0x0000
	0x008	Interrupt mask register	INTMSK	R/W	8/16	0x00FF
	0x00C	External interface configuration register	BUSIFCNFG	R/W	8/16	0x0000
	0x010	Output stream access size register	STRMACCSIZ	R/W	8/16	0x0002
	0x014	DMA signal control register	DMACNTL	R/W	8/16	0x0000
Input parameter	0x100	Input image setup register	INIMAGE	R/W	8/16	0x0061
	0x104	Input image capture mode setting register	IMGCPTMODE	R/W	8/16	0x0032
	0x108	Vertical capture start pixel setting register	VSTART	R/W	8/16	0x0000
	0x10C	Horizontal capture start pixel setting register	HSTART	R/W	8/16	0x0000
	0x110	Input image data range conversion setting register	IMGRANGE	R/W	8/16	0x0002
MPEG-4 encoding control	0x180	Profile setting register	ENCPROFILE	R/W	8/16	0x0051
	0x184	Coding type setting register	CODINGTYPE	R/W	8/16	0x0001
	0x188	Rate control quantization type setting register	RATECNTLTYPE	R/W	8/16	0x0012
	0x18C	Bit rate setting register 1	BITRATE1	R/W	8/16	0x0900
	0x18E	Bit rate setting register 2	BTRATE2	R/W	8/16	0x003D
	0x190	Input frame skipping setting register	ENCFRAMERATE	R/W	8/16	0x0001
	0x194	Intra-refresh rate setting register	INTRAREFRESHRATE	R/W	8/16	0x000F
	0x19C	Maximum quantization step size setting register	MAXQUANT	R/W	8/16	0x0018
	0x1A0	Intra-quantization step size setting register	INTRAQUANT	R/W	8/16	0x0008
	0x1A4	Inter-quantization step size setting register	INTERQUANT	R/W	8/16	0x0008
Output stream	0x200 to 0x23F	Output stream register	STRMDATA	R	8/16	0x0000
	0x240	Output stream size register 1	STRMSIZ1	R	8/16	0x0000
	0x242	Output stream size register 2	STRMSIZ2	R	8/16	0x0000

Note: Do not access any area other than those shown above.

2.1.2 LSI Status Register (STATUS)

Address: 0x000
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	softrst	–*	–*	enable	–*	–*	register_ ready	LSI_ready
Access	W	–	–	R/W	–	–	R	R
Initial value	0	0	0	0	0	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register indicates the status of this LSI. Also, this register is used to start or stop encoding processing.
Bit 1 of this register and all the other registers than this can be accessed only after bit 1 of this register is set to "1".

[Description of Bits]

- **LSI_ready** (bit 0)
  Indicates that encoding is enabled (the enable bit can be set to "1").
  During reset, this bit is set to 0. After reset is released, this bit is set to 1 at completion of SDRAM automatic initialization.

LSI_ready	Description
0	The LSI is being reset (standby).
1	Initialization of SDRAM completed after reset release (ready).

- **register_ready** (bit 1)
  Indicates that register access (setting) is enabled.
  This bit is set to 0 during reset and 1 after release of reset.

register_ready	Description
0	The LSI is being reset (standby).
1	Reset has been released (ready).

- **enable** (bit 4)
  This bit enables or disables the LSI.

enable	Description
0	Disable (Initial value)
1	Enable

- **softrst** (bit 7)
  Writing "1" to this bit makes a soft reset (for a soft reset, see Section 4.1, "Reset") to the entire LSI. After the reset is asserted, this register is automatically cleared to 0. This bit is write only. (The read value is undefined.)

softrst	Description
0	Setting prohibited
1	Resets the LSI.

2.1.3 Interrupt Status Register (INTSTS)

Address: 0x004
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	status[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register indicates the type of interrupt source.
If an exception of bit 5 occurs, software reset must be executed for the LSI. After interrupt is asserted, this register is cleared to "0" by writing "1" to the interrupt cause (source) bit.

[Description of Bits]
- **status[7:0]** (bits 7 to 0)
  - One-frame-data ready (bit 0)
    Indicates that one frame of stream data is ready.
  - One-frame-data read complete (bit 1)
    Indicates that reading of one frame of stream data has been completed.
  - LSI ready(bit 2)
    Indicates that encoding processing is enabled (the Enable bit of the status register can be set to "1"). During reset, this bit is set to 0 and it is set to 1 at completion of initialization of SDRAM after release of reset. This bit is set to 1 at completion of transition to a suspended state.
  - Register ready (bit 3)
    Indicates that register access (setting) is enabled (excluding the enable bit of the status register). This bit is set to 0 during reset and it is set to 1 after release of reset.
  - Capture error (bit 4)
    See Section 3.5, "Exception Processing."
  - Encoding abnormality (bit 5)
    See Section 3.5, "Exception Processing."
  - Stream data read abnormality (bit 6)
    See Section 3.5, "Exception Processing."
  - Set bit rate exceeded (bit 7)
    See Section 3.5, "Exception Processing."

Each status bit	Description
0	No interrupt generated (Initial value)
1	Interrupt generated

2.1.4 Interrupt Mask Register (INTMSK)

Address: 0x008
Access: R/W
Access size: 8/16 bits
Initial value: 0x00FF

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	intemask[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to enable or disable each interrupt of the interrupt status register. Disable or enable can be set for each interrupt source. When an interrupt source is masked and an exception of the masked source occurs, the interrupt signal is not asserted, but the exception occurrence cause is reflected in the status bit of the interrupt status register (set to 1).
As the initial value, all interrupts are masked.

[Description of Bits]
- **intemask[7:0]** (bits 7 to 0)

Each intemask bit	Description
0	Enables interrupts (no mask).
1	Disables (masks) interrupts (Initial value).

2.1.5 External Interface Configuration Register (BUSIFCNFG)

Address: 0x00C
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	amux[1:0]		–*	–*	–*	hostbw
Access	–	–	R/W	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the bus width of the host CPU and the column length of DRAM.

[Description of Bits]

- **hostbw** (bit 0)
  This bit sets Host CPU bus width.
  Set the data bit width of bus interface with the host CPU.
  When this bit is set to 1, 16-bit access must be used even if the stream data has odd-number bytes in size.
  When this bit is set to 1, 8-bit (1-byte) access cannot be made.

hostbw	Description
0	8 bits (Initial value)
1	16 bits

- **amux[1:0]** (bits 5 to 4)
  These bits set DRAM column length.
  Set the column address length of SDRAM.

amux[1:0]	Description
00	8 bits (Initial value)
01	9 bits
10	10 bits
11	Setting prohibited

  Note:
  Set the column address length according to the DRAM to be connected. For details refer to the documents attached to the DRAM used.

2.1.6 Output Stream Access Size Register (STRMACCSIZ)

Address: 0x010
Access: R/W
Access size: 8/16 bits
Initial value: 0x0002

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	–*	–*	streamaccsiz[2:0]		
Access	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the access size for reading an output stream.

[Description of Bits]
- **streamaccsiz[2:0]** (bits 2 to 0)
  These bits specify output stream read access size.
  Specify the read size for asserting the DREQ signal when reading an output stream.
  Thiese bits indicate how many bytes of data will be read in one transfer.

streamaccsiz[2:0]	Description
000	1 byte
001	2 bytes
010	4 bytes (Initial value)
011	8 bytes
100	16 bytes
101	32 bytes
110	64 bytes
111	Setting prohibited

The DREQ signal will be asserted every number of bytes specified in this register.

2.1.7 DMA Signal Control Register (DMACNTL)

Address: 0x014
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	dack	–*	–*	–*	dreq
Access	–	–	–	R/W	–	–	–	R
Initial value	0	0	0	0	0	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used for controlling the DMA signal.
By using this register, stream data can be read through program transfer without connecting the DREQ or DACK signal. In this case, fix the DACK signal at a Low level.

[Description of Bits]

- **dreq** (bit 0)
  DMA signal contol
  This bit is used to make the DREQ/DACK signal of the external pin read/write enable from the register.
  Bit 0: DREQ
  ReadOnly
  This bit indicates the status of the DREQ signal of the external pin.
  This bit changes at the same timing as the change of the DREQ signal.

- **dack** (bit 4)
  Bit 4: DACK
  Read/Write
  This bit is used for an alternative to the DACK signal of the external pin. The DACK bit must be set to 0 by writing to the register after setting the DACK bit to 1 and confirming that the DREQ bit is at 0. After the DACK bit is set to 0, the next DREQ is asserted.

  Note:
  When not using the external DREQ/DACK pin, fix the DACK pin (input) to 0.

2.1.8 Input Image Setup Register (INIMAGE)

Address: 0x100
Access: R/W
Access size: 8/16 bits
Initial value: 0x0061

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	FrameRateID [1:0]		TopField First	Interlaced	–*	InImage [2:0]		
Access	R/W	R/W	R/W	–	–	R/W	R/W	R/W
Initial value	0	1	1	0	0	0	0	1

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the size, interlacing, and frame rate of input images.

[Description of Bits]

- **InImage [2:0]** (bits 2 to 0)
  These bits specify size of input images.

InImage [2:0]	Description
0	Setting prohibited
1	VGA (640x480) progressive (Initial value)
2	PAL (720x576) interlaced
3	NTSC (720x480) interlaced
4	Setting prohibited
5	Setting prohibited
6	QVGA (320x240) progressive
7	Setting prohibited

- **Interlaced** (bit 4)

This bit disables or enables interlacing.

Interlaced	Description
0	OFF (Initial value)
1	ON

- **TopFieldFirst** (bit 5)
  This bit specifies the field position during interlacing.

TopFieldFirst	Description
0	BOTTOM
1	TOP (Initial value)

- **FrameRateID [1:0]** (bits 7 to 6)
  These bits specify the frame rate of input images.

FrameRateID [1:0]	Description
0	Setting prohibited
1	30 (Initial value)
2	29.973
3	25

Note:
The following combinations are available when setting up the Input Image Setup Register (INIMAGE):

FrameRateID[1:0]	TopFieldFirst	Interlaced	InImage[2:0]	Description
—	—	—	0	Setting prohibited
1	1	0	1	VGA (640×480) (Initial value)
3	0	1	2	PAL (720×576)
2	1	1	3	NTSC (720×480)
—	—	—	4	Setting prohibited
—	—	—	5	Setting prohibited
1	1	0	6	QVGA (320×240)
—	—	—	7	Setting prohibited

2.1.9 Input Image Capture Mode Setting Register (IMGCPTMODE)

Address: 0x104
Access: R/W
Access size: 8/16 bits
Initial value: 0x0032

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	hsynclevel	vsynclevel	clkcamedge	vsyncmode	–*	savmode
Access	–	–	R/W	R/W	R/W	R/W	–	R/W
Initial value	0	0	1	1	0	0	1	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set various modes of input image capturing.

[Description of Bits]
- **savmode** (bit 0)
  This bit is for choosing SAV/EAV or SYNC mode.

savmode	Description
0	SYNC mode (Initial value) : Select this mode when set to VGA or QVGA.
1	SAV/EAV mode: Select this mode when set to NTSC or PAL.

- **vsyncmode** (bit 2)
  This bit specifies the mode of vsync detection.

vsyncmode	Description
0	Level detection mode (Initial value)
1	Edge detection mode

- **clkcamedge** (bit 3)
  This bit specifies the clock edge at which each of the YUVDATA, VSYNC, HSYNC, and FIELDTOP signals is captured.

clkcamedge	Description
0	negedge clkcam (Initial value)
1	posedge clkcam

- **vsynclevel** (bit 4)
  This bit specifies polarity of VSYNC.

vsynclevel	Description
0	Negative polarity
1	Positive polarity (Initial value)

- **hsynclevel** (bit 5)
  This bit specifies polarity of HSYNC.

hsynclevel	Description
0	Negative polarity
1	Positive polarity (Initial value)

Note:
Set this register according to the camera etc. to be connected. For details see Chapter 4, "External Interface."

2.1.10 Vertical Capture Start Pixel Setting Register (VSTART)

Address: 0x108
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	vstart [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the capture start position in the vertical direction.

[Description of Bits]
- **vstart [7:0]** (bits 7 to 0)
  These bits serves as parameters for specifying the capture start line in the vertical direction in 1-line units.

  Note:
  Set this register according to the camera etc. to be connected. For details see Chapter 4, "External Interface."

2.1.11 Horizontal Capture Start Pixel Setting Register (HSTART)

Address: 0x10C
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	hstart[9:8]	
Access	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	hstart[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the capture start position in the horizontal direction.

[Description of Bits]
- **hstart[9:0]** (bits 9 to 0)
  These bits serves as parameters for specifying the capture starting position in the horizontal direction in 1-pixel units.

  Note:
  Set this register according to the camera etc. to be connected. For details see Chapter 4, "External Interface."

2.1.12 Input Image Data Range Conversion Setting Register (IMGRANGE)

Address: 0x110
Access: R/W
Access size: 8/16 bits
Initial value: 0x0002

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	–*	–*	–*	VideoRange [1:0]	
Access	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the data range of input image data.

[Description of Bits]
- **VideoRange[1:0]** (bits 1 to 0)
  These bits set the range of image data conversion.

VideoRange[1:0]	Description
0	16–240 compression
1	16–240 clipping
2	0–255 (Initial value)
3	Setting prohibited

2.1.13 Profile Setting Register (ENCPROFILE)

Address: 0x180
Access: R/W
Access size: 8/16 bits
Initial value: 0x0051

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
		Level[3:0]			–*	–*	–*	Profile
Access	R/W	–	–	–	–	–	–	R/W
Initial value	0	1	0	1	0	0	0	1

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to determine the profile used for, and sets the level of, MPEG-4 encoding.
Available combinations are limited. See the use cases in Section 2.3 for the details.

[Description of Bits]

- **Profile** (bit 0)
  This bit is for determining the MPEG-4 encoding profile.

Profile	Description
0	Simple Profile
1	Advanced Simple Profile (Initial value)

- **Level[3:0]** (bits 7 to 4)
  These bits set the level of MPEG-4 encofing.

Level[3:0]	Description
3	Level 3
5	Level 5 (Initial value)
Others	Setting prohibited

2.1.14 Coding Type Setting Register (CODINGTYPE)

Address: 0x184
Access: R/W
Access size: 8/16 bits
Initial value: 0x0001

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	–*	–*	–*	–*	CodingType
Access	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	1

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the type of coding used for MPEG-4 encoding.

[Description of Bits]
- **CodingType** (bit 0)
  This bit sets the type of coding.

CodingType	Description
0	IIII
1	IPPP (Initial value)

2.1.15 Rate Control Quantization Type Setting Register (RATECNTLTYPE)

Address: 0x188
Access: R/W
Access size: 8/16 bits
Initial value: 0x0012

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	QuantType	–*	RateCntlBufSize [1:0]		RateCntl Type
Access	–	–	–	R/W	–	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	1	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the type of bit rate control and the type of quantization.

[Description of Bits]

- **RateCntlType** (bit 0)
  This bit sets the type of bit rate control.

RateCntlType	Description
0	CBR (Constant Bit Rate): Fixed bit rate (Initial value)
1	VBR (Variable Bit Rate): Variable bit rate

  Related registers: At CBR→Bit rate setting registers 1 to 3, maximum quantization step size setting register
  Related registers: At VBR→Intra-quantization step size register, inter-quantization step size register

- **RateCntlBufSize [1:0]** (bits 2 to 1)
  These bits set a bit rate control buffer size.
  These bits are enabled at CBR only. At VBR, set them to 1.
  The values that can be set are 1 to 3.

RateCntlBufSize [1:0]	Description
0	Setting prohibited
1	Buffer = 1 (Initial value)
2	Buffer = 2
3	Buffer = 3

  Note:
  If the buffer size is large, deterioration of image quality can be prevented to some extent even if a sudden change occurs in the image at a low bit rate. However, the delay time increases in 1-frame units. Set these bits to 1 at VBR.

- **QuantType** (bit 4)
  This bit set the type of quantization.

QuantType	Description
0	H.263 quantization: Select this when SP is selected.
1	MPEG quantization: Select this when ASP is selected. (Initial value)

Related register: Profile setting register

2.1.16 Bit Rate Setting Registers 1,2 (BITRATE1, 2)

BITRATE1
Address: 0x18C
Access: R/W
Access size: 8/16 bits
Initial value: 0x0900

	15	14	13	12	11	10	9	8
	BitRate [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	1

	7	6	5	4	3	2	1	0
	BitRate [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BITRATE2
Address: 0x18E
Access: R/W
Access size: 8/16 bits
Initial value: 0x003D

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	BitRate[22:16]						
Access	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	1	1	1	0	1

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set an average bit rate of output streams at CBR. The units are bits per seconds.
When the rate is set to a low bit rate, bit shortage occurs, causing frame omission.
When the bit rate is set to a high bit rate, the rate may not reach the bit rate that is set.

Values that can be set are limited depending on the profile used, as shown below.

For ASP@L5:
512000 ,1000000, 2000000, 4000000, 6000000
For SP@L3:
512000, 1000000, 2000000

[Description of Bits]

- **BitRate[15:0]** (bits 15 to 0)
- **BitRate[22:16]** (bits 6 to 0)
  These bits set an average bit rate of output streams at CBR.

  Related registers: Rate control quantization type setting register

2.1.17 Input Frame Skipping Setting Register (ENCFRAMERATE)

Address: 0x190
Access: R/W
Access size: 8/16 bits
Initial value: 0x0001

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	incull [5:0]					
Access	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	1

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set frame skipping of input images.
For instance, to set the output frame to 15 fps when the input image is 30 fps (VGA), set frame skipping to 1/2 by setting FrameRateID to 1 (= 30 fps) and this register to 2.
The frame rate is "input frame rate × (1/n)".

[Description of Bits]
- **incull [5:0]** (bits 5 to 0)
  The settable range varis depending on the type of input image. The following values can only be set. Other values are disabled.
  - When InImage = 1/6(VGA/QVGA), n = 1, 2, 30, 60
  - When InImage = 3(NTSC), n = 1, 2, 30, 60
  - When InImage = 2(PAL), n = 1, 2, 25, 50

  Related registers: Input image setup register

2.1.18 Intra-Refresh Rate Setting Register (INTRAREFRESHRATE)

Address: 0x194
Access: R/W
Access size: 8/16 bits
Initial value: 0x000F

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	IntraRefreshRate [4:0]				
Access	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set an intra frame insertion interval.

[Description of Bits]

- **IntraRefreshRate [4:0]** (bits 4 to 0)
  One of the following values can be set:
  5,10,15,25,30 [frames]
  Available combinations at parameter setting are limited. See the use cases in Section 2.3 for the details.

  This register is disabled when the type of coding is set to "IIII".

2.1.19 Maximum Quantization Step Size Setting Register (MAXQUANT)

Address: 0x19C
Access: R/W
Access size: 8/16 bits
Initial value: 0x0018

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	MaxQuant [4:0]				
Access	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	1	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the maximum quantization step size at CBR.
The lower the value, the higher the picture quality becomes; however, the number of bits required increases.
Bit shortage occurs depending on the bit rate set, causing frame omission.

[Description of Bits]
- **MaxQuant[4:0]** (bits 4 to 0)
  These bits set the maximum quantization step size. Valid when the type of bit rate control is set to CBR.

MaxQuant [4:0] [steps]	Description
16	High image quality
24	Standard (Initial value)
28	High compression
Others	Setting prohibited

Related registers: Rate control quantization type setting register

2.1.20 Intra-Quantization Step Size Setting Register (INTRAQUANT)

Address: 0x1A0
Access: R/W
Access size: 8/16 bits
Initial value: 0x0008

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	IntraVopQuant [4:0]				
Access	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the quantization step size of intra-images at VBR.
The lower the value, the higher the image quality becomes; however, the output stream size increases.

[Description of Bits]

- **IntraVopQuant [4:0]** (bits 4 to 0)
  These bits set intra-quantization step size. Valid when the type of bit rate control is set to VBR.

IntraVopQuant [4:0] [steps]	Description
4	High image quality
8	Standard (Initial value)
12	High compression
Others	Setting prohibited

Related register: Rate control quantization type setting register

2.1.21 Inter-Quantization Step Size Setting Register (INTERQUANT)

Address: 0x1A4
Access: R/W
Access size: 8/16 bits
Initial value: 0x0008

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access:	–	–	–	–	–	–	–	–
Initial value:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	InterVopQuant [4:0]				
Access:	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value:	0	0	0	0	1	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register is used to set the quantization step size of inter-images at VBR.
The lower the value, the higher the image quality becomes; however, the output stream size increases.

[Description of Bits]
- **InterVopQuant[4:0]** (bits 4 to 0)
  These bits set inter-quantization step size. Valid when the type of bit rate control is set to VBR.

InterVopQuant[4:0] [steps]	Description
4	High image quality
8	Standard (Initial value)
12	High compression
Others	Setting prohibited

Related register: Rate control quantization type setting register

2.1.22 Output Stream Register (STRMDATA)

Address: 0x200 to 0x23F
Access: R
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8
	streamdata [15:8]							
Access	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

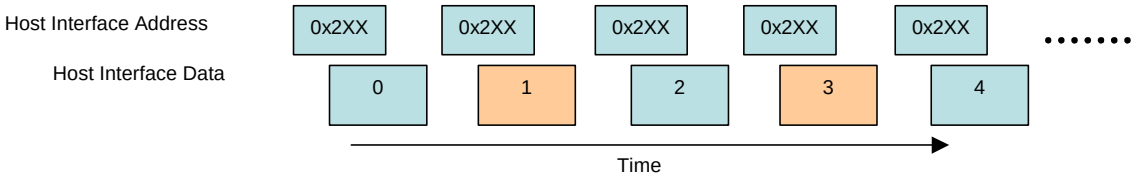
	7	6	5	4	3	2	1	0
	streamdata [7:0]							
Access	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

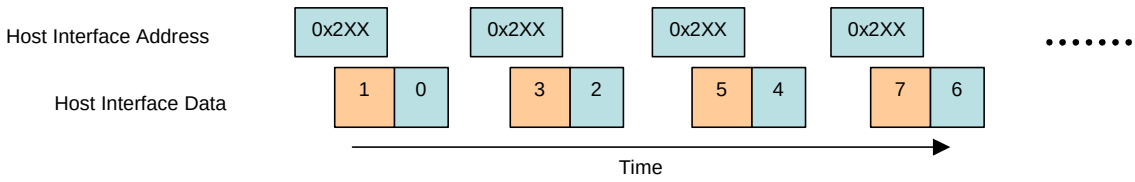
[Description of Register]
This register is used to read output streams.
Output streams can be read by reading this register after the output stream data DREQ signal is asserted. An identical value is read even if any position in the 16-word address space (0x200–0x23F) is read. Once DREQ is asserted, the data of the number of bytes specified in the "streamaccsiz" register can be read. DACK must be asserted from the host CPU after the specified number of bytes are read. This register is read only.

[Description of Bits]

- **streamdata [7:0]** (bits 7 to 0)
  These bits are used when the data bus width of the interface with the host CPU is set to 8 bits.
  (When the hostbw bit of the external interface setting register (BUSIFCNFG) is set to 0:) Output streams are read byte by byte in the sequence of generation.



- **streamdata [15:0]** (bits 15 to 0)
  These bits are used when the data bus width of the interface with the host CPU is set to 16 bits.
  (When the hostbw bit of the external interface setting register (BUSIFCNFG) to 1:) Output streams are read in 2-byte units in the sequence of generation and the reading of 2 bytes is performed in little-endian format.



2.1.23 Output Stream Size Registers 1, 2 (STRMSIZ1, STRMSIZ2)

STRMSIZ1
Address: 0x240
Access: R
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8
	streamsize [15:8]							
Access	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	streamsize [7:0]							
Access	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

STRMSIZ2
Address: 0x242
Access: R
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8
	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
	–*	–*	–*	–*	streamsize [19:16]			
Access	–	–	–	–	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

Note:
*: Bits marked as "–" will read "0" when read, but it is recommended that the program does not assume "0" at read (i.e., make it don't care).

[Description of Register]
This register indicates the size of an output stream (for each frame).The units are bytes per frames:
This information is necessary to determine the DMA transfer count when data is read from the host CPU through DMA transfer.

[Description of Bits]
- **streamsize [15:0]** (bits 15 to 0)
- **streamsize [19:16]** (bits 3 to 0)
  These bits indicate the output stream size. This register is read only.

2.2 Initial Settings of the Registers

The following initial settings are used to perform encoding:
Image size : VGA@30 fps,
Encoding method : ASP@Level5, CBR, Bit rate = 4 Mbps, Intra-refresh rate = 15
Video input section : VSYNC/HSYNC method (positive polarity), VSYNC detection = level detection mode

2.3 Standard Available Combinations (Use Cases) of Parameter Settings for MPEG Encoding

This section describes the possible combinations (use cases) of parameter settings for MPEG encoding in this LSI. Table 2-1 lists the uses of this LSI, encoding data requirements that are assumed for each use, and the typical parameter setting values.

Table2-1 Assumed Uses of This LSI and Typical Parameter Values

No.	Use	Parameter Setting																
		Input image				Profile and level		Type of coding	Rate control quantization			Bit rate (bps)	Input frame skipping	Intra-refresh rate	Quantization step		
		0x100				0x180		0x184	0x188			0x18C 0x18D 0x18E	0x190	0x194	0x19C	0x1A0	0x1A4
		InImage	Interlaced	TopFieldFirst	FrameRateID	Profile	Level	CodingType	RateCntlType	RateCntlBufSize	QuantType	BitRate	incull	IntraRefreshRate	MaxQuant	IntraVopQuant	InterVopQuant
1	Real time use	PAL	Inter-lace	Bottom First	25	ASP	5	IPPP	CBR	3	MPEG	6M	1	25	16	—	—
2												4M			24	—	—
3		0xD2				0x51		0x01	0x16			2M			24	—	—
4												1M			28	—	—
5												512K			28	—	—
6												6M	2	15	16	—	—
7												4M			24	—	—
8												2M			24	—	—
9												1M			28	—	—
10												512K			28	—	—
11		NTSC	Inter-lace	Top First	29.97	ASP	5	IPPP	CBR	3	MPEG	6M	1	30	16	—	—
12												4M			24	—	—
13		0xB3				0x51		0x01	0x16			2M			24	—	—
14												1M			28	—	—
15												512K			28	—	—
16												6M	2	15	16	—	—
17												4M			24	—	—
18												2M			24	—	—
19												1M			28	—	—
20												512K			28	—	—
21		VGA	Progres-sive	—	30	ASP	5	IPPP	CBR	3	MPEG	6M	1	30	16	—	—
22												4M			24	—	—
23		0x41				0x51		0x01	0x16			2M			24	—	—
24												1M			28	—	—
25												512K			28	—	—
26												6M	2	15	16	—	—
27												4M			24	—	—
28												2M			24	—	—
29												1M			28	—	—
30												512K			28	—	—

No.	Use	Parameter Setting																
		Input image				Profile and level		Type of coding	Rate control quantization			Bit rate (bps)	Input frame skipping	Intra-refresh rate	Quantization step		
		0x100				0x180		0x184	0x188			0x18C 0x18D 0x18E	0x190	0x194	0x19C	0x1A0	0x1A4
		InImage	Interlaced	TopFieldFirst	FrameRateID	Profile	Level	CodingType	RateCntlType	RateCntlBufSize	QuantType	BitRate	incull	IntraRefreshRate	MaxQuant	IntraVopQuant	InterVopQuant
31		QVGA	Progres-sive	—	30	SP	3	IPPP	CBR	3	H.263	1M	1	30	16	—	—
32												512K			24	—	—
33		0x46				0x30		0x01	0x06			1M	2	15	16	—	—
34												512K			24	—	—
35	Long-term accumulation of high-quality images	PAL	Inter-lace	Bottom First	25	ASP	5	IIII	VBR	1	MPEG	—	25	—	—	4	4
36		0xD2				0x51		0x00	0x13			—	50	—	—	4	4
37		NTSC	Inter-lace	Top First	29.97							—	30	—	—	4	4
38		0xB3										—	60	—	—	4	4
39		VGA	Progres-sive	-	30							—	30	—	—	4	4
40		0x41										—	60	—	—	4	4
41		QVGA	Progres-sive	-	30	SP	3		VBR	1	H.263	—	30	—	—	4	4
42		0x46				0x30			0x03			—	60	—	—	4	4
43		PAL	Inter-lace	Bottom First	25	ASP	5	IPPP	VBR	1	MPEG	—	25	10	—	4	4
44		0xD2				0x51		0x01	0x13			—	50	5	—	4	4
45		NTSC	Inter-lace	Top First	29.97							—	30	10	—	4	4
46		0xB3										—	60	5	—	4	4
47		VGA	Progres-sive	—	30							—	30	10	—	4	4
48		0x41										—	60	5	—	4	4
49		QVGA	Progres-sive	—	30	SP	3		VBR	1	H.263	—	30	10	—	4	4
50		0x46				0x30			0x03			—	60	5	—	4	4

No.	Use	Parameter Setting																
		Input image				Profile and level		Type of coding	Rate control quantization			Bit rate (bps)	Input frame skipping	Intra-refresh rate	Quantization step		
		0x100				0x180		0x184	0x188			0x18C 0x18D 0x18E	0x190	0x194	0x19C	0x1A0	0x1A4
		InImage	Interlaced	TopFieldFirst	FrameRateID	Profile	Level	CodingType	RateCntlType	RateCntlBufSize	QuantType	BitRate	incull	IntraRefreshRate	MaxQuant	IntraVopQuant	InterVopQuant
51	Low network lines	PAL	Inter-lace	Bottom First	25	ASP	5	IPPP	CBR	1	MPEG	512K	25	10	24	—	—
52		0xD2				0x51		0x01	0x12				50	5	16	—	—
53		NTSC	Inter-lace	Top First	29.97							512K	30	10	24	—	—
54		0xB3											60	5	16	—	—
55		VGA	Progres-sive	—	30							512K	30	10	24	—	—
56		0x41											60	5	16	—	—
57		QVGA	Progres-sive	—	30	SP	3		CBR	1	H.263	512K	30	10	24	—	—
58		0x46				0x30			0x02				60	5	16	—	—

3. Description of Operation

3.1 States of Operation

This LSI can enter the following four states of operation.

Table 3-1 States of Operation

State of operation	Description
Reset	The LSI is being reset. There are two resets: A "hard reset," which is a reset by hardware, and a "soft reset," which is a reset by software. For the details of these two resets, see Section 4.1, "Reset."
Register Ready (SDRAM being initialized)	The LSI is initializing SDRAM. Registers can be set. However, the following settings are prohibited: •Activation of MPEG-4 encoding by setting the enable bit of the LSI status register to "1". •Execution of soft reset by setting the softrst of the LSI status register to "1"'.
LSI Ready (Standby)	The LSI is standby. Registers can be set. MPEG-4 encoding can be activated by setting the enable bit of the LSI status register to "1". A soft reset can be executed by setting the softrst bit of the LSI status register to "1".
Run (Encoding being executed)	The LSI is executing MPEG-4 encoding. MPEG-4 encoding can be stopped by setting the enable bit of the LSI status register to "0". A soft reset can be executed by setting the softrst bit of the LSI status register to "1".

*1: See the item of "Explanatory notes to the table" in Section 3.2.

3.1.1 Diagram of Transition of the States of Operation

Figure 3-1 shows how the states of operation of this LSI transition.

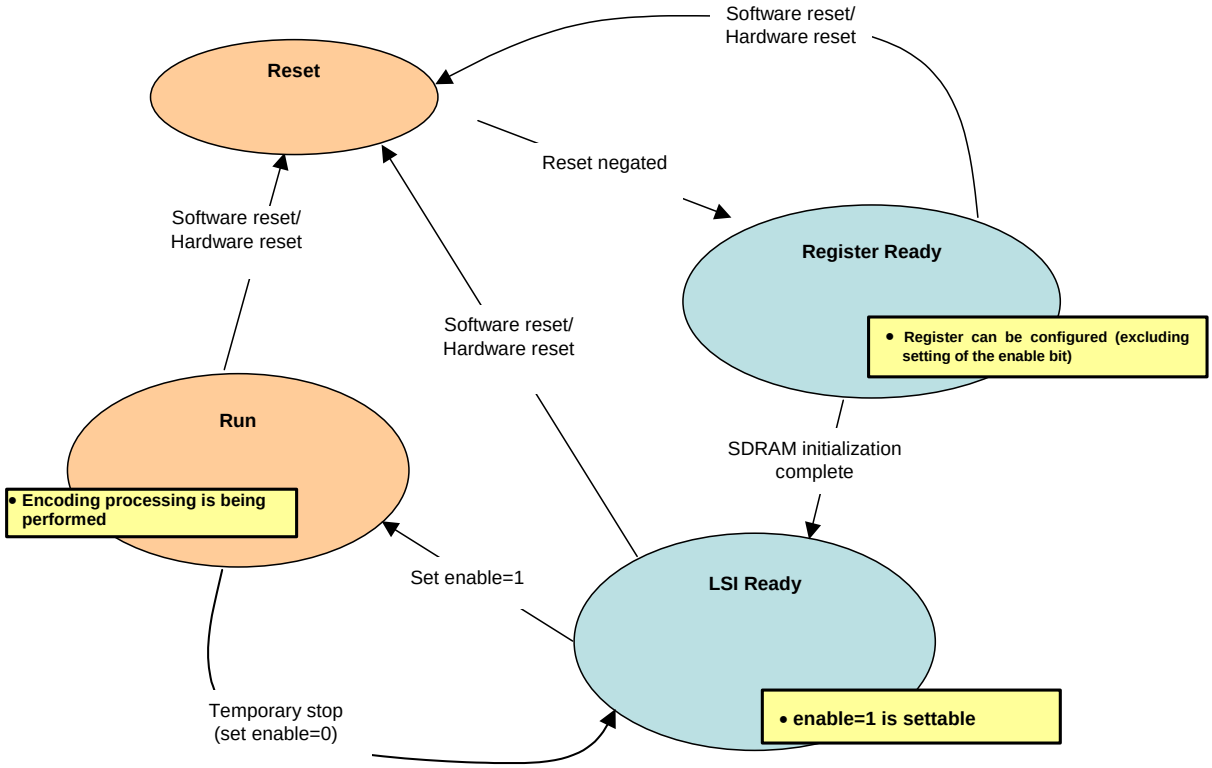


Figure 3-1 Transition of the States of Operation

Register Ready : Transition to this state from any other state can be confirmed with bit 3 (register_ready = 1) of the interrupt status register.

LSI Ready : Transition to this state from any other state can be confirmed with bit 2 (LSI_ready = 1) of the interrupt status register.

3.2 Procedure for Activating MPEG-4 Encoding

MPEG-4 encoding starts by activation of encoding and terminates by suspension of encoding or by a reset.
Table 3-2 shows the example of software procedure at the host CPU for MPEG-4 encoding activation.
The processing status of this LSI is reflected in the interrupt status register and is posted to the host CPU by an interrupt or polling of the interrupt status register.
Each interrupt source can be masked to suppress the occurrence of interrupt.
Table 3-2 shows the case where polling is used for all the interrupt sources.

Explanatory notes to the table:

(1) "register-name[m:n]" : Indicates the m-th through the n-th bits of the register .

(2) "left-member-value = right-member-value" : Indicates that the left member value and the right member value are equal.

(3) "left-member-value = = right-member-value" : Indicates that whether the left member value and the right member value are equal is judged.

(4) "left-member-value <= right-member-value" : Indicates that the right member value should be written to the left member value.

Table 3-2 Example of Software Procedure for MPEG-4 Encoding Activation

State of LSI's operation	LSI (hardware)	Host CPU program
Reset	•The LSI is being reset.	(*1)
Register Ready	•Start initialization of SDRAM. •The interrupt mask register is masked (all the bits = "1"). (INTMSK[7:0] = 0xFF) •Interrupt status register: register_ready bit (bit 3) = "1". (INTSTS[7:0] = 0x08) •The bit width of the XBUS data bus (XD) is set to 8 bits. (BUSIFCNFG[0] = 0)	
		[01] •Check that the interrupt status register is in the Register Ready state by reading the interrupt status register. ((INTSTS[7:0] & 0x08) == 0x08) The program cannot proceed to the subsequent processing until the interrupt status register enters the Register Ready state.
		[02] •If an interrupt is used to post the processing status from the LSI to the host CPU, release the mask by setting the interrupt mask register to "0". (INTMSK[7:0] <= Setting value) (*2)

State of LSI's operation	LSI (hardware)	Host CPU program
Register Ready		[03] •By writing to the interrupt status register, clear the register_ready bit (bit 3) of it. (INTSTS[7:0] <= 0x08)
	•The interrupt status register is changed to: register_ready bit (bit 3) = "0".	
		[04] •Set the bit width of XBUS's data bus (XD) by writing to the external interface setting register. - When the bus width is 8 bits: BUSIFCNFG[0] <= 0 - When the bus width is 16 bits: BUSIFCNFG[0] <= 1 (*3) At the same time, set also the column address bit width of SDRAM. (BUSIFCNFG[5:4] <= Setting value)
	•The bit width setting of the data bus (XD) of XBUS is the value set in [04]. (BUSIFCNFG[0] = 0) or (BUSIFCNFG[0] = 1)	
		[05] •Set the video input parameter by writing to the register related to the video input parameter. (INIMAGE[7:0] <= Setting value IMGCPTMODE[7:0] <= Setting value etc.) (*4)
		[06] •Reference the use cases in Section 2.3, then set values in the register that is related to MPEG-4 encoding control by writing to the register. (ENCPROFILE[7:0] <= Setting value CODINGTYPE[7:0] <= Setting value etc.) (*5)
		[07] •Set a value in the output stream access size register by writing to the register. (STREAMACCSIZ[2:0] <= Setting value) (*6)
LSI Ready	•Since SDRAM initialization is completed, the LSI enters the LSI Ready state, enabling activation of MPEG-4 encoding. • The interrupt status register is changed to: LSI_ready bit (bit 2) = "1".	

State of LSI's operation	LSI (hardware)	Host CPU program
LSI Ready		[08] •Check that the interrupt status register is in the LSI Ready state by reading the interrupt status register. ((INTSTS[7:0] & 0x04) == 0x04) The program cannot proceed to the subsequent processing until the interrupt status register enters the LSI Ready state.
		[09] •Clear bit 2 (LSI_ready) of the interrupt status register by writing to the register. (INTSTS[7:0] <= 0x04)
	•The interrupt status register is changed to: LSI_ready bit (bit 2) = "0".	
		[10] •Set the enable bit of the LSI status register by writing to the register. (STATUS[7:0] <= STATUS[7:0] | 0x10)
	•The LSI enters the Run state.	
Run	•The LSI enters the RUN state and starts MPEG-4 encoding.	
Operation after activation will be explained in Section 3.3, "Stream Data Transfer."		

*1: Any register cannot be accessed while the LSI is being reset.

*2: Once step [02] is over, the mask of the interrupt mask register can be released at arbitrary timing.
In this example, the host CPU program sets the ML86410 to an interrupt mask state so as not to generate an interrupt; the host CPU recognizes the LSI processing status by polling the interrupt status register.

*3: Execution of step [04] is allowed even if the LSI is in the "LSI Ready" state.

*4: Execution of step [05] is allowed even if the LSI is in the "LSI Ready" state.
Register setting in step [05] can be performed in any order.
Also, [05], [06], and [07] can be in the reverse order.

*5: Execution of step [06] is allowed even if the LSI is in the "LSI Ready" state.
Register setting in step [06] can be performed in any order.
Also, [05], [06], and [07] can be in the reverse order.

*6: Execution of step [07] is allowed even if the LSI is in the "LSI Ready" state.
Steps [05], [06], and [07] can be executed in any order.

3.3 Procedure for Stream Data Transfer

Processing in which a host CPU reads image data that has been encoded by this LSI (referred to as stream data) is called stream data transfer.
Stream data transfer is performed in frame units and is composed of the following three sections according to the execution sequence.

(1) One-frame-data ready (*1)	When encoding of one frame of data is completed, the LSI notifies the host CPU of data ready using the one-frame-data ready bit of the interrupt status register. When the host CPU receives the notification, it clears the one-frame-data ready bit of the interrupt status register. After that, it completes processing (1) by reading the output stream size registers (STRMSIZ1,2), then control is passed to processing (2). (*1)
(2) One-frame data transfer	The host CPU reads the encoded data from this LSI. Data transfer starts by assertion of the DREQ signal from the LSI to the host CPU. Processing (2) is completed by reading from the LSI the stream data of the output stream size that was acquired in (1). Control is then passed to processing (3). DMA transfer and program transfer are available as the methods of reading stream data. (See Sections 3.3.1 and 3.3.2)
(3) One-frame data transfer completion	When data transfer for one frame is completed, the LSI notifies the host CPU of completion of data transfer by the one-frame data read completion bit of the interrupt status register. When the host CPU receives the notification, it completes processing (3) by clearing the one-frame data read completion bit of the interrupt status register, then control is passed to processing (1).

*1: When the one-frame-data ready bit of the interrupt mask register is masked, this LSI terminates the processing of one-frame-data ready section without waiting for the reading of the output stream size registers (STRMSIZ1,2) and proceeds to processing (2).

Table 3-3 to Table 3-5 show the software procedures.

Table 3-3 Example of Software Procedure for One-Frame-Data Ready Section

State of LSI's operation	LSI (hardware)	Host CPU program
Run	•The LSI is executing encoding	
	•When one frame is encoded, the interrupt status register is set to (INTSTS[0] = "1"), indicating one frame of data being ready.	
		[11] •Check that the interrupt status register is in the one-frame-data ready state by reading the interrupt status register. ((INTSTS[7:0] & 0x01) == 0x01) The program cannot proceed to subsequent processing until the interrupt status register enters one-frame-data ready state.
		[12] •Clear bit 1 (one-frame-data ready) of the interrupt status register by writing to the interrupt status register. (INTSTS[7:0] <= 0x01)
	•The one-frame-data ready bit of the interrupt status register is set to "0". (INTSTS[0] = "0") •As a result, the LSI enters an output stream size register (STRMSIZ1,2) read wait state.	
		[13] •Acquire the output stream size by reading the output stream size registers. (STRMSIZ1,2)

*1: When the one-frame-data ready bit of the interrupt mask register is masked, this LSI terminates the processing of one-frame-data ready section without waiting for the reading of the output stream size registers (STRMSIZ1,2) and proceeds to processing (2).

Table 3-4 Example of Software Procedure for One-Frame Data Transfer Section

State of LSI's operation	LSI (hardware)	Host CPU program
Run	•When the output stream size registers (STRMSIZ1,2) have been read, the LSI starts stream transfer with the host CPU by handshaking.	[14] To perform stream transfer using DMAC, reflect the output stream size into DMAC and enable the DMAC. To perform stream transfer directly without using DMAC, store the output stream size in the variable. See Sections 3.3.1 and 3.3.2 for the details.

Table 3-5 Example of Software Procedure for One-Frame Data Transfer Completion Section

State of LSI's operation	LSI (hardware)	Host CPU program
Run		
	•At completion of data transfer of one frame, the status register is set to (INTSTS[1] = "1"), indicating the completion of one-frame data read.	
		[15] •Check that the interrupt status register is in a state where one-frame data read is complete by reading the interrupt status register. ((INTSTS[7:0] & 0x02) == 0x02) The program cannot proceed to the subsequent processing until the interrupt status register enters the one-frame data read complete state.
		[16] •Clear bit 1 (one-frame data read completion) of the interrupt status register by writing to the interrupt status register. (INTSTS[7:0] <= 0x02)
	•The one-frame data read completion bit of the interrupt status register is set to "0". (INTSTS[1] = "0")	
	•LSI is executing encoding	
Returns to the one-frame-data ready completion section of the next frame (Table3-3).		

3.3.1 Procedure for DMA Transfer

Table 3-6 shows an example of the software procedure for the one-frame data transfer section when the host CPU performs stream transfer (DMA transfer) using a DMA controller (DMAC).
For how to connect the host CPU and this LSI, see Section 4.3, "Host CPU Interface."

Table 3-6 Example of Software Procedure for One-Frame Data Transfer Section (for DMA Transfer)

State of LSI's operation	LSI (hardware)	Host CPU program
Run	•When the output stream size registers (STRMSIZ1,2) have been read, the LSI starts stream transfer with the host CPU by handshaking.	[14-1] To perform stream transfer using MAC, reflect the output stream size into DMAC control register and enable the DMAC. (*1)
	<01> •Asserts the DMA transfer request signal (DREQ).	
	<02> Waits until the host CPU reads the stream data of the number of bytes specified in the output stream read access size register (STRMACCSIZ). (*1)	
	<03> If the DMAC transfer acknowledgement signal (DACK) that is sent from the host CPU is active, control proceeds to <04> and if it is inactive, stop at <03>. (*2)	
	<04> Since DACK is active, the LSI deasserts DREQ.	
	<05> If the DMA transfer acknowledgment signal (DACK) from the host CPU is inactive, control proceeds to <06>. If it is active, stops at <05>. (*5)	
	<06> If the number of bytes of the stream data that has been read is equal to or greater than the number of bytes indicated by the output stream size registers (STRMSIZ1,2), control proceeds to <07>. Otherwise, the LSI returns to <01>. (*1)	
	<07> Terminates the one-frame data transfer section.	

*1: The number of bytes of stream data that is read by the host CPU must be the minimum number that satisfies the following conditions:

1) An integer multiple of the number of bytes specified by the output stream access size register (STRMACCSIZ) and
2) the number of bytes greater than or equal to the output stream size register (STRMSIZ1,2) value that has been read.

*2: This LSI operates by recognizing the signal level (active/inactive) of the DACK signal. This LSI does not recognize the rising/falling edge of the DACK signal.

3.3.2 Procedure for Program Transfer

Direct stream transfer by the host CPU without using DMAC is referred to as program transfer in this LSI.
For how to connect the host CPU and this LSI, see Section 4.3, "Host CPU Interface."
At program transfer, the host CPU must emulate handshaking by the DREQ/DACK signal in DMA transfer. The following handshaking emulation methods are available.

(1) Access the DMA signal control register (DMACNTL) that is incorporated in this LSI.
In this case, connection between the host CPU and the DREQ/DACK signal becomes unnecessary.
In this case, fix the DACK input pin of this LSI to inactive (Low).

(2) Access the general-purpose I/O port (GPIO) that is incorporated in the host CPU by connecting it with the DREQ/DACK pin of this LSI.

Table 3-7 shows an example of the software procedure of the one-frame data transfer section when the host CPU performs program transfer.

For the software procedure applied when the host CPU performs program transfer using the method (2), interpret the DMACNTL register read access and write access as the following phrases:

- Interpret the DMACNTL register read access as the read access to the register of the general-purpose I/O port connected to the DREQ pin of this LSI.
- Interpret the DMACNTL register write access as the write access to the register of the general-purpose I/O port connected to the DACK pin of this LSI.

Table 3-7 Example of Software Procedure for One-Frame Data Transfer Section (for Program Transfer Using the DMACNTL Register)

State of LSI's operation	LSI (hardware)	Host CPU program
Run	•When the output stream size registers (STRMSIZ1,2) have been read, the LSI starts stream transfer with the host CPU by handshaking.	[14-1] To perform stream transfer using program transfer, store the output stream size in the variable. (*1)
	<01> •Asserts the DMA transfer request signal (DREQ). •Waits until the host CPU reads the stream data of the number of bytes specified in the output stream read access size register (STRMACCSIZ). (*1)	
		[14-2] •Read the DMA signal control register and wait until the dreq bit of it is set to "1". (DMACNTL[7:0] & 0x01 == 0x01)
		[14-3] •Read the stream data of the number of bytes specified in the output stream access size register (STRMACCSIZ) from the output stream register (STRMDATA). (*2)

State of LSI's operation	LSI (hardware)	Host CPU program
Run	<03> If the DMA transfer acknowledgement signal (DACK) from the host CPU or the dack bit of the DMA signal control register (DMACNTL) is active, control proceeds to <04>. If it is inactive, stops at <03>. (*2)	[14-4] •Write "1" to the dack bit of the DMA signal control register (DMACNTL). (DMACNTL[7:0] <= 0x10) •Read the DMA signal control register and wait until the dreq bit of it is set to "0". (DMACNTL[7:0] & 0x01 == x01)
	<04> Since DACK is active, the LSI deasserts DREQ.	
	<05> If the dack bit of the DMA signal control register (DMACNTL) is inactive, control proceeds to <06>. If it is active, control stops at <05>. (*2)	[14-5] •Write "0" to the dack bit of the DMA signal control register (DMACNTL). (DMACNTL[7:0] <= 0x00) •If the number of bytes of the stream data that was read is greater than or equal to the number of bytes indicated in the output stream size registers (STRMSIZ1,2), control proceeds to [14-6]. Otherwise, returns to [14-2]. (*1)
	<06> The number of bytes of the stream data that was read is greater than or equal to the number of bytes indicated in the output stream size registers (STRMSIZ1,2), control proceeds to <07>). Otherwise, control returns to <01>. (*1)	[14-6] Terminate the one-frame data transfer section.
	<07> Terminates the one-frame data transfer section.	

*1: The number of stream data bytes that are read by the host CPU must be the minimum number that satisfies the following conditions.

- An integer multiple of the number of bytes specified by the output stream access size register (STRMACCSIZ) and
- Has the number of bytes greater than or equal to the number of bytes indicated by the output stream size register (STRMSIZ1,2) value that was read

*2: For program transfer, faster stream transfer can be achieved by specifying the number of bytes in the output stream access register (STRMACCSIZ) according to the architecture of the host CPU used. For instance, if the host CPU is an ARM processor, specify
STRMACCSIZ[2:0] <= 0x7 (64 bytes) and
execute two LDM (LoaD Multiple) instructions (specifying eight general-purpose registers (= 8*4 bytes) for the destination) as transfer of stream data of 64 bytes.

3.4 Procedure for Suspending/Restarting Encoding

That the LSI which is executing MPEG4 encoding stops encoding by a request from the host CPU is called suspension of encoding or simply suspension.
A suspension request is issued by writing "0" to the enable bit of the LSI status register.
By suspension, this LSI transitions from the Run state to the LSI Ready state.
During suspension, this LSI retains the contents of the registers. Therefore, encoding can be restarted by writing "1" to the enable bit of the LSI status register without resetting the video input parameter of a register or MPEG-4 encoding parameters. (After restart, streaming starts from the start code and the time code starts from 0.)
It is also possible to change the MPEG-4 encoding parameters.
Table 3-8 shows the outline of suspension and restart.

Table 3-8 Outline of MPEG-4 Encoding Activation/Suspension/Restart

State of LSI's operation	LSI (hardware) & host CPU program	Host CPU program
LSI Ready	Activate MPEG-4 encoding	
Run	1st frame: One-frame-data ready / One-frame-data transfer / One-frame data transfer completion 2nd frame: One-frame-data ready / One-frame data transfer / One-frame data transfer completion : : n-th frame: One-frame-data ready / One-frame data transfer / One-frame data transfer completion	← Suspension request
	Encoding suspension processing	
LSI Ready		← Restart request
Run	m-th frame: One-frame-data ready / One-frame data transfer / One-frame data transfer completion (m+1)-th frame: One-frame-data ready / One-frame data transfer / One-frame data transfer completion : :	

Operation is not guaranteed if a suspension request is issued in a state other than the Run state
If this LSI is in the Run state, a suspension request can be issued at any time unless "encoding suspension processing" is in progress.

After issuing a suspension request, this LSI and the host CPU software completes the processing up to "one-frame data transfer completion" that is currently being executed, and after that, control is passed to "Encoding suspension processing" (Table 3-8, n-th frame).

After "1-frame-data transfer completion," the contents of data in the frame are valid without being affected by the suspension request (Table 3-8, n-th frame).

However, if a suspension request is issued during processing of "one-frame data transfer completion", it is possible that this LSI does not suspend processing even after completion of the processing of the frame being executed, executes the next frame processing, and executes "encoding suspension processing" after the processing of "one-frame data transfer completion" (Table 3-9, (n+1)-th frame).

To ensure the suspension of encodint after completion of the current frame without executing the next frame, the register write access for the suspension request must be completed 500 nsec or more prior to the clearing of the one-frame-data read completion bit (INTSTS[7:0] <= 0x02) of the interrupt status register by the software on the host CPU side in the "one-frame data transfer completion processing" (see Table 3-5, "Example of Software Procedure for One-Frame Data Transfer Completion Section").

Table 3-9 When Encoding is not Suspended until the Next Frame is Completed

State of LSI's operation	LSI hardware & host CPU program	Host CPU program
Run	n-th frame: One-frame-data ready One-frame data transfer One-frame data transfer completion (m+1)-th frame: One-frame-data ready One-frame data transfer One-frame data transfer completion Encoding suspension processing	← Suspension request
LSI Ready		

Table 3-10 shows an example of software procedure for a suspension request, encoding suspension processing, and restart request.

Table 3-10 Example of Software Procedure for Suspension Request, Encoding Suspension Processing, and Restart Request

State of LSI's operation	LSI (hardware) & host CPU program	Host CPU program
Run	One-frame-data ready	
	One-frame data transfer	[Suspension request] (*1) (*2) [1-1] •Check that bit 2(LSI_ready) of the interrupt status register is at "0" by reading the interrupt status register. ((INTSTS[7:0] & 0x04) == 0x00) The program cannot proceed to step [1-2] until the bit is set to "0".
		[1-2] •Write "0" to the enable bit of the LSI status register. (STATUS[7:0] <= STATUS[7:0] & 0xFE)
	One-frame data transfer completion	[Encoding suspension processing] [2-1] •Check that bit 2 (LSI_ready) of the interrupt status register is at "0" by reading the interrupt status register. ((INTSTS[7:0] & 0x04) == 0x0) The program cannot proceed to step [2-2] until the bit is set to "1". (A normal frame read needs to be executed.)
	[Encoding suspension processing](*3) •Suspends encoding upon receiving a suspension request. •Sets the LSI_ready bit of the interrupt status register to "1". (INTSTS[2] = "1") •Sets the register_ready bit and LSI_ready bit of the LSI status register to "1". (INTSTS[7:0] = 0x3) •Terminates the encoding suspension processing.	
LSI Ready	•Encoding is being suspended.	[2-2] •Since bit 2 (LSI_ready) of the interrupt status register has been set to "1", clear all the bits of the interrupt status register to terminate processing. ((INTSTS[7:0] <= 0xFF)
		*4
		[Restart request] [3-1] •Write "1" to the enable bit of the LSI status register. (STATUS[7:0] <= STATUS[7:0] | 0x10)
Run	•Starts encoding upon receiving a restart request.	

*1: When an interrupt caused by some other unmasked interrupt source occurs during the period from the issuing of a suspension request to the setting of the LSI_ready bit of the LSI status register to "1" during the "encoding suspension processing", the interrupt by that source is asserted.

*2: After a suspension request is issued, the re-issuing of a suspension request is prohibited before completion of "encoding suspension processing".

*3: During "encoding suspension processing", operation is not guaranteed for any register access other than read access to the LSI status register.

*4: It is also possible to change the MPEG-4 encoding parameters.

3.5 Exception Processing

Table 3-11 lists the exception statuses that this LSI can enter

Table 3-11 Causes of Occurrence of Exceptions

Type	Description	Countermeasure
Capture error	Indicates that the input image is abnormal. If this exception occurs, the frame rate deteriorates.	Check if there is any abnormality in the input image caused by cable disconnection, noise, etc.
Stream data read abnormality	Too much time taken for read processing an abnormality occurred during stream data read by the host CPU. If this exception occurs, the frame rate deteriorates.	Check the stream data read processing.
Set bit rate exceeded	This exception occurs when during CBR the amount of image data to be encoded is too much with respect to the set bit rate. If this exception occurs, the frame rate deteriorates.	Check the combination of use cases. Increase the bit rate or select standard or high compression for the picture quality setting.
Encoding abnormality	Indicates that data could not be encoded normally.	Perform a soft reset.

4. External Interface

4.1 Reset

This LSI has the following three types of reset functions.

Table 4-1 Rest Functions

Reset function	Description	Range of reset	Reset period	Period during which register access is disabled
(1) Hard reset (at Power ON)	Caused by asserting the reset pin at LSI Power On.	Entire LSI (*1)	11 ms (min.)	During reset, or a period of 100 ns after the reset pin assert is released
(2) Hard reset (during LSI operation)	Caused by asserting the reset pin during LSI operation.	Entire LSI (*1)	11 ms (min.)	During reset, or a period of 100 ns after the reset pin assert is released
(3) Soft reset (during LSI operation)	Caused by writing "1" to the softrst bit of the LSI status register during LSI operation.	Entire LSI (*1)	200 ns	A period of 500 ns after a "1" is written to the softrst bit

*1: All the values set in the registers are initialized. Contents of stream data (contents of SDRAM) are not guaranteed.

4.2 Video Interface

4.2.1 VSYNC/HSYNC Mode

4.2.1.1 VSYNC/HSYNC Mode (VSYNC Level Mode)

Timing in the vertical direction

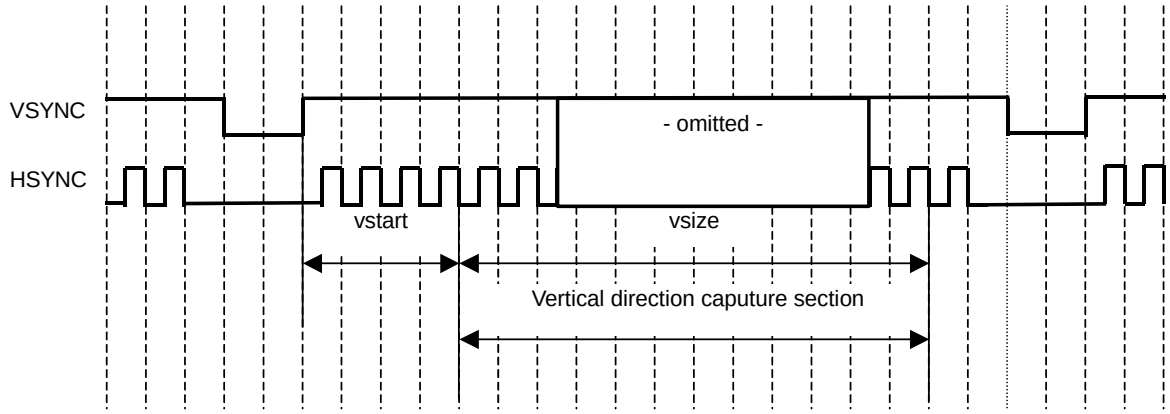


Figure 4-1 Timing in the Vertical Direction in VSYNC Level Mode

* Specify the line count for vstart and vsize.
* vstart is determined by the vstart parameter. vsize is determined by the InImage parameter.

InImage	vsize
1: VGA (640x480) progressive	1: 480
2: PAL (720x576) interlaced	2: 576
3: NTSC (720x480) interlaced	3: 480
6: QVGA (320x240) progressive	6: 240

(Setting InImage to 2:PAL or 3:NTSC is not allowed in VSYNC/HSYNC mode.)

Timing in the horizontal direction

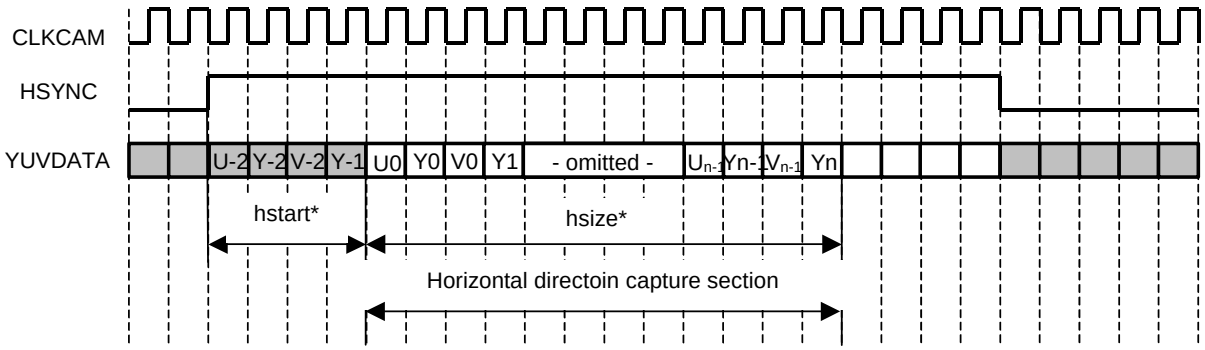


Figure 4-2 Timing in the Horizontal Direction in VSYNC Level Mode

* Specify the pixel count for hstart and hsize.
* hstart is determined by the hstart parameter. hsize is determined by the InImage parameter.

InImage	hsize
1: VGA (640x480) progressive	1: 640
2: PAL (720x576) interlaced	2: 720
3: NTSC (720x480) interlaced	3: 720
6: QVGA (320x240) progressive	6: 320

(Setting InImage to 2:PAL or 3:NTSC is not allowed in VSYNC/HSYNC mode.)

* Use the clkcamedge parameter to determine the edge at which the YUVDATA, HSYNC, VSYNC, and FIELDTOP signals are loaded.
- Will be latched at a negative edge of CLKCAM (clkcamedge = 0)
- Will be latched at a positive edge of CLKCAM (clkcamedge = 1)

4.2.1.2 VSYNC/HSYNC Mode (VSYNC Edge Mode)

Timing in the vertical direction

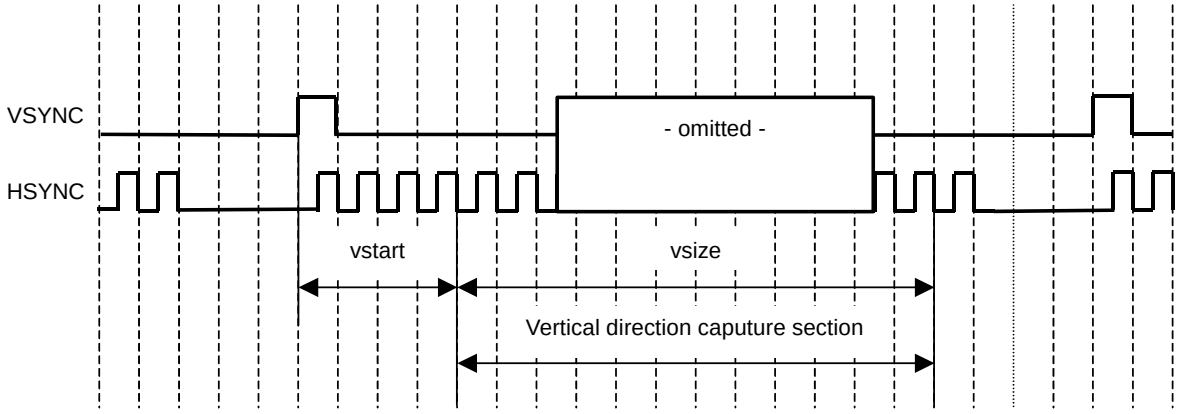


Figure4-3 Timing in the Vertical Direction in VSYNC Edge Mode

* Specify the line count for vstart and vsize.
* vstart is determined by the vstart parameter. vsize is determined by the InImage parameter.

InImage	vsize
1: VGA (640x480) progressive	1: 480
2: PAL (720x576) interlaced	2: 576
3: NTSC (720x480) interlaced	3: 480
6: QVGA (320x240) progressive	6: 240

(Setting InImage to 2:PAL or 3:NTSC is not allowed in VSYNC/HSYNC mode.)

Timing in the horizontal direction

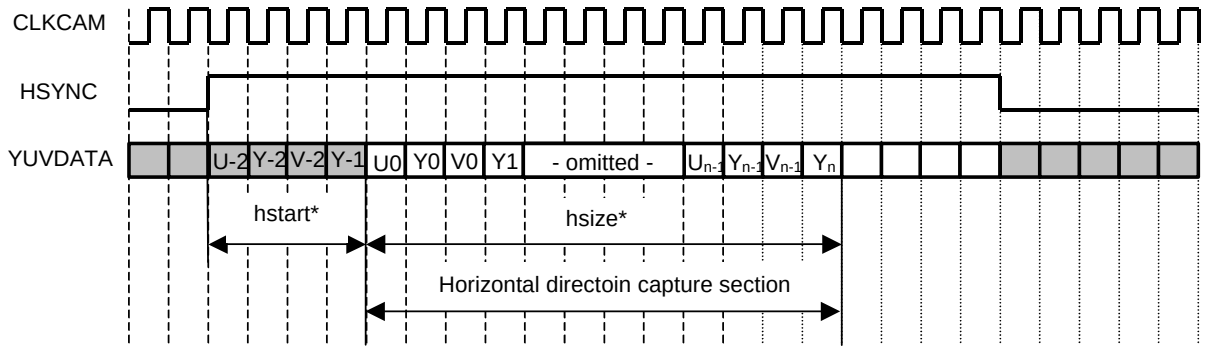


Figure 4-4 Timing in the Horizontal Direction in VSYNC Edge Mode

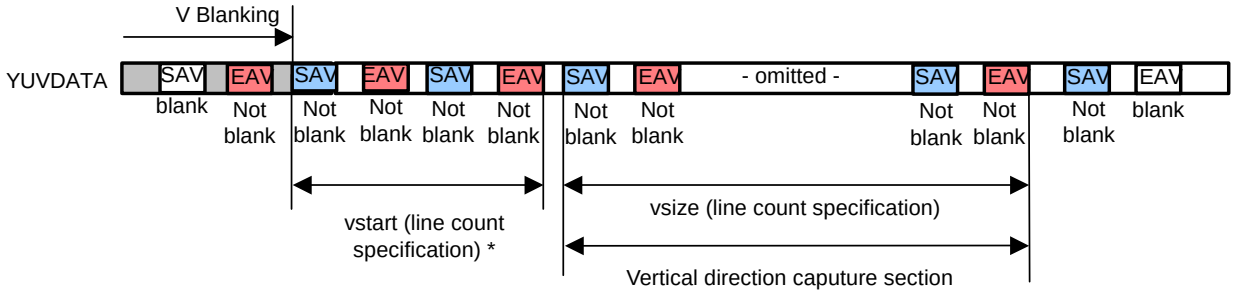
* Specify the pixel count for hstart and hsize.
* hstart is determined by the hstart parameter. hsize is determined by the InImage parameter.

InImage	hsize
1: VGA (640x480) progressive	1: 640
2: PAL (720x576) interlaced	2: 720
3: NTSC (720x480) interlaced	3: 720
6: QVGA (320x240) progressive	6: 320

* Use the clkcamedge parameter to determine the edge at which the YUVDATA, HSYNC, VSYNC, and FIELDTOP signals are loaded.
- Will be latched at a negative edge of CLKCAM (clkcamedge = 0)
- Will be latched at a positive edge of CLKCAM (clkcamedge = 1)

4.2.2 ITU-R BT.656 (SAV/EAV) Mode

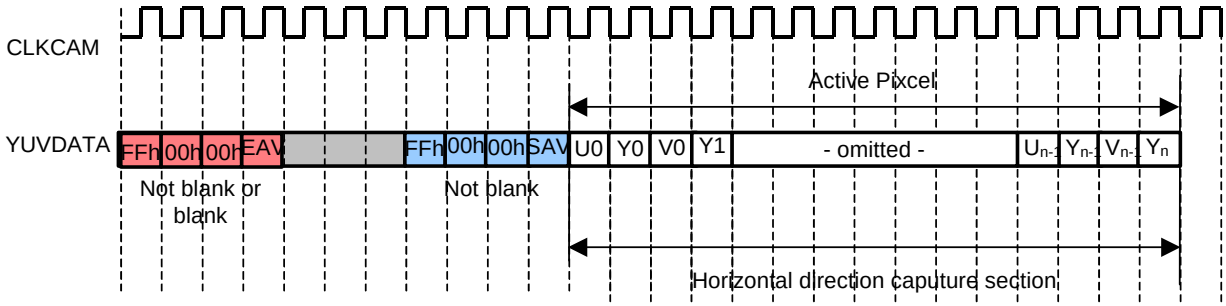
- For input, conform to the ITU-R BT.656 standard.
  Timing in the vertical direction



* Images are not captured in the period from the start of the Active Line till SAVs of the line count specified in the vertical direction capture starting position are counted (vstart) .

Figure 4-5 Timing in the Vertical Direction in SAV/EAV Mode

Timing in the horizontal direction



* Set the horizontal direction capture starting position (hstart) to 0. Specify the predefined value for the horizontal direction capture section (hsize) according to the input image size.

Figure 4-6 Timing in the Horizontal Direction SAV/EAV Mode

* Use the clkcamedge parameter to determine the edge at which the YUVDATA signal is loaded.
- Will be latched at a negative edge of CLKCAM (clkcamedge = 0)
- Will be latched at a positive edge of CLKCAM (clkcamedge = 1)

In SAV/EAV mode, the synchronous signal information (SAV/EAV) incorporated in image data is judged without using the vertical sync signal VSYNC and horizontal sync signal HSYNC and image data in the valid section is loaded.

The values in the table below are used to judge SAV/EAV.

Table 4-2 SAV/EAV Codes

Word	YDATAI0-7								
	7	6	5	4	3	2	1	0	F=0: During Top field
First	1	1	1	1	1	1	1	1	F=1: During Bottom field
Second	0	0	0	0	0	0	0	0	V=0: Elsewhere
Third	0	0	0	0	0	0	0	0	V=1: During field blanking
Fourth	1	F	V	H	P3	P2	P1	P0	H=0: SAV H=1: EAV

The relationship between the F,V, and H bits in the Fourth Word and the protection bits (P3, P2, P1, P0) of SAV/EAV is shown below.

Table 4-3 Protection Bit Assignment

F	V	H	P3	P2	P1	P0	Description
0	0	0	0	0	0	0	SAV (during top field, elsewhere field blanking)
0	0	1	1	1	0	1	EAV (during top field, elsewhere field blanking)
0	1	0	1	0	1	1	SAV (during top field, during blanking)
0	1	1	0	1	1	0	EAV (during top field, during field blanking)
1	0	0	0	1	1	1	SAV (during bottom field, elsewhere field blanking)
1	0	1	1	0	1	0	EAV (during bottom field, elsewhere field blanking)
1	1	0	1	1	0	0	SAV (during bottom field, during field blanking)
1	1	1	0	0	0	1	EAV (during bottom field, during field blanking)

4.2.3 Capture Area Detection Conditions

Basic capture processing captures all the image data in the section where the horizontal sync signal (HSYNC) is at a "High" level. A capture area can be selected using the following registers (parameters):

- VSTART(vstart[7:0]) : Set the vertical direction capture start position
- HSTART(hstart[9:0]) : Set the horizontal direction capture start position

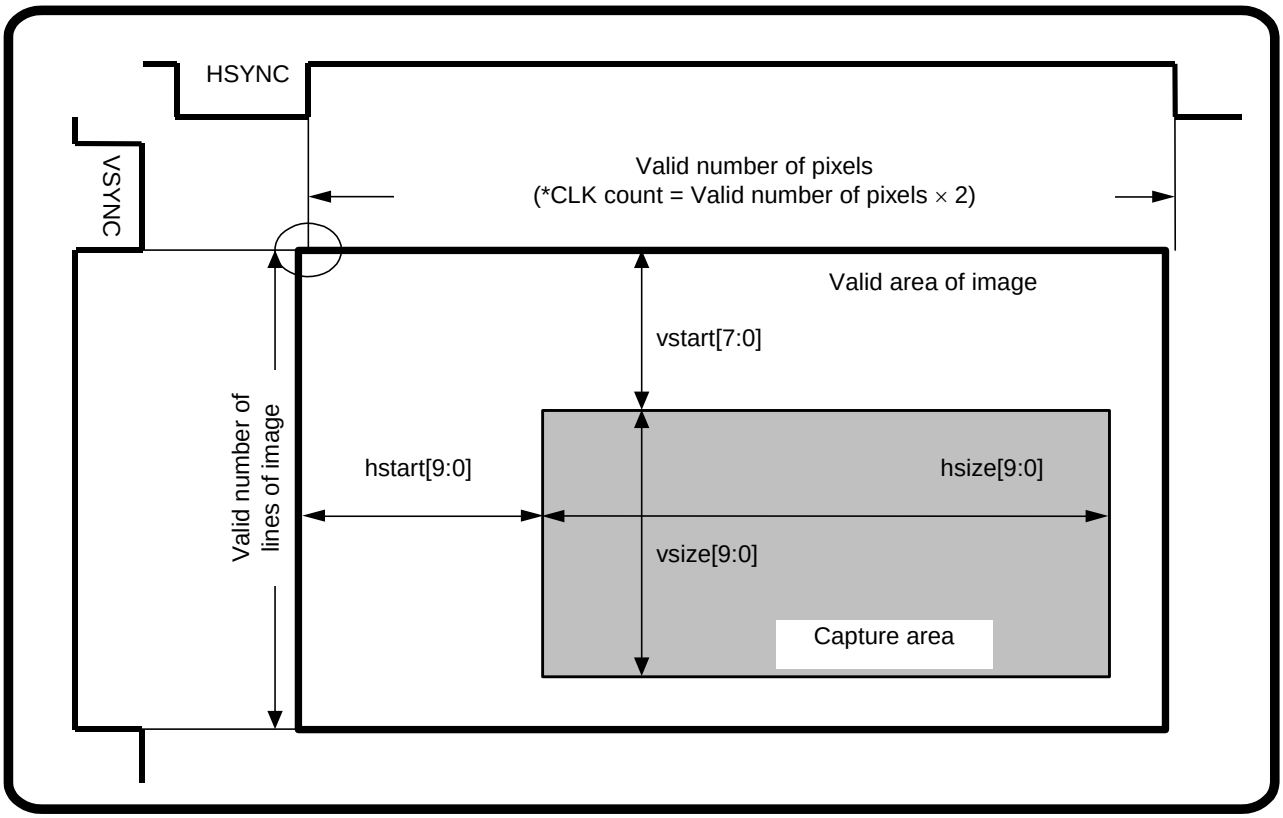


Figure 4-7 Capture Area Detection Conditions

< Capture Area Setting Constraint >

[Constraint 1] Set a multiple of 2 in HSTART,
[Constraint 2] In SAV/EAV mode, set "0" in HSTART.
[Constraint 3] In Interlaced mode, set a multiple of 2 in VSTART.

4.2.4 Vertical Direction Capture Area Detection Specification

Progressive

Captures as many lines as the number of vertical lines specified in the INIMAGE register from the vertical direction capture starting line specified in the VSTART register.

Interlaced

Captures the half of the number of vertical lines specified in the INIMAGE register for each of the top field and bottom field.

4.2.5 Capture Start Conditions

Capture starts from the frame following the frame where the enable parameter of the LSI status register is set to High. (Capture does not start from the middle of the frame even if the enable parameter is set to High in the middle of the frame.)

4.2.6 Illegal Operations

4.2.6.1 VSYNC/ HSYNC Mode (When in VSYNC Level Mode)

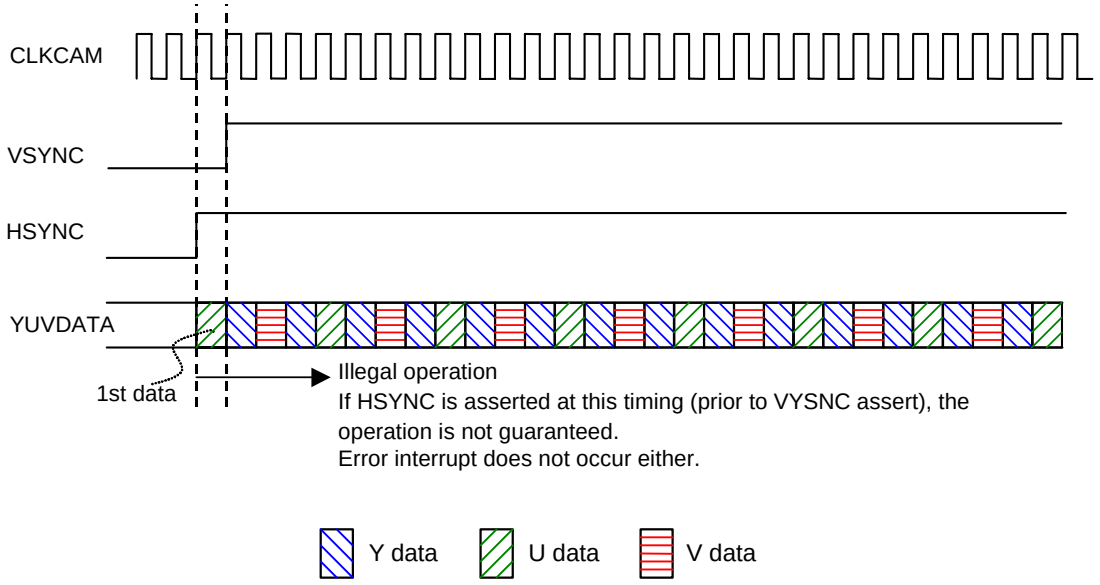


Figure 4-8 Illegal Operation 1 in VSYNC Level Mode

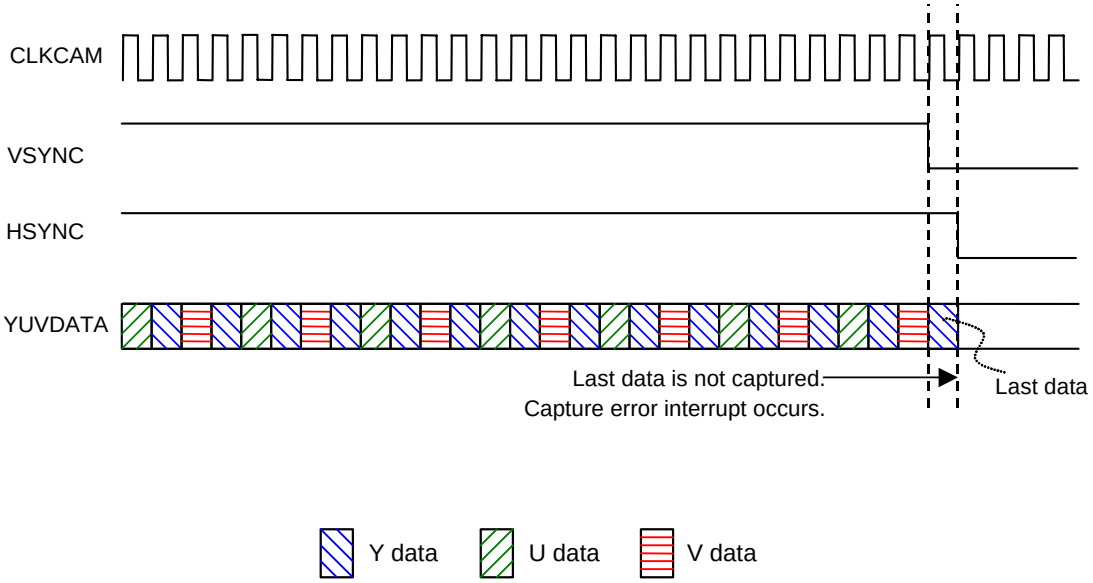


Figure 4-9 Illegal Operation 2 in VSYNC Level Mode

4.2.6.2 VSYNC/ HSYNC Mode (When in VSYNC Edge Mode)

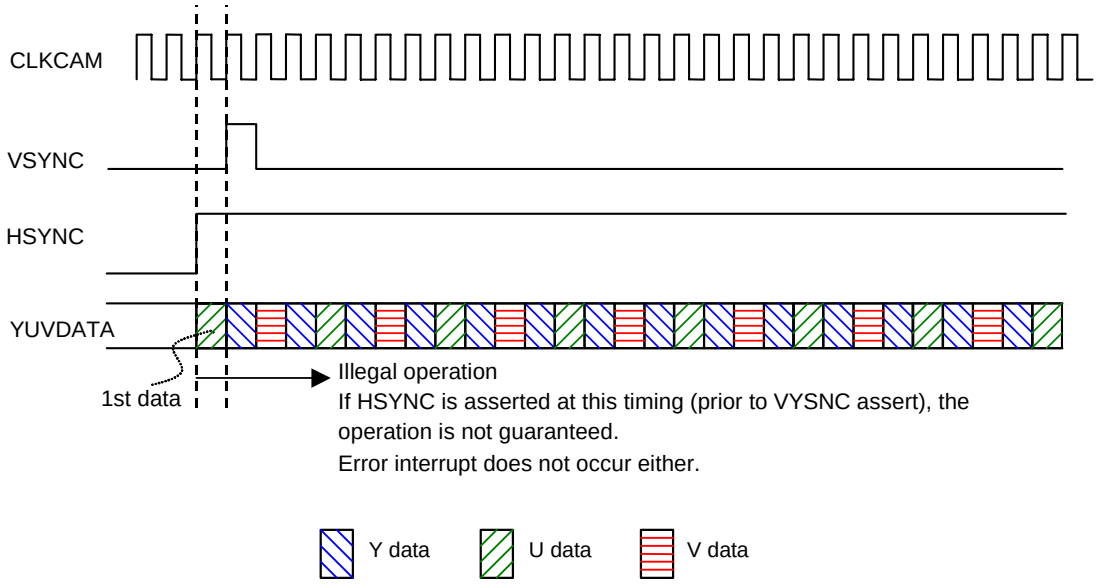
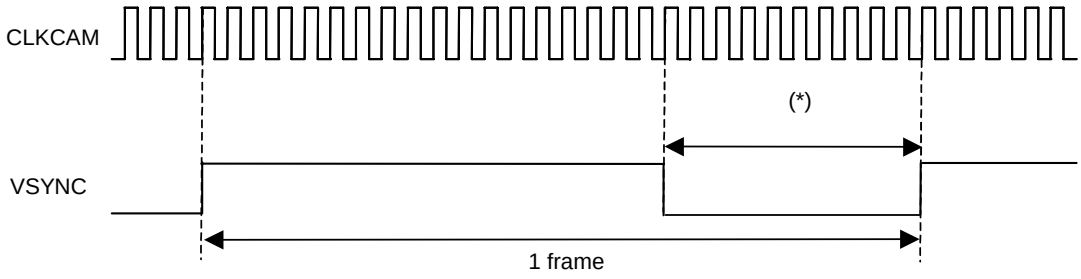


Figure 4-10 Illegal Operation 1 in VSYNC Edge Mode

4.2.7 VSYNC/ HSYNC Signal Timing Constraint

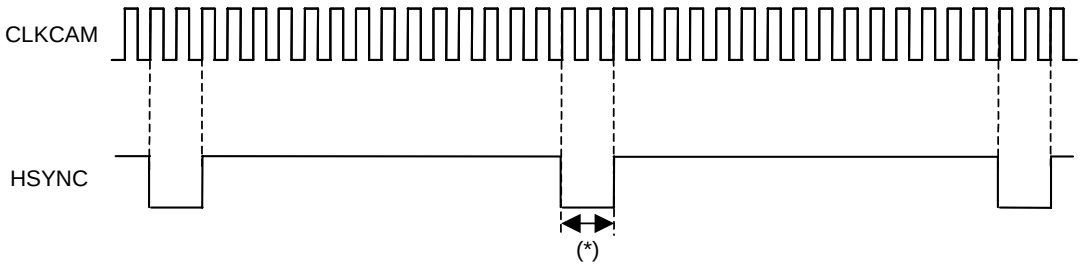
4.2.7.1 VSYNC/ HSYNC Signal Timing Constraint (When in VSYNC Level Mode (Active-High))

Timing in the vertical direction



(*) At least 10 CLKCAM cycles are required to negate VSYNC.

Timing in the horizontal direction

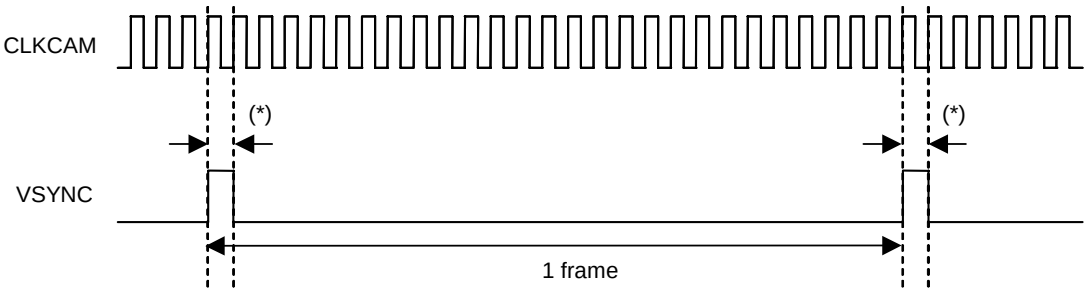


(*) At least 2 CLKCAM cycles are required to negate HSYNC.

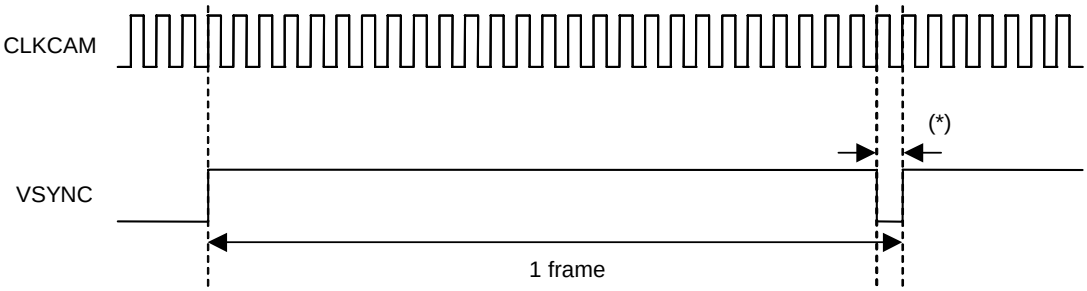
Figure 4-11 Timing Constraint in VSYNC Level Mode

4.2.7.2 VSYNC/ HSYNC Signal Timing Constraint (When in VSYNC Edge Mode (Active-High))

Timing in the vertical direction

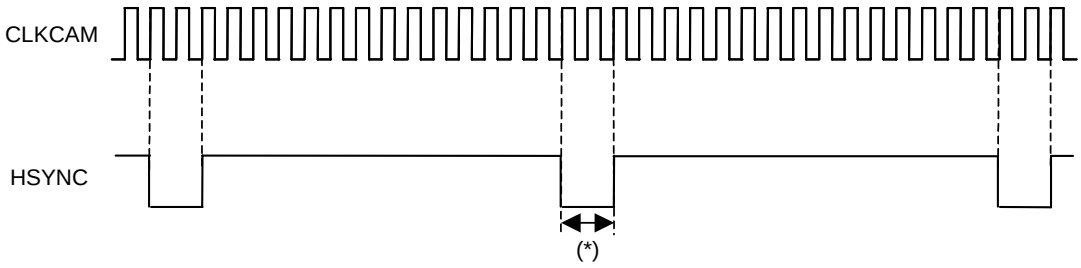


(*) At least 1 CLKCAM cycle is required to assert VSYNC.



(*) At least 1 CLKCAM cycle is required to negate VSYNC.

Timing in the horizontal direction



(*) At least 2 CLKCAM cycles are required to negate HSYNC.

Figure 4-12 Timing Constraint in VSYNC Edge Mode

4.2.8 Image Data Format

Table 4-4 shows the image data format (YUV image data).

Table 4-4 YUV 4:2:2 8-Bit Format

Signal	Pixel Byte Sequence							
YUVDATA 7	U7	Y7	V7	Y7	U7	Y7	V7	Y7
YUVDATA 6	U6	Y6	V6	Y6	U6	Y6	V6	Y6
YUVDATA 5	U5	Y5	V5	Y5	U5	Y5	V5	Y5
YUVDATA 4	U4	Y4	V4	Y4	U4	Y4	V4	Y4
YUVDATA 3	U3	Y3	V3	Y3	U3	Y3	V3	Y3
YUVDATA 2	U2	Y2	V2	Y2	U2	Y2	V2	Y2
YUVDATA 1	U1	Y1	V1	Y1	U1	Y1	V1	Y1
YUVDATA 0	U0	Y0	V0	Y0	U0	Y0	V0	Y0
Y Data FRAME	0		1		2		3	
U,V Data FRAME	0 1				2 3			

4.2.9 Connection Examples

4.2.9.1 Connection in VSYNC/HSYNC Mode (with Camera Modules etc.)

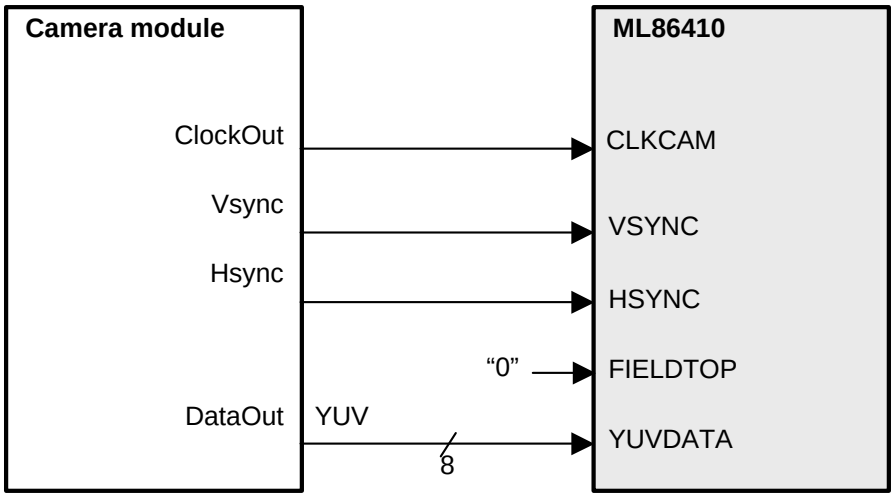


Figure 4-13 Connection in VSYNC/HSYNC Mode (with Camera Modules etc.)

4.2.9.2 Connection in BT.656 Mode (with Digital Video Decoder etc.)

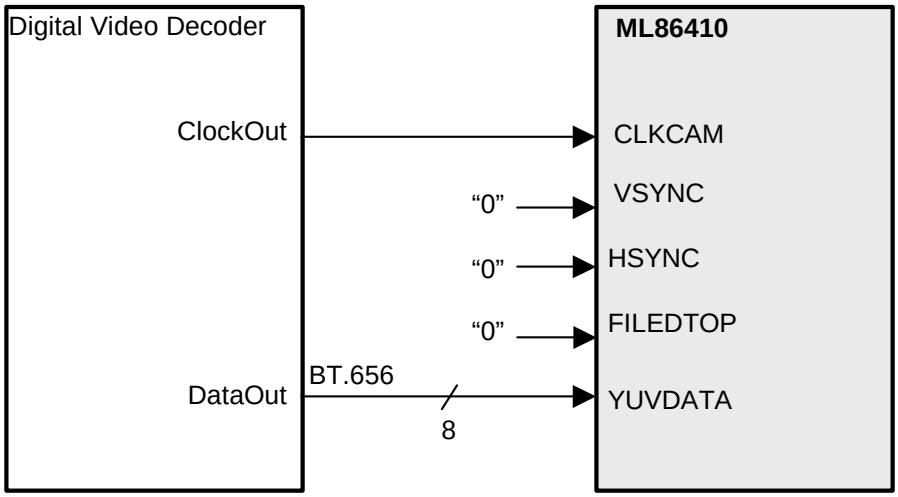


Figure 4-14 Connection in BT.656 Mode (with Digital Video Decoder etc.)

4.3 Host CPU Interface

This LSI can be connected to a general-purpose host CPU having an 8-/16-bit data bus. The LSI can operate as an I/O device from the host CPU.

Figures 4-15 to 4-17 show examples of connecting host CPUs.

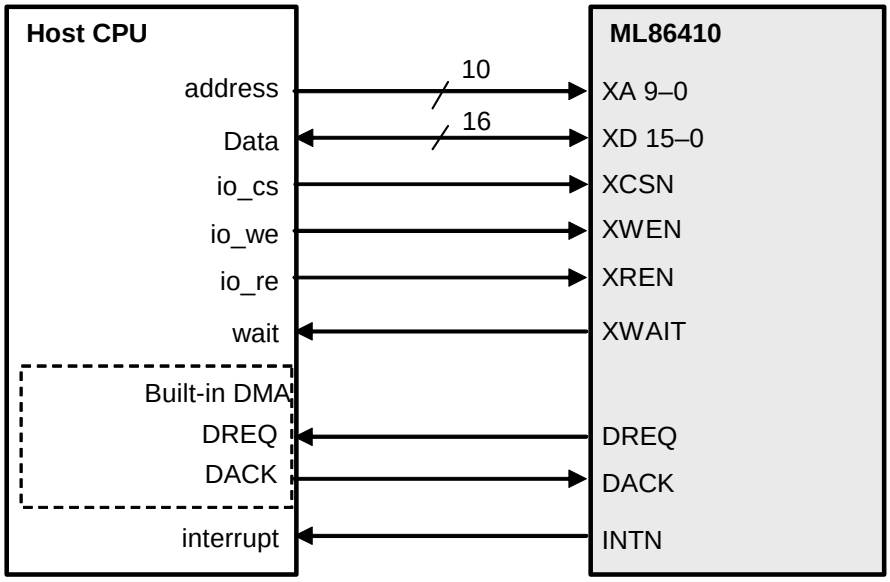


Figure 4-15 Host CPU Connection Example (Built-in DMA Used)

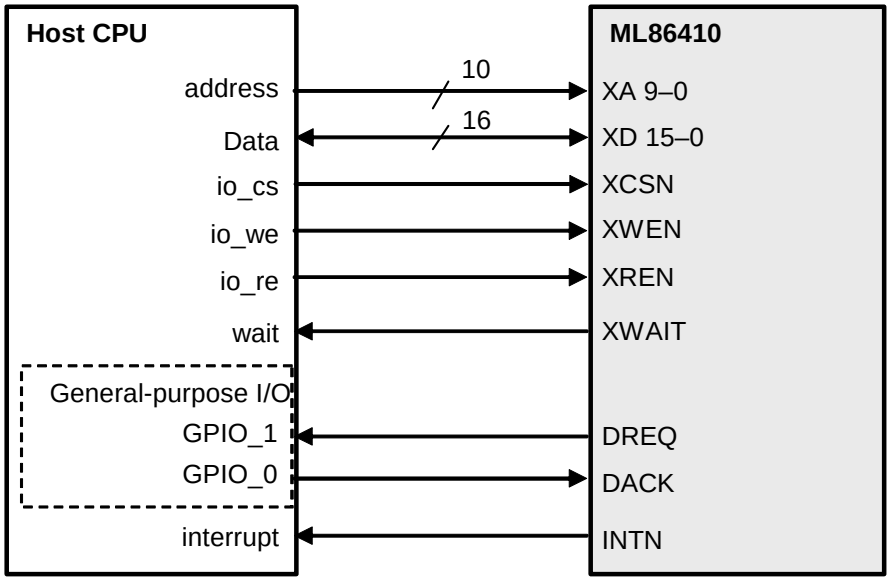


Figure 4-16 Host CPU Connection Example (General-Purpose I/O Used)

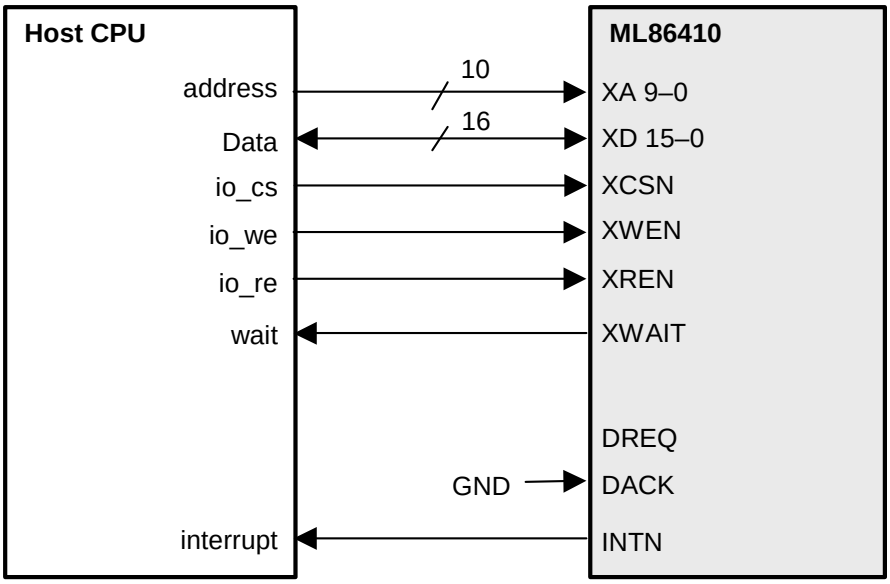


Figure 4-17 Host CPU Connection Example (DMA Signal Control Register Used)

Note:
For XA and XD, XA0 and XD0 are LSBs (last significant bits).

4.4 External SDRAM Interface

Table 4-5 shows the types of SDRAM that are supported by this LSI and Table 4-6 shows the outline of the SDRAM control functions.
This LSI automatically executes the SDRAM initialization sequence after reset assert (both soft reset and hard reset).

Table4-5 Supported SDRAM Types

Operating frequency [MHz]	SDRAM				
	PC133	PC125	PC100	PC83	PC66
81.0	○	○	○	×	×

○ : Supported × : Not supported

Note : The input setup time(t_{SI}) should be 1.5nsec or less.

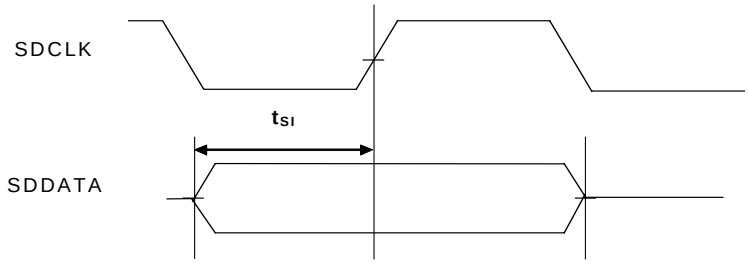


Table 4-6 Outline of SDRAM Control Functions

Item	Description	
Capacity of DRAM that enables connection	2 MWords x 32 bits (8 Mbytes)(minimum configuration)	
Control	Address: output	RAS/CAS addresses are output in multiplex mode. Supports column lengths of 8 to 10 bits.
DRAM initialization	The initialization sequence is automatically executed by this LSI.	

Figure 4-18 shows an example of external SDRAM connection.

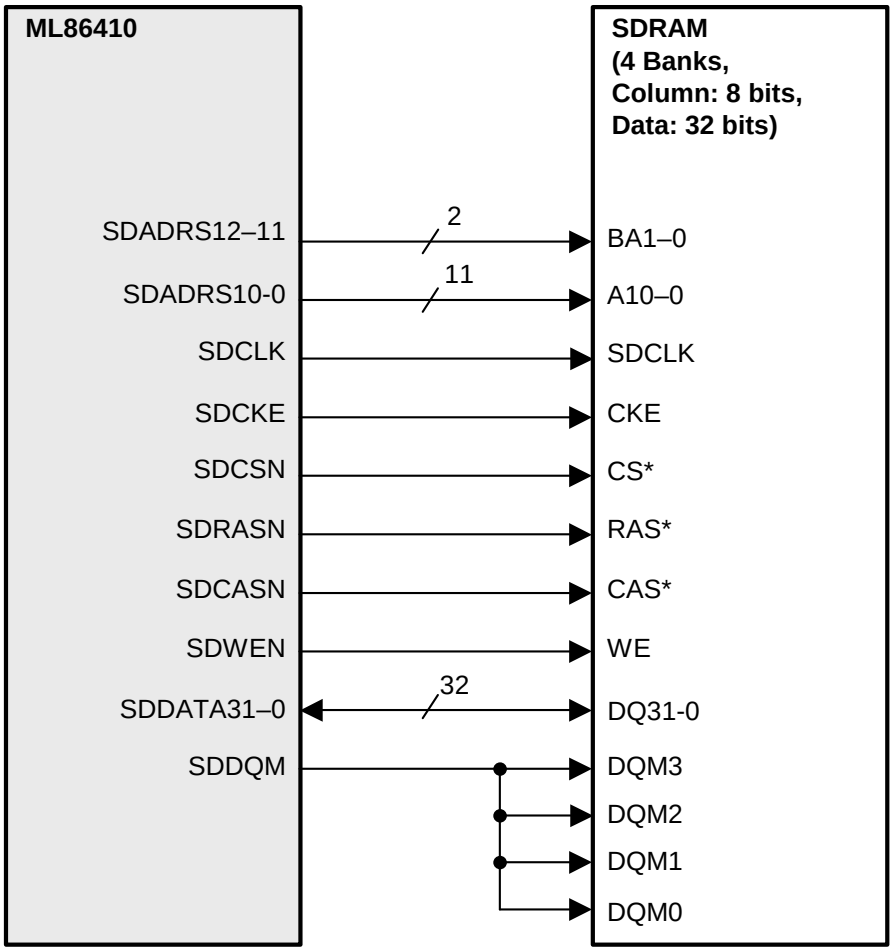


Figure 4-18 Example of External SDRAM Connection

4.5 Example of External Oscillator Connection

Figure 4-19 shows an example of external Oscillator connection.

NOTE : Since the value of Rf/Rd/Cg/Cd is influenced by the parasitic capacitance of the board, adjustment is necessary for each product.

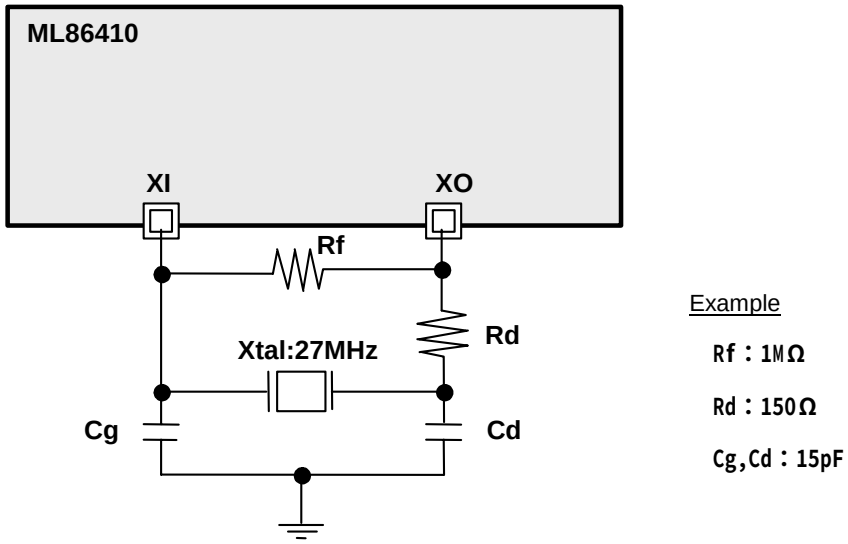


Figure 4-19 Example of External Oscillator Connection

4.6 Example of Board Layout

Figure 1-6 shows an example of components that composes a system that use the ML86410. The figure also shows a layout example of the components on a board.

List of components (example)

- ML86410
  Package: 144-pin LQFP
- Digital video decoder
  OKI ML86V7668
  Package: 100-pin TQFP
- ARM-equipped microcontroller (host CPU)
  ML69Q6500
  Package: 272-pin LFBGA
- SDRAM for ML86410
  Oki MD56V62320K-6TA1G3A (64-Mbit)

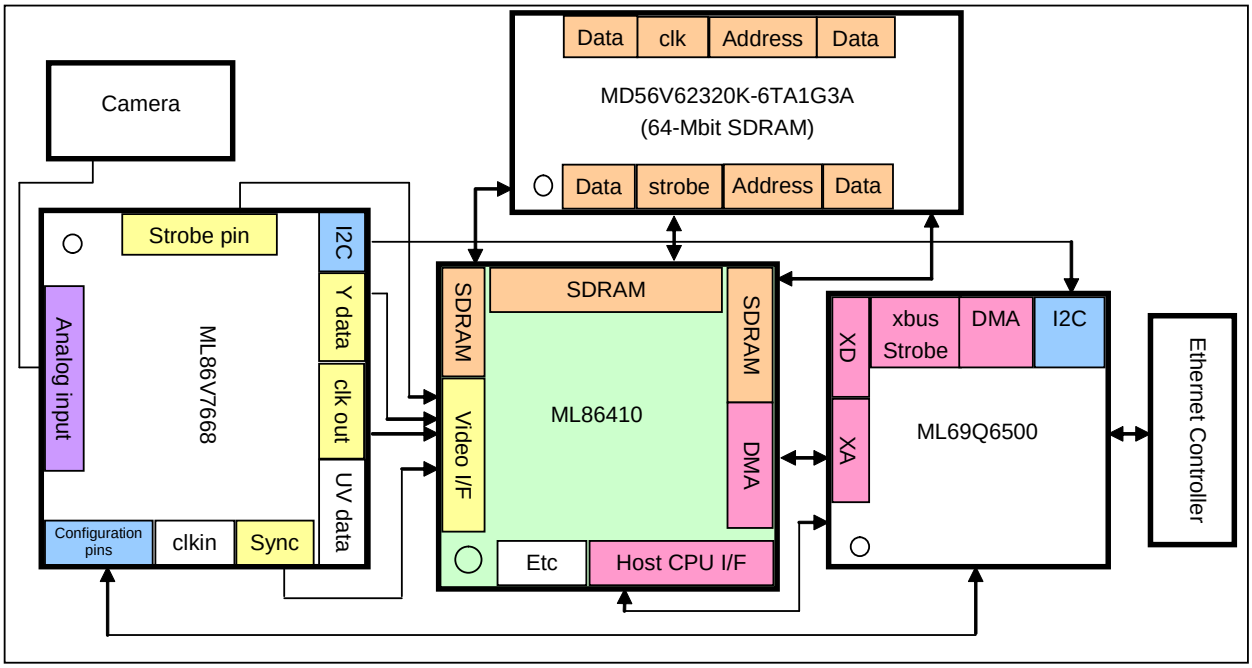


Figure 4-20 Layout Example of System Components

5. Electrical Specifications (Preliminary)

5.1 Absolute Maximum Ratings

Table 5-1 shows the absolute maximum ratings.

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage (CORE)	V_{DDCORE}	– (*1)	–0.3 to +2.0	V
Digital power supply voltage (I/O)	V_{DDIO}	– (*1)	–0.3 to +4.6	
PLL power supply voltage	V_{DDPLL}	– (*1)	–0.3 to +2.0	
Input voltage (normal buffer)	V_I	– (*1)	–0.3 to V_{DDIO}+0.3	
Output voltage (normal buffer)	V_O	– (*1)	–0.3 to V_{DDIO}+0.3	
Allowable input current	I_I	– (*1)	–10 to +10	mA
Allowable output current (2 mA buffer)	I_O	– (*1)	–8 to +8	
Allowable output current (4 mA buffer)			–16 to +16	
Allowable output current (6 mA buffer)			–24 to +24	
Power dissipation	P_D	Ta = 85°C	1450	mW
Storage temperature	T_{STG}	—	–50 to +150	°C

*1: The GND pins are at 0 V when Ta = 25°C

5.2 Recommended Operating Conditions

Table 5-2 shows the recommended operating conditions.

Table 5-2 Recommended Operating Conditions

(GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital power supply voltage (CORE)	V_{DDCORE}	$V_{DDIO} \geq V_{DDCORE}$	1.35	1.5	1.65	V
Digital power supply voltage (I/O)	V_{DDIO}		3.0	3.3	3.6	
PLL power supply voltage	V_{DDPLL}		1.35	1.5	1.65	
Operating frequency	f_{OP}		—	—	81	MHz
Ambient temperature	Ta	—	-20	25	85	°C

5.2.1 Power-On and Power-Off

5.2.1.1 Restrictions on Power-On /Power-Off Procedures

Power-on : Turn on the 1.5 V power supply (CORE) → Turn on the 3.3 V power supply (IO) → Turn on the 1.5 V power supply (PLL)
Power-off : Turn off the 1.5 V power supply (PLL) → Turn off the 3.3 V power supply (IO) → Turn off the 1.5 V power supply (CORE)

5.3 DC Characteristics

Table 5-3 DC Characteristics

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input "H" voltage (normal pins)	V_{IH1}	Applied to normal pins	2.0	—	V_{DDIO}+0.3	V
Input "L" voltage (normal pins)	V_{IL1}	Applied to normal pins	–0.3	—	0.8	
TTL level Schmitt trigger input threshold voltage	V_{T+}	—	—	—	2.1	
	V_{T-}		0.7	—	—	
	ΔV_T	V_{T+} — V_{T-}	0.25	—	—	
Output "H" voltage	V_{OH1}	V_{DDIO} = 3.0 to 3.6 V Applied to normal pins	2.4	—	—	
Output "L" voltage	V_{OL1}	V_{DDIO} = 3.0 to 3.6 V Applied to normal pins	—	—	0.4	
Input leakage current 1	I_{IL1}	V_I = 0V / V_{DDIO} Applied to normal pins	–10	—	10	μA
Input leakage current 2	I_{IL2}	V_I = 0 V Applied to pins pulled up with 50 kΩ	–200	—	-10	
Input leakage current 3	I_{IL3}	V_I = V_{DDIO} Applied to pins pulled down with 50 kΩ	10	—	200	
Input pin capacitance	C_I	—	—	5	—	pF
Output pin capacitance	C_O	—	—	5	—	
Input/output pin capacitance	C_{IO}	—	—	5	—	
Chip power consumption (operating)	P_{Total}	VDDCORE = 1.5 V, VDDIO = 3.3 V, Ta = 25°C	—	250	—	mW
IO supply current (operating)	I_{DDOIO}		—	30	—	mA
Core and PLL supply current (operating)	$I_{DDOCore}$		—	100	—	mA
IO Supply current (standby)	I_{DDSIO}	VDDCORE = 1.5 V, VDDIO = 3.3 V, Ta = 25°C	—	1	—	uA
Core and PLL Supply current (standby)	$I_{DDSCore}$		—	2	—	mA

5.4 AC Characteristics

Note: In the AC characteristics timing diagrams shown in this section, the intervals are measured at the 1/2 V_{DDIO} on the input and output waveforms.

5.4.1 Reset Timing

Table 5-4 Reset Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset pulse width	t_{RSTW}	—	11	—	—	ms

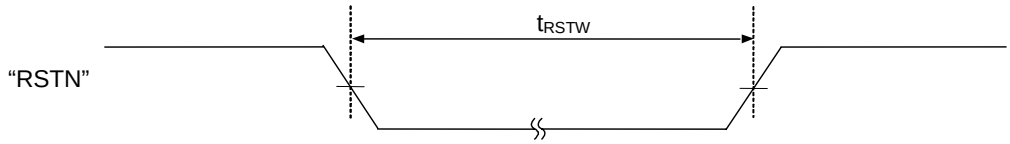


Figure 5-1 Reset Timing

5.4.2 Clock Timing (XI, XO)

Table 5-5 Clock Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta =-20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock (CLK) frequency	f_{CLK}	—	—	27.0	—	MHz
Clock (CLK) cycle	t_{CLK}	—	—	$1/f_{CLK}$	—	s

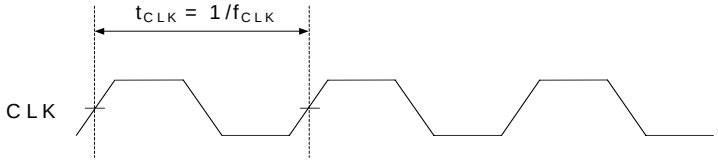


Figure 5-2 Clock Timing

5.4.3 External SDRAM Timing

Table 5-6 External SDRAM Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

SDRAM							
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
SDCLK cycle	t_{SDC}	CL = 20 pF	—	t_{CLK} / 3	—	ns	(81 MHz)
CS output delay time	t_{SDCSD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
DQM output delay time	t_{SDDQMD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
RAS output delay time	t_{SDRASD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
CAS output delay time	t_{SDRASD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
WE output delay time	t_{SDWED}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
SDADRS[12:0] output delay time	t_{SDXAD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
SDDATA[31:0] output delay time	t_{SDXDOD}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
SDDATA[31:0] output hold time	t_{SDXDOH}		$0.5t_{SDC}$ – 3.0	—	—		
SDDATA[31:0] output enable time	t_{SDXDOE}		$0.5t_{SDC}$ – 3.0	—	$0.5t_{SDC}$ + 4.5		
SDDATA[31:0] output disable time	$t_{SDXDODE}$		$0.5t_{SDC}$ – 3.0	—	—		
SDDATA[31:0] input setup time	t_{SDXDIS}		2	—	—		
SDDATA[31:0] input hold time	t_{SDXDIH}		4.5	—	—		
Minimum delay time, RAS to CAS	t_{SDRCD}	—	n_{SD1} x t_{SDC}	—	—		n_{SD1} = tRCD=2
RAS active time	t_{SDRAS}		n_{SD2} x t_{SDC}	—	—		n_{SD2} = tRAS=5
RAS precharge time	t_{SDRP}		n_{SD3} x t_{SDC}	—	—		n_{SD3}= tRP=2

Note : tCLK =1/ fCLK (fCLK=27MHz)

5.4.3.1 External SDRAM Read Timing

(32-bit bus width SDRAM word access)

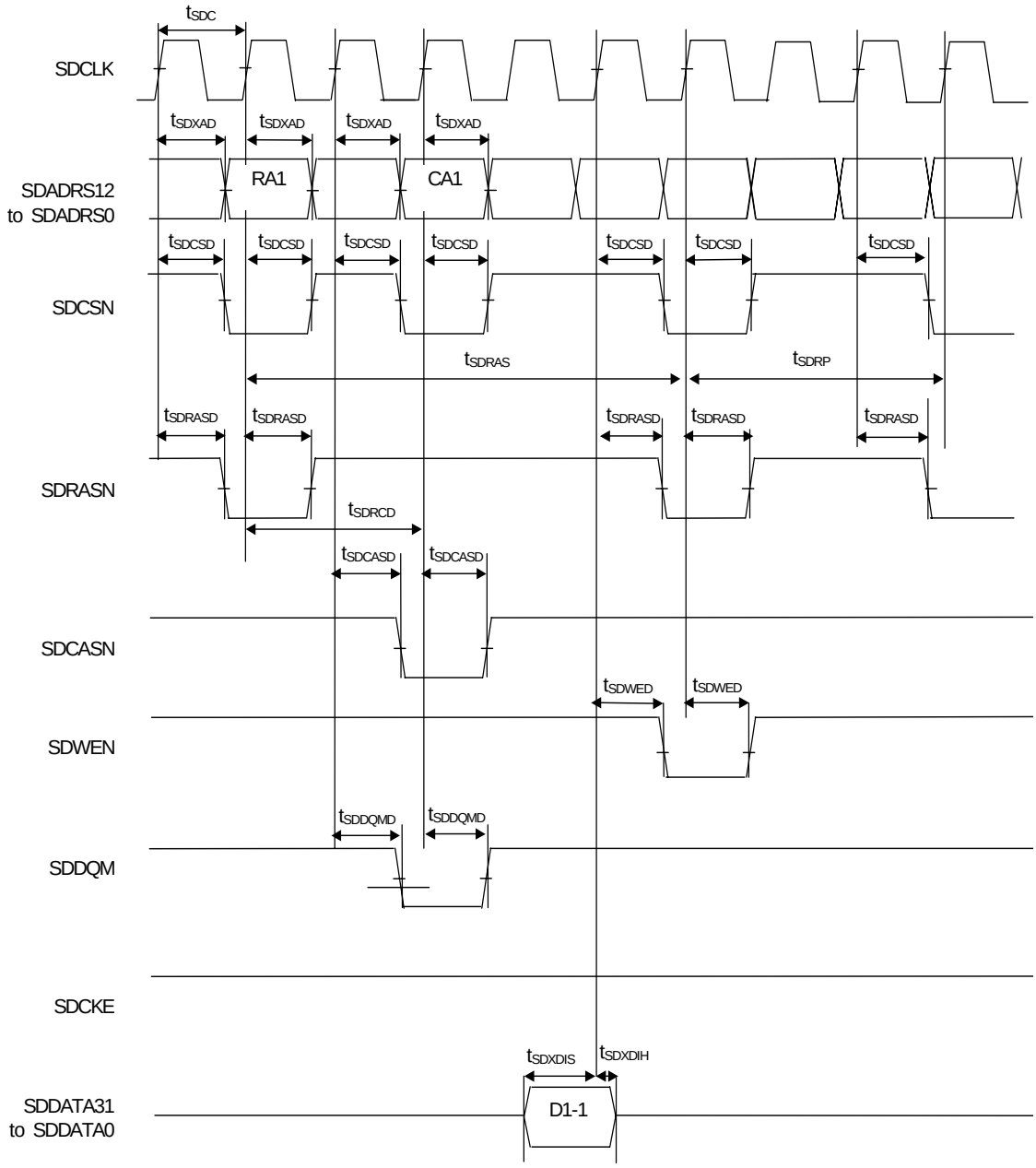


Figure 5-3 External SDRAM Read Timing

5.4.3.2 External SDRAM Write Timing

(32-bit bus width SDRAM byte/half-word access)

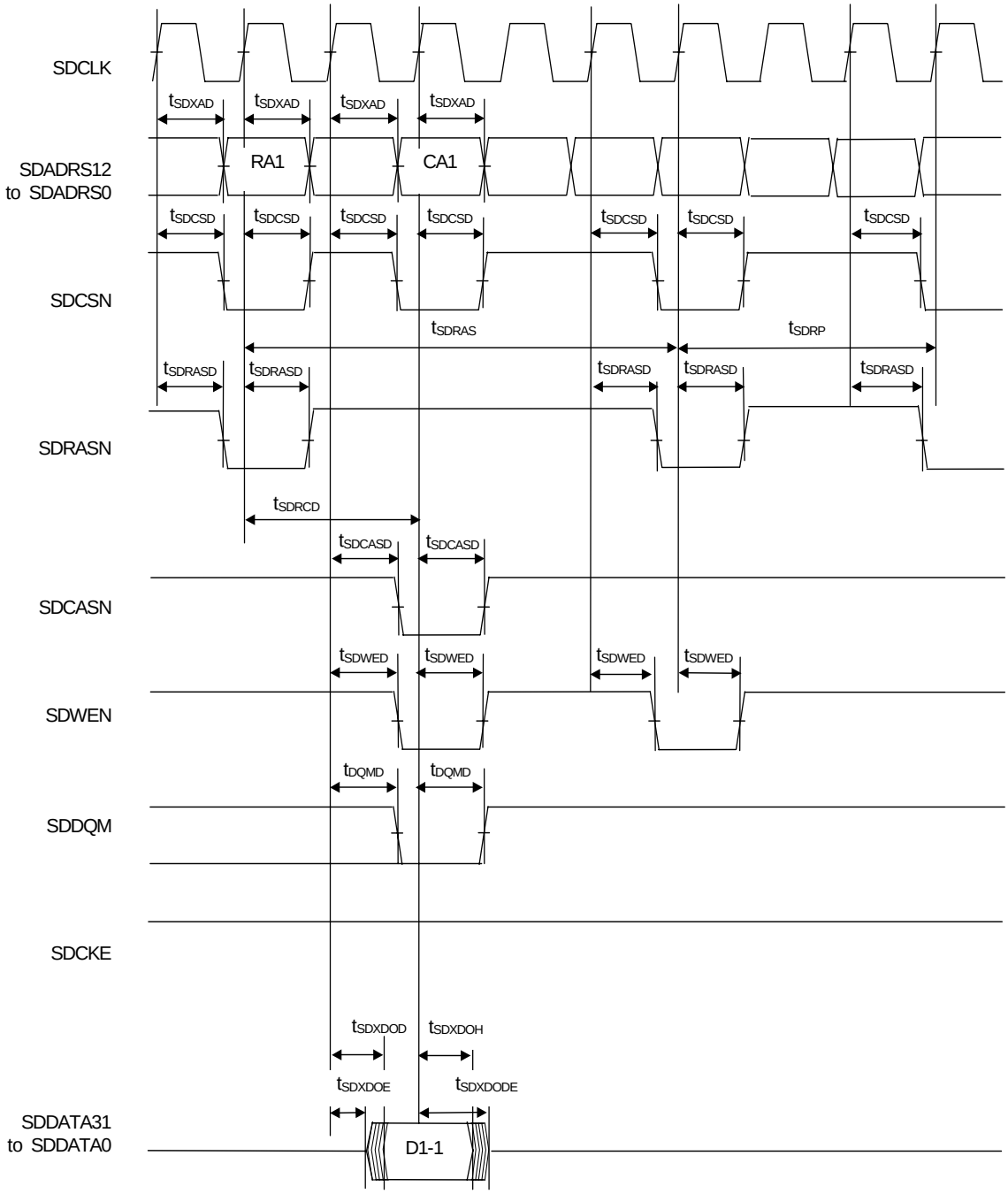


Figure 5-4 External SDRAM Write Timing

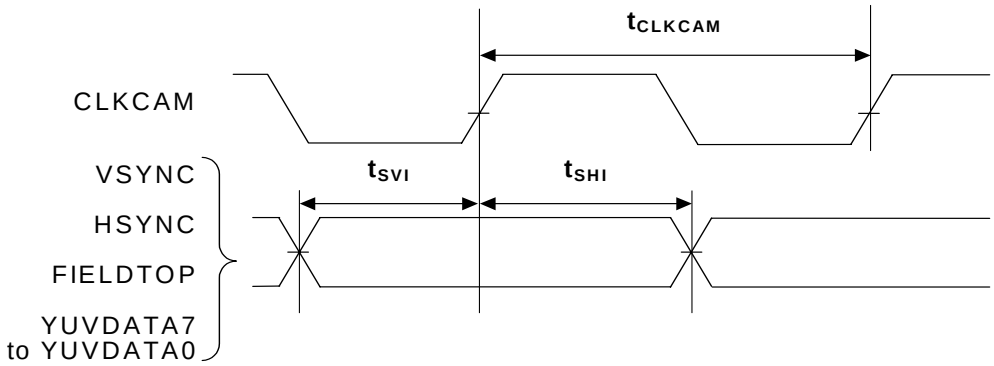
5.4.4 Video Interface Timing

Table 5-7 Video Interface Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
CLKCAM frequency	f_{CLKCAM}	CL = 20 pF	—	27	—	MHz	
CLKCAM cycle	t_{CLKCAM}		—	$1/f_{CLKCAM}$	—	s	
CLKCAM input setup time	t_{SVI}		10	—	—	ns	
CLKCAM input hold time	t_{HVI}		5	—	—		

Capture clock edge setting: Positive



Capture clock edge setting: Negative

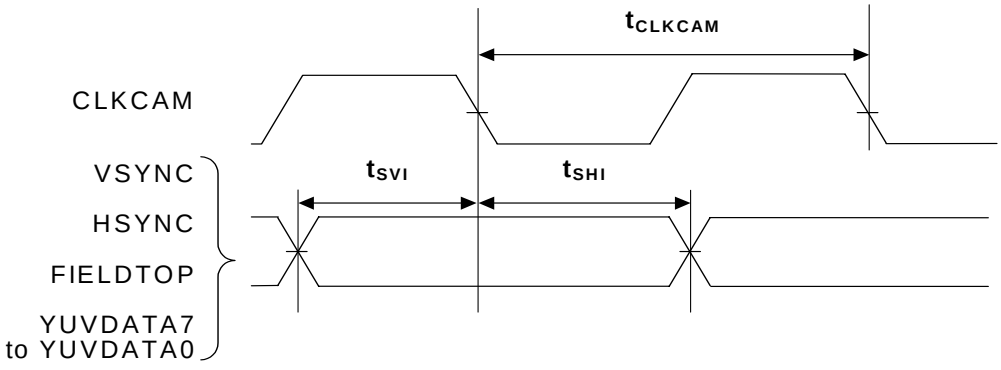


Figure 5-5 Video Interface Timing

5.4.5 Host CPU Interface Timing

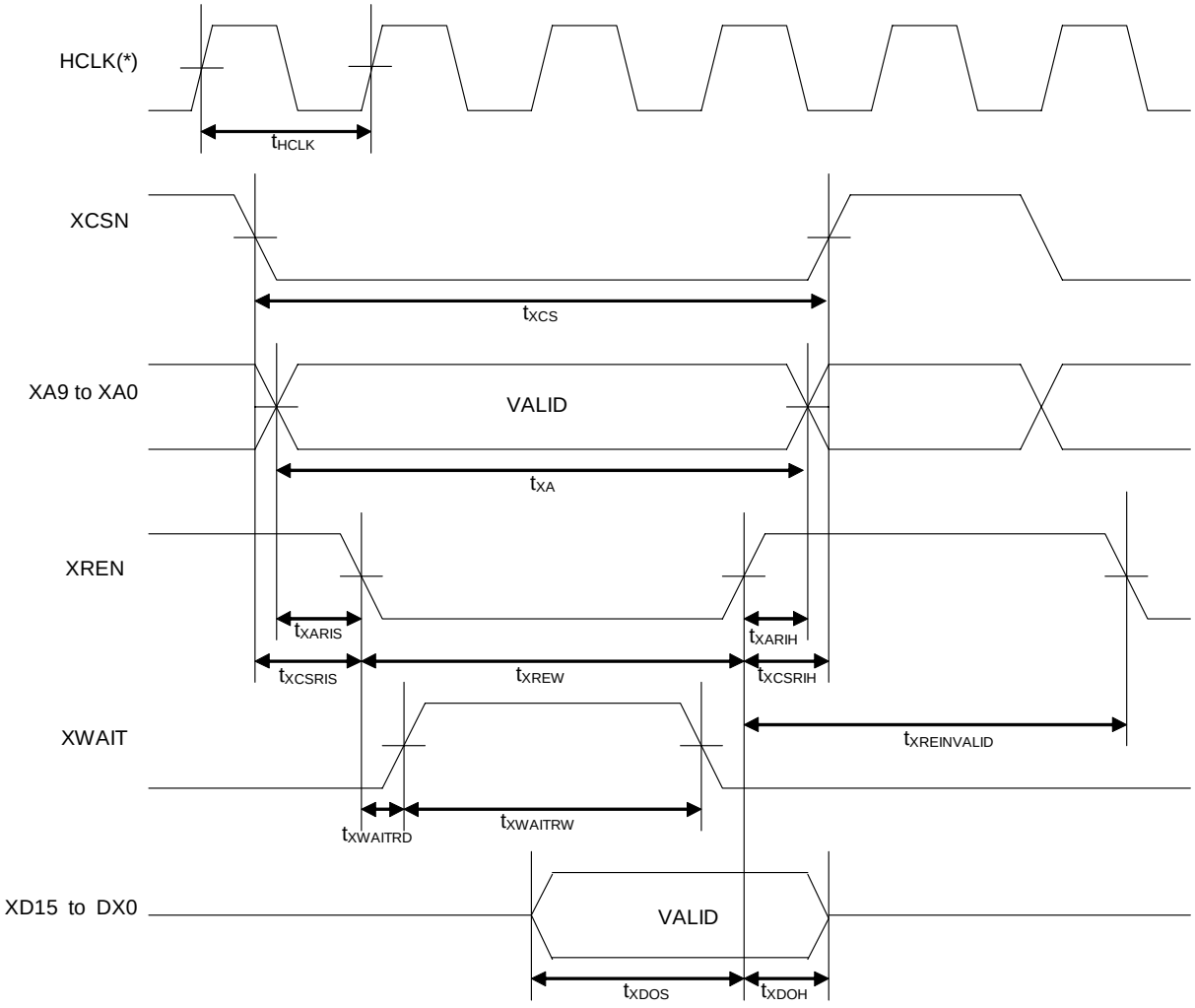
Table 5-8 Host CPU Interface Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
System clock period	t_{HCLK}	—	—	t_{CLK} / 3	—	ns	The signal internal to the LSI (81 MHz)
XCSN access time	t_{XCS}	CL = 40 pF	$5t_{HCLK}$ + 5.0	—	—	ns	
XA access time	t_{XA}		$5t_{HCLK}$ + 5.0	—	—		
XREN access time	t_{XREW}		$t_{XWAITRD}$ + $t_{XWAITRW}$ + 5.0	—	—		
XREN input setup time 1	t_{XCSRIS}		5.0	—	—		
XREN input setup time 2	t_{XARIS}		5.0	—	—		
XREN input hold time 1	t_{XCSRIH}		5.0	—	—		
XREN input hold time 2	t_{XARIH}		5.0	—	—		
XREN invalid time	$t_{XREINVALID}$		$2t_{HCLK}$ + 5.0	—	—		
XWEN access time	t_{XWEW}		$t_{XWAITWD}$ + $t_{XWAITWW}$ + 5.0	—	—		
XWEN input setup time 1	t_{XCSWIS}		5.0	—	—		
XWEN input setup time 2	t_{XAWIS}		5.0	—	—		
XWEN input hold time 1	t_{XCSWIH}		5.0	—	—		
XWEN input hold time 2	t_{XAWIH}		5.0	—	—		
XWEN invalid time	$t_{XWEINVALID}$		$2t_{HCLK}$ + 5.0	—	—		
XWAIT output delay time (read access)	$t_{XWAITRD}$		0.0	—	10.0		
XWAIT output delay time (write access)	$t_{XWAITWD}$		0.0	—	10.0		
XWAIT output time (read access)	$t_{XWAITRW}$		$4t_{HCLK}$	—	$7t_{HCLK}$		
XWAIT output time (write access)	$t_{XWAITWW}$		$4t_{HCLK}$	—	$7t_{HCLK}$		
XD output setup time	t_{XDOS}		t_{HCLK} – 2.0	—	—		
XD output hold time	t_{XDOH}		1.5	—	10.0		
XD input setup time	t_{XDIS}		5.0	—	—		
XD input hold time	t_{XDIH}		5.0	—	t_{HCLK}		

Note : t_{CLK} =1/ f_{CLK} (f_{CLK}=27MHz)

5.4.5.1 Read Cycle (Read Access from Host CPU to ML86410)



* The signal internal to the LSI

Figure 5-6 Host CPU Interface Timing (Read Cycle)

5.4.5.2 Write Cycle (Write Cycle from Host CPU to ML86410)

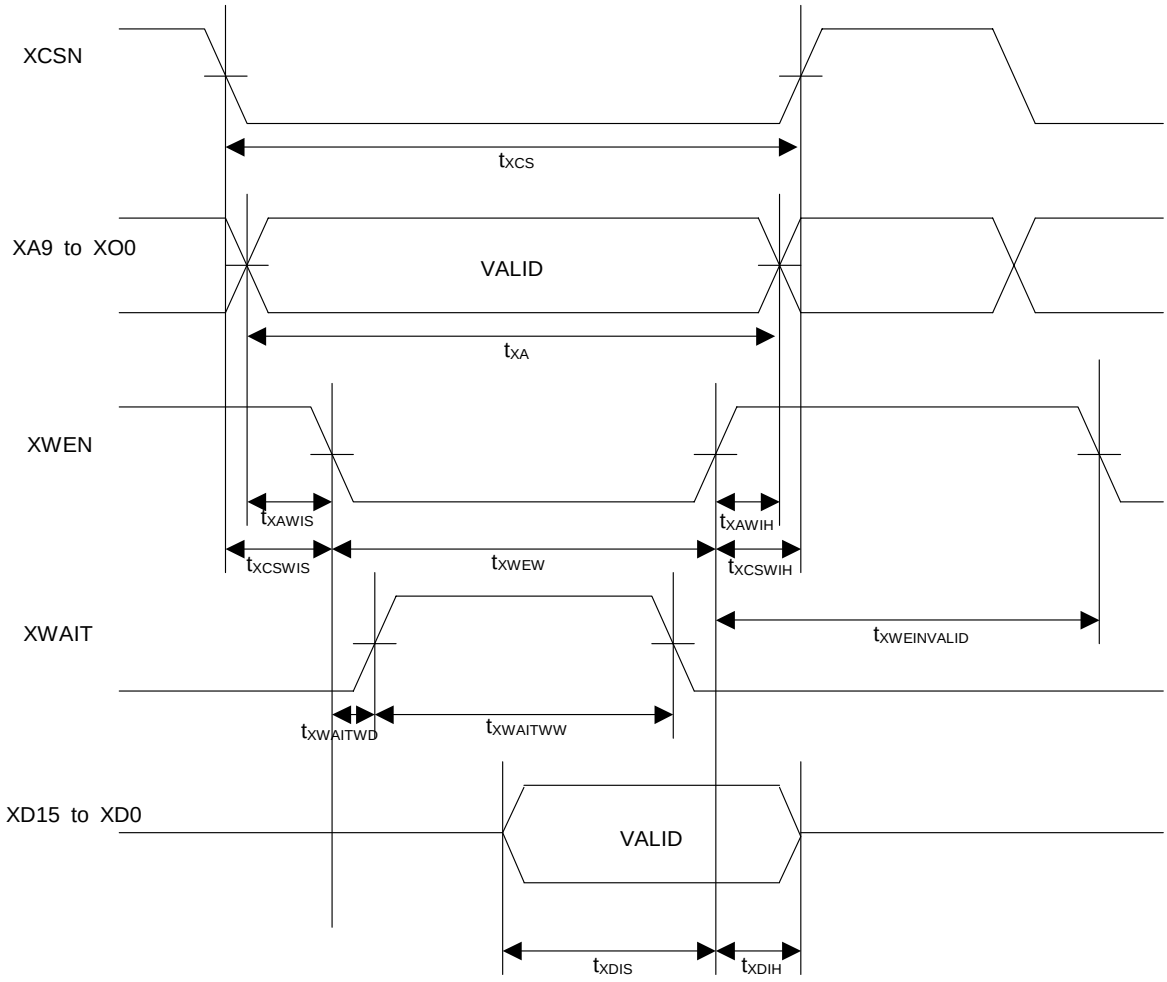


Figure 5-7 Host CPU Interface Timing (Write Cycle)

5.4.6 DMA Signal Timing

Table 5-9 DMA Signal Timing

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 3.0 to 3.6 V, Ta = -20 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
System clock period	t_{HCLK}	—	—	t_{CLK} / 3	—	ns	The signal internal to the LSI (81 MHz)
DREQ positive period	$t_{DREQPOS}$	CL=20pF	$4t_{HCLK}$	-	-	ns	
DREQ negative period	$t_{DREQNEG}$	CL=20pF	$3t_{HCLK}$	-	-	ns	
DREQ de-assert delay	t_{DREQDD}	CL=20pF	$3t_{HCLK}$	-	$5t_{HCLK}$	ns	This maximum value is a value when DACK is asserted after the DMA read access by this LSI is completed. When DACK is asserted before the access is completed, the DREQ deassert delay increases.
DREQ assert delay	t_{DREQAD}	CL=20pF	$3t_{HCLK}$	-	-	ns	
DACK positive period	$t_{DACKPOS}$	CL=20pF	$3t_{HCLK}$	-	-	ns	
DACK negative period	$t_{DACKNEG}$	CL=20pF	$3t_{HCLK}$	-	-	ns	
DACK de-assert delay	t_{DACKDD}	CL=20pF	$0t_{HCLK}$	-	-	ns	
DACK assert delay	t_{DACKAD}	CL=20pF	$0t_{HCLK}$	-	-	ns	

Note : t_{CLK} =1/ f_{CLK} (f_{CLK}=27MHz)

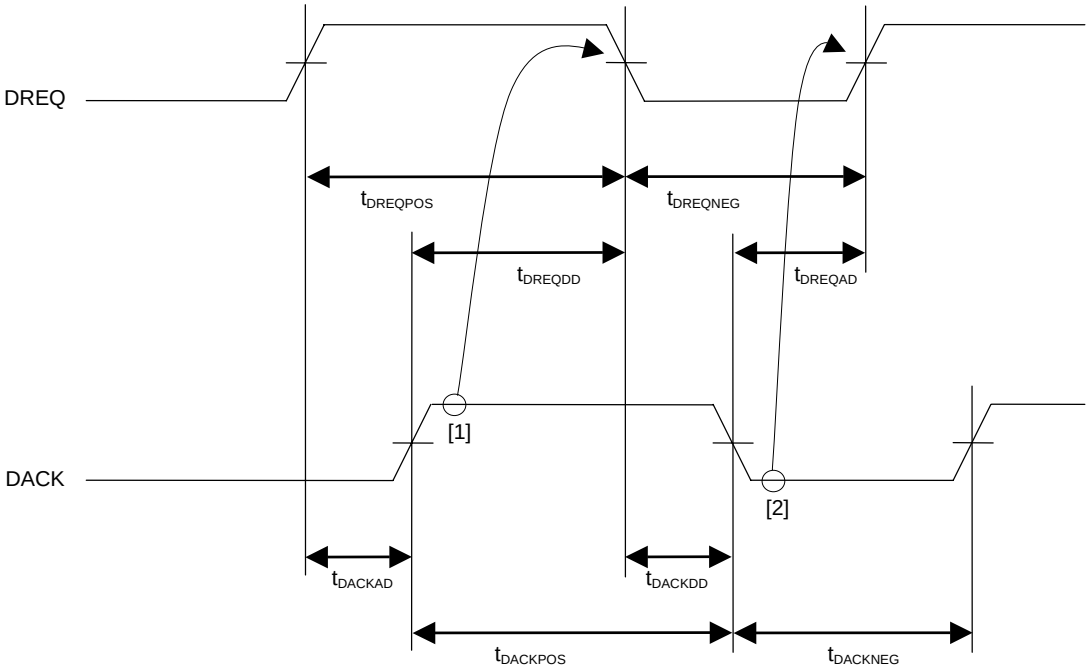


Figure 5-8 DMA Signal Timing

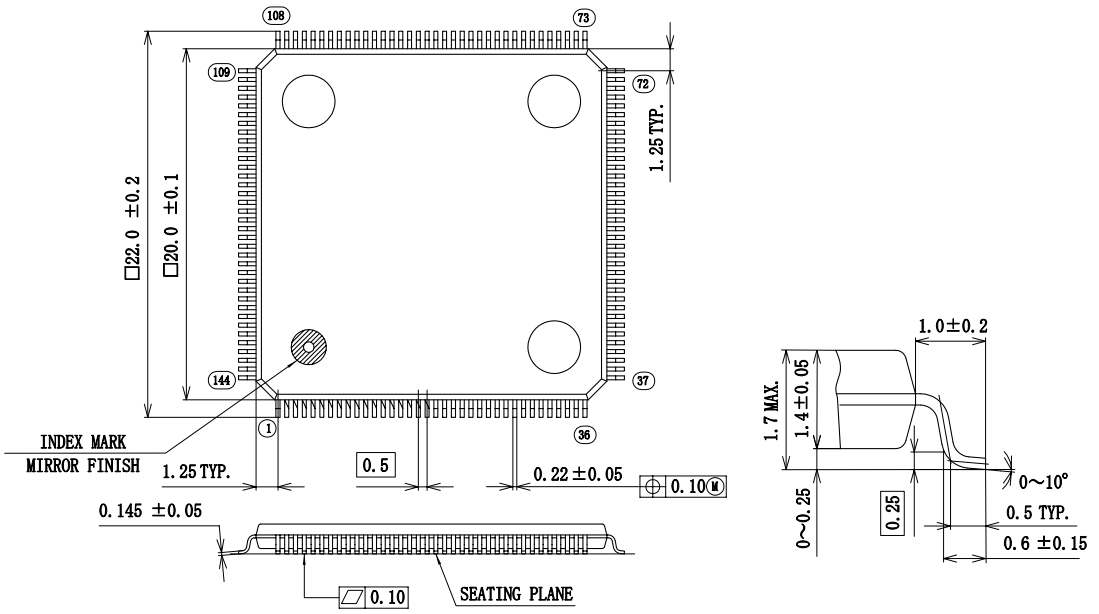
[1]: After the data transfer, the sample does DACK to this LSI. If DACK is high-level, DREQ is deasserted. It is waited to become high-level if it is a low-level.
This LSI operates recognizing the signal level of DACK.

[2]:After the DREQ is deasserted , this LSI waits for DACK to become a low-level.
When the DACK is low-level , the next stream data is transmitted.

6. Package Dimensions

(Unit: mm)

LQFP144-P-2020-0.50-ZK



Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Sn / 1 to 3Bi
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.29 TYP.
Rev. No./Last Revised	3/Nov. 15, 2004

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEUL86410-01	Oct.27,2006	–	–	Preliminary edition 1 (This edition is not official.)
PEUL86410-02	Dec.20,2006	–	–	Preliminary edition 2 (Same as Japanese 2nd edition)