Introduction

The phenomenal growth in design size and complexity continues to make design verification a critical bottleneck for today's FPGA systems. Limited access to internal signals, complex FPGA packages, and PCB electrical noise all contribute to making design debugging the most challenging process of the design cycle. More than 50% of the design cycle time can easily be spent on debugging and verifying the design. To help with the process of design debugging, Altera® provides a solution that enables a designer to examine the behavior of internal signals, without using extra I/O pins, while the design is running at full speed on an FPGA device.

The SignalTap® II Embedded Logic Analyzer is scalable, easy to use, and is included with the Quartus® II software subscription. This logic analyzer helps debug an FPGA design by probing the state of the internal signals in the design without the use of external equipment. Defining custom trigger-condition logic provides greater accuracy and improves the ability to isolate problems. The SignalTap II Embedded Logic Analyzer does not require external probes, or changes to the design files to capture the state of the internal nodes or I/O pins in the design. All captured signal data is conveniently stored in device memory until the designer is ready to read and analyze the data.

The SignalTap II Embedded Logic Analyzer is a second-generation system-level debugging tool that captures and displays real-time signal behavior in a system on a programmable chip (SOPC). The SignalTap II Embedded Logic Analyzer supports the highest number of channels, sample depth, and clock speeds of any embedded logic analyzer in the programmable logic market. Figure 12–1 shows a block diagram of the components that make up the SignalTap II Embedded Logic Analyzer.
This chapter is intended for any designer who wants to debug their FPGA design during normal device operation without the need for external lab equipment. Due to the SignalTap II Embedded Logic Analyzer’s similarity to traditional external logic analyzers, familiarity with external logic analyzer operations is helpful but not necessary. To take advantage of faster compile times when making changes to the SignalTap II Logic Analyzer, knowledge of the Quartus II Incremental Compilation feature is helpful.

For information about using the Quartus II Incremental Compilation feature, refer to the Incremental Compilation for Hierarchical & Team-Based Design chapter in the Quartus II Handbook.

Hardware & Software Requirements

The following components are required to perform logic analysis with the SignalTap II Embedded Logic Analyzer:

- Quartus II design software

or

Notes to Figure 12–1:

(1) This diagram assumes that the SignalTap II Logic Analyzer was compiled with the design as a separate design partition using the Quartus II Incremental Compilation feature. If incremental compilation is not used, the SignalTap II logic is integrated with the design. For information about the use of incremental compilation with SignalTap II, refer to “Faster Compilations Using SignalTap II Incremental Compilation” on page 12–40.
Quartus II Web Edition (with TalkBack feature enabled)  
or  
SignalTap II Logic Analyzer standalone software

- Download/Upload Cable
- Altera development kit or user design board with JTAG connection to device under test

Captured data is stored in the device’s memory blocks and transferred to the Quartus II software waveform display with a JTAG communication cable such as EthernetBlaster or USB-BlasterTM. Table 12–1 summarizes some of the features and benefits of the SignalTap II Embedded Logic Analyzer.

<table>
<thead>
<tr>
<th>Table 12–1. SignalTap II Features &amp; Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature</td>
</tr>
<tr>
<td>Multiple logic analyzers in a single device</td>
</tr>
<tr>
<td>Multiple logic analyzers in multiple devices</td>
</tr>
<tr>
<td>in a single JTAG chain</td>
</tr>
<tr>
<td>Plug-In Support</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Up to 10 basic or advanced trigger levels for</td>
</tr>
<tr>
<td>each analyzer</td>
</tr>
<tr>
<td>Power-Up Trigger</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Incremental Compilation</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Flexible buffer acquisition modes</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>MATLAB integration with included MEX function</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Up to 1,024 channels in each device</td>
</tr>
<tr>
<td>Up to 128K samples in each device</td>
</tr>
<tr>
<td>Clock frequencies up to 270 MHz</td>
</tr>
<tr>
<td>Resource usage estimator</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>No additional cost</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
The SignalTap II Logic Analyzer supports the following device families:

- Stratix® II
- Stratix II GX
- Stratix
- Stratix GX
- Cyclone II
- Cyclone™
- APEX™ II
- APEX 20KE
- APEX 20KC
- APEX 20K
- Mercury™

On-Chip Debugging Tool Comparison

The Quartus II software provides a number of different ways to help debug your FPGA design after programming the device. The SignalTap II Logic Analyzer, SignalProbe™, and the Logic Analyzer Interface (LAI) share some similar features, but each has advantages. In some debugging situations, it can be difficult to decide which tool is best to use or whether multiple tools are required. Table 12–2 compares these debugging tools and lists situations and requirements for the use of each.

<table>
<thead>
<tr>
<th>Feature</th>
<th>SignalProbe</th>
<th>Logic Analyzer Interface (LAI)</th>
<th>SignalTap II Embedded Analyzer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Depth—An external logic analyzer used with the LAI has a bigger buffer to store more captured data than SignalTap II Logic Analyzer. No data is captured or stored with SignalProbe.</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Ease in Debugging Timing Issue—An external logic analyzer used with the LAI provides you with access to a “timing” mode, enabling you to debug combined streams of data.</td>
<td>N/A</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Performance—The LAI adds minimal logic to a design, requiring fewer device resources. The SignalTap II Logic Analyzer has little affect on performance when it is set as a separate design partition using incremental compilation. SignalProbe incrementally routes nodes to pins, not affecting the design at all.</td>
<td>✓</td>
<td>✓(1)</td>
<td>✓(1)</td>
</tr>
</tbody>
</table>
## Table 12–2. On-Chip Debugging Tools-Comparison (Part 2 of 2)

<table>
<thead>
<tr>
<th>Feature</th>
<th>SignalProbe</th>
<th>Logic Analyzer Interface (LAI)</th>
<th>SignalTap II Embedded Analyzer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Compile and Recompile Time</strong>—SignalProbe attaches incrementally routed signals to previously reserved pins, requiring very little recompilation time to make changes to source signal selections. The SignalTap II Logic Analyzer and the LAI can take advantage of incremental compilation to refit their own design partitions to decrease recompilation time.</td>
<td>✔️</td>
<td>✔️ (1)</td>
<td>✔️ (1)</td>
</tr>
<tr>
<td><strong>Triggering Capability</strong>—Although advanced triggering is available in the SignalTap II Logic Analyzer, many additional triggering options are available on an external logic analyzer when used with the LAI.</td>
<td>N/A</td>
<td>✔️</td>
<td></td>
</tr>
<tr>
<td><strong>I/O Usage</strong>—No additional output pins are required with the SignalTap II Logic Analyzer. Both the LAI and SignalProbe require I/O pin assignments.</td>
<td></td>
<td></td>
<td>✔️</td>
</tr>
<tr>
<td><strong>Acquisition Speed</strong>—The SignalTap II Logic Analyzer can acquire data at speeds of over 200 MHz. The same acquisition speeds are obtainable with an external logic analyzer used with the LAI, but signal integrity issues may limit this.</td>
<td>N/A</td>
<td></td>
<td>✔️</td>
</tr>
<tr>
<td><strong>No JTAG Connection Required</strong>—An FPGA design with the SignalTap II Logic Analyzer or the LAI requires an active JTAG connection to a host running the Quartus II software. SignalProbe does not require a host for debugging purposes.</td>
<td>✔️</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>External Equipment</strong>—The SignalTap II Logic Analyzer is completely internal to the programmed FPGA device, so no extra equipment other than a JTAG connection is required. SignalProbe and the LAI requires the use of external debugging equipment such as multimeters, oscilloscopes, or logic analyzers.</td>
<td></td>
<td></td>
<td>✔️</td>
</tr>
</tbody>
</table>

*Note to Table 12–2:*
(1) Applies when used with incremental compilation.
Design Flow Using the SignalTap II Logic Analyzer

Figure 12–3 shows a typical overall FPGA design flow for using the SignalTap II Logic Analyzer in your design. A SignalTap II file (.stp) is added to and enabled in your project, or a SignalTap II HDL function, created with the MegaWizard® Plug-in Manager, is instantiated in your design. The diagram shows the flow of operations from initially adding the SignalTap II Logic Analyzer to your design to the final device configuration, testing, and debugging.

Figure 12–2. SignalTap II FPGA Design & Debugging Flow
SignalTap II Logic Analyzer Task Flow

To use the SignalTap II Logic Analyzer to debug your design, you perform a number of tasks to add, configure, and run the logic analyzer. **Figure 12–3** shows a typical flow of the tasks you complete to debug your design. Refer to the appropriate section of this chapter for more information about each of these tasks.

**Figure 12–3. SignalTap II Logic Analyzer Task Flow**
Add the SignalTap II Logic Analyzer to Your Design

Create a SignalTap II file or create a parameterized HDL instance representation of the logic analyzer using the MegaWizard Plug-In Manager. If you want to monitor multiple clock domains simultaneously, you can add additional instances of the logic analyzer to your design, limited only by the available resources in your device.

Configure the SignalTap II Logic Analyzer

Once the SignalTap II Logic Analyzer is added to your design, you configure it to monitor the signals you want. You can manually add signals or use a plug-in, such as the Nios II plug-in, to quickly add entire sets of associated signals. You can also specify settings for the data capture buffer such as its size, the method in which data is captured and stored, and the device memory type to use for the buffer in devices that support memory type selection.

Define Triggers

To capture signal data, you set up triggers that tell the logic analyzer under what conditions to begin the capture. The SignalTap II Logic Analyzer lets you define Run-Time Triggers that range from very simple, such as the rising edge of a single signal, to very complex, involving groups of signals, extra logic, and multiple conditions. Power-Up Triggers give you the ability to capture data from trigger events occurring immediately after the device enters user-mode after configuration.

Compile the Design

With the SignalTap II file configured and triggers defined, you compile your project as usual to include the logic analyzer in your design. Since you may need to frequently change monitored signal nodes or adjust trigger settings during debugging, you can use the incremental compilation feature built-in to the SignalTap II Logic Analyzer along with Quartus II incremental compilation to reduce recompile times.

Program the Target Device(s)

When you are debugging a design with the SignalTap II Logic Analyzer, you program a target device directly from the SignalTap II file without using the Quartus II Programmer. You can also program multiple devices with different designs and simultaneously debug them.
Run the SignalTap II Logic Analyzer

In normal device operation, you control the logic analyzer through the JTAG connection, specifying when to start looking for your trigger conditions to begin capturing data. With Run-Time or Power-Up Triggers, you read and transfer the captured data from the on-chip buffer to the SignalTap II file for analysis.

View, Analyze & Use Captured Data

Once you have captured data and read it into the SignalTap II file, it is available for analysis and use in the debugging process. You can set up mnemonic tables, either manually or with a plug-in, to make it easier to read and interpret the captured signal data. You can use the locate feature in the SignalTap II node list to quickly find the locations of problem nodes in other tools in the Quartus II software to speed up debugging. Save the captured data for later analysis or convert it to other formats for sharing and further study.

Add the SignalTap II Logic Analyzer to Your Design

Since the SignalTap II Logic Analyzer is implemented in logic on your target device, it must be added to your FPGA design as another part of the design itself. There are two ways to generate the SignalTap II Logic Analyzer and add it to your design for debugging. The first method is to create a SignalTap II file (.stp) and use the SignalTap II file window to configure the details of the logic analyzer. The second method is to create and configure the SignalTap II file with the MegaWizard Plug-in Manager and instantiate it in your design.

Creating & Enabling a SignalTap II File

To create an embedded logic analyzer, you can use an existing SignalTap II file or create a new file. Once a file is created or selected, it must be enabled in the project where it is used.

Creating a SignalTap II File

The SignalTap II file contains the SignalTap II Logic Analyzer settings and the captured data for viewing and analysis. To create a new SignalTap II file, perform the following steps:

1. On the File menu, click New.
2. In the New dialog box, click the Other Files tab, and select SignalTap II File.
3. Click OK.
To open an existing SignalTap II file already associated with your project, on the Tools menu, click **SignalTap II Logic Analyzer**. You can also use this method to create a new SignalTap II file if no SignalTap II file exists for the current project, or, to open an existing file, on the File menu, click **Open** and select a SignalTap II file (Figure 12–4).

*Figure 12–4. SignalTap II File Window*
Enabling & Disabling a SignalTap II File for the Current Project

Whenever you save a new SignalTap II file, the Quartus II software asks you if you want to enable the file for the current project. However, you can add this file manually, change the selected SignalTap II file, or completely disable the logic analyzer by performing the following steps:

1. On the Assignments menu, click Settings. The Settings dialog box appears.

2. In the Category list, select SignalTap II Logic Analyzer. The SignalTap II Logic Analyzer page appears.

3. Turn on Enable SignalTap II Logic Analyzer. Turn off this option to disable the logic analyzer, completely removing it from your design.

4. In the SignalTap II File name box, type the name of the SignalTap II file you want to include with your design, or browse to and select a file name.

5. Click OK.

Using the MegaWizard Plug-In Manager to Create Your Embedded Logic Analyzer

Alternatively, you can create a SignalTap II Logic Analyzer instance by using the MegaWizard Plug-In Manager. The MegaWizard Plug-In Manager generates an HDL file that you instantiate in your design. You can also use a hybrid approach in which you instantiate the MegaWizard Plug-In Manager file in your HDL, and then use the method described in “Creating & Enabling a SignalTap II File” on page 12–9.

Creating an HDL Representation Using the MegaWizard Plug-In Manager

The Quartus II software allows you to easily create your SignalTap II Logic Analyzer using the MegaWizard Plug-In Manager. To implement the SignalTap II megafunction, perform the following steps:

1. On the Tools menu, click MegaWizard Plug-In Manager. The MegaWizard Plug-In Manager dialog box appears.

2. Select Create a new custom megafuction variation.

3. Click Next.
4. In the Installed Plug-In list, select SignalTap II Logic Analyzer. Select an output file type and enter the desired name of the SignalTap II megafunction. You can choose AHDL (.tdf), VHDL (.vhd), or Verilog HDL (.v) as the output file type (Figure 12–5).

![MegaWizard Plug-In Manager](image)

**Figure 12–5. Creating the SignalTap II Logic Analyzer in the MegaWizard Plug-In Manager**

5. Click Next.

6. Configure the analyzer by specifying the Sample depth, RAM Type, Data input port width, Trigger levels, Trigger input port width, and whether to enable an external Trigger in or Trigger out (Figure 12–6).
7. Click Next.

8. Set the **Trigger level** options by selecting **Basic** or **Advanced** (Figure 12–7).

    ![You cannot define a Power-Up Trigger using the MegaWizard Plug-In Manager. Refer to “Define Triggers” on page 12–28 to learn how to do this using the SignalTap II file.]
9. Click **Finish** to create an HDL representation of the SignalTap II Logic Analyzer.

For information about the configuration settings options in the MegaWizard Plug-In Manager, refer to “Configure the SignalTap II Logic Analyzer” on page 12–17. For information about defining triggers, refer to “Define Triggers” on page 12–28.
SignalTap II Megafunction Ports

Table 12–3 provides information on the SignalTap II megafunction ports.

For the most current information on the ports and parameters for this megafunction, refer to the latest version of the Quartus II Help.

<table>
<thead>
<tr>
<th>Port Name</th>
<th>Type</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>acq_data_in</td>
<td>Input</td>
<td>No</td>
<td>This set of signals represents the set of signals that are monitored in the SignalTap II Logic Analyzer.</td>
</tr>
<tr>
<td>acq_trigger_in</td>
<td>Input</td>
<td>No</td>
<td>This set of signals represents the set of signals that are used to trigger the analyzer.</td>
</tr>
<tr>
<td>acq_clk</td>
<td>Input</td>
<td>Yes</td>
<td>This port represents the sampling clock that the SignalTap II Logic Analyzer uses to capture data.</td>
</tr>
<tr>
<td>trigger_in</td>
<td>Input</td>
<td>No</td>
<td>This signal is used to trigger the SignalTap II Logic Analyzer.</td>
</tr>
<tr>
<td>trigger_out</td>
<td>Output</td>
<td>No</td>
<td>This signal is enabled when the trigger event occurs.</td>
</tr>
</tbody>
</table>

Instantiating the SignalTap II Logic Analyzer in Your HDL

Instantiating the logic analyzer in your HDL is similar to instantiating any other Verilog HDL or VHDL megafunction in your design. You can instantiate up to 127 analyzers in your design, or as many as physically fit in the FPGA. Once you have instantiated the SignalTap II file in your HDL file, compile your Quartus II project to fit the logic analyzer in the target FPGA.

To capture and view the data, you must create a SignalTap II file from your SignalTap II HDL output file. To do this, select Create/Update on the File menu, and click Create SignalTap II File from Design Instance(s).

Embedding Multiple Analyzers in One FPGA

The SignalTap II Logic Analyzer includes support for multiple logic analyzers in an FPGA device. This feature allows you to create a unique logic analyzer for each clock domain in the design. As multiple instances of the analyzer are added to the SignalTap II file, the resource usage increases proportionally.

In addition to debugging multiple clock domains, this feature allows you to apply the same SignalTap II settings to a group of signals in the same clock domain. For example, if you have a set of signals that must use a
sample depth of 64K, while another set of signals in the same clock domain requires a sample depth of 1K, you can create two instances to meet these needs.

To create multiple analyzers, on the Edit menu, click Create Instance, or right-click in the Instance Manager window and click Create Instance.

**Monitoring FPGA Resources Used by the SignalTap II Logic Analyzer**

The SignalTap II Logic Analyzer has a built-in resource estimator that calculates the logic resources and amount of memory that each SignalTap II Logic Analyzer uses. You can see the resource usage of each logic analyzer instance and the total resources used in the columns of the Instance Manager section of the SignalTap II file window. This feature is useful when device resources are limited and you must know what device resources the SignalTap II Logic Analyzer uses. The value reported in the resource usage estimator may vary by as much as 5% from the actual resource usage.

Table 12–4 shows the SignalTap II Logic Analyzer M4K memory block resource usage for these devices per signal width and sample depth.

<table>
<thead>
<tr>
<th>Signals (Width)</th>
<th>Samples (Width)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>256</td>
</tr>
<tr>
<td>8</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>16</td>
<td>1</td>
</tr>
<tr>
<td>32</td>
<td>2</td>
</tr>
<tr>
<td>64</td>
<td>4</td>
</tr>
<tr>
<td>256</td>
<td>16</td>
</tr>
</tbody>
</table>

*Note to Table 12–4:*

(1) When you configure a SignalTap II Logic Analyzer, the Instance Manager reports an estimate of the memory bits and logic elements required to implement the given configuration.
Configure the SignalTap II Logic Analyzer

The SignalTap II file provides many options for configuring instances of the logic analyzer. Some of the settings are similar to those found on traditional external logic analyzers. Other settings are unique to the SignalTap II Logic Analyzer because of the properties of configuring an embedded logic analyzer. All settings give you the ability to configure the logic analyzer the way you want to help debug your design.

Some settings can only be adjusted when you are viewing Run-Time Trigger conditions instead of Power-Up Trigger conditions. To learn about Power-Up Triggers and viewing different trigger conditions, refer to “Creating a Power-Up Trigger” on page 12–33.

Assigning an Acquisition Clock

You must assign a clock signal to control the acquisition of data by the SignalTap II Logic Analyzer. The logic analyzer samples data on every rising edge of the acquisition clock. You can use any signal in your design as the acquisition clock. However, for best results, Altera recommends that you use a global clock for data acquisition and not a gated clock. Using a gated clock as your acquisition clock can result in unexpected data that does not accurately reflect the behavior of your design. The Quartus II Timing Analyzer shows the maximum acquisition clock frequency at which you can run your design.

To assign an acquisition clock, perform the following steps:

1. In the SignalTap II Logic Analyzer window, click the Setup tab.

2. Click Browse next to the Clock field in the Signal Configuration pane. The Node Finder dialog box appears.

3. If you are not using the SignalTap II incremental compilation feature, select SignalTap II: pre-synthesis in the Filter list.
   or
   If you are using incremental compilation, select SignalTap II: post-fitting in the Filter list.

You cannot insert a clock signal that is shown in the SignalTap II: post-fitting filter unless you are using incremental compilation. The opposite is true as well. If you are using incremental compilation, you cannot use a clock signal shown in the SignalTap II: pre-synthesis filter. For more information about the use of incremental compilation with SignalTap II, refer to “Compile the Design” on page 12–39.
4. In the **Named** field, type or select the name of the signal that you would like to use as your sample clock.

5. To start the node search, click **List**.

6. In the **Node Finder** dialog box, select the node representing the design's global clock signal.

7. To copy the selected node name to the **Selected Nodes** list, click “>” or Double-click the node name.

8. Click **OK**. The node is now specified as the clock in the SignalTap II window.

If you do not assign an acquisition clock in the SignalTap II window, the Quartus II software automatically creates a clock pin called `auto_stp_external_clk`.

You must make a pin assignment to this pin independently from the design. You must ensure that a clock signal in your design drives the acquisition clock.

For information on assigning signals to pins, refer to the **I/O Management** chapter in volume 2 of the *Quartus II Handbook*.

**Adding Signals to the SignalTap II File**

While configuring the logic analyzer, you add signals to the node list in the SignalTap II file to select which signals in your design you want to monitor. Selected signals are also used to define triggers. You can assign the following two types of signals to your SignalTap II file:

- **Pre-synthesis**—A pre-synthesis signal exists after design elaboration, but before any synthesis optimizations are done. This set of signals should reflect your Register Transfer Level (RTL) signals.

- **Post-fitting**—A post-fitting signal exists after physical synthesis optimizations and place-and-route.

If you are not using incremental compilation, add only pre-synthesis signals to your SignalTap II file. This is particularly useful if you want to quickly add a new node after you have made design changes. To do this, on the Processing menu, click **Start Analysis & Elaboration**.
After successful Analysis and Elaboration, the signals shown in red text are invalid signals, and you must remove them from the SignalTap II file for correct operation. This can happen if, for example, you added pre-synthesis signals to the SignalTap II file and then enabled incremental compilation. Because only post-fitting signals are used with SignalTap II incremental compilation, the pre-synthesis signals are invalid. The SignalTap II Health Monitor also indicates if an invalid node name exists in the SignalTap II file.

For more information about the use of incremental compilation with the SignalTap II Logic Analyzer, refer to “Faster Compilations Using SignalTap II Incremental Compilation” on page 12–40.

**Signal Preservation**

Many of your RTL signals are optimized during the process of synthesis and place-and-route. This can lead to issues when you debug your design, because the post-fitting signal names differ significantly from your RTL names. This can also cause a problem if you are using incremental compilation. Since only post-fitting signals can be added to the SignalTap II Logic Analyzer if incremental compilation is used, RTL signals that you want to monitor may not be available post-fit, preventing their usage. To avoid this issue, you can use synthesis attributes to preserve signals during synthesis and place-and-route. When the Quartus II software encounters these synthesis attributes, it does not perform any optimization on the specified signals, forcing them to continue to exist in the post-fit netlist. However, if you do this, you could see an increase in resource utilization or a decrease in timing performance. The two attributes you can use are:

- **Keep**—This attribute ensures that combinational signals are not removed.
- **Preserve**—This attribute ensures that registers are not removed.

For more information on using these attributes, refer to the *Quartus II Integrated Synthesis* chapter in volume 1 of the *Quartus II Handbook*.

If you are debugging an IP core, such as the Nios II CPU, you may need to preserve nodes from these cores to make them available for debugging with the SignalTap II Logic Analyzer. This is often necessary when a plug-in is used to add a group of signals for a particular IP. To do this, on the Assignments menu, click **Settings**. In the **Category** list, select **Analysis & Synthesis Settings**. Turn on **Create debugging nodes for IP cores** to make these nodes available to the SignalTap II Logic Analyzer.
Assigning Data Signals

To assign data signals, perform the following steps:

1. Perform Analysis and Elaboration, Analysis and Synthesis, or compile your design.

2. In the SignalTap II Logic Analyzer window, click the Setup tab.

3. Double-click anywhere in the node list of the SignalTap II window to open the Node Finder dialog box.

4. In the Fitter list, select SignalTap II: pre-synthesis or SignalTap II: post-fitting.

   If you use the SignalTap II Incremental Compilation feature, you can only add post-fitting nodes to the node list.

5. In the Named field, type a node name, partial node name, or wildcard characters. To start the node name search, click List.

6. In the Nodes Found list, select the node or bus you want to add to the SignalTap II file.

7. To copy the selected node names to the Selected Nodes list, double-click the names or click “>”.

8. To insert the selected nodes in the SignalTap II file, click OK. With the default colors set for the SignalTap II Logic Analyzer, a pre-synthesis signal in the list is shown in black while a post-fitting signal is shown in blue.

   You can also drag and drop signals from the Node Finder dialog box into a SignalTap II file.

Node List Signal Use Options

Once a signal is added to the node list, you can specify options about how the signal is used with the logic analyzer. You can turn off the ability of a signal to trigger the analyzer by disabling the Trigger Enable for that signal in the node list in the SignalTap II file. This option is useful when you want to see only the captured data for a signal, and you are not using that signal as part of a trigger.

You can turn off the ability to view data for a signal by disabling the Data Enable column. This option is useful when you want to trigger on a signal, but have no interest in viewing data for that signal.
For information about using signals in the node list to create SignalTap II trigger conditions, refer to “Define Triggers” on page 12–28.

**Untappable Signals**

Not all of the post-fitting signals in your design are available in the **SignalTap II: post-fitting** filter in the **Node Finder** dialog box. The following signal types cannot be tapped:

- Signals that are part of a carry chain—You cannot tap the carry out (\texttt{cout0} or \texttt{cout1}) signal of a logic element. Due to architectural restrictions, the carry out signal can only feed the carry in of another logic element (LE).
- Phase-locked loop (PLL) \texttt{clkout}—You cannot tap the output clock of a PLL. Due to architectural restrictions, the \texttt{clkout} signal can only feed the clock port of a register.
- JTAG Signals—You cannot tap the JTAG control (\texttt{TCK}, \texttt{TDI}, \texttt{TDO}, and \texttt{TMS}) signals.
- ALTGXB megafonction—You can not directly tap any ports of an ALTGXB instantiation.
- LVDS—You cannot tap the data output from a serializer/deserializer (SERDES) block.

**Adding Signals with a Plug-In**

Instead of adding individual or grouped signals through the **Node Finder** dialog box, you can add groups of relevant signals of a particular type of IP through the use of a plug-in. The SignalTap II Logic Analyzer comes with one plug-in already installed for the Nios II processor. Besides easy signal addition, plug-ins also provide a number of other features such as pre-designed mnemonic tables, useful for trigger creation and data viewing, as well as the ability to disassemble code in captured data.

The Nios II plug-in, for example, creates one mnemonic table in the **Setup** tab, and two tables in the **Data** tab:

- **Nios II Instruction** (**Setup** tab)—Capture all the required signals for triggering on a selected instruction address.
- **Nios II Instance Address** (**Data** tab)—Display address of executed instructions in hexadecimal format or as a programming symbol name if defined in an optional Executable and Linking Format (.elf) file.
- **Nios II Disassembly** (**Data** tab)—Displays disassembled code from the corresponding address.
For information about the other features plug-ins provide, refer to “Define Triggers” on page 12–28 and “View, Analyze & Use Captured Data” on page 12–50.

To add signals to the SignalTap II file using a plug-in, perform the following steps:

1. Right-click in the node list. On the **Add Nodes with Plug-In** submenu, click the name of the plug-in you want to use, such as the included plug-in named **Nios II**.

   ![Image](image1.png)

   If the intellectual property (IP) for the selected plug-in does not exist in your design, a message appears informing you that you cannot use the selected plug-in.

2. A dialog box appears with the IP hierarchy of your design (Figure 12–8). Select the IP that has the signals you want to monitor with the plug-in, and click **OK**.

   ![Figure 12–8. IP Hierarchy Selection](image2.png)

3. If all the signals in the plug-in are available, a dialog box may appear, depending on the plug-in selected, where you can set any available options for the plug-in. With the Nios II plug-in, you can optionally select an Executable and Linking Format (.elf) file containing program symbols from your Nios II Integrated Development Environment (IDE) software design. Set options for the selected plug-in as desired, and click **OK**.
To make sure all the required signals are available, turn on the **Create debugging nodes for IP cores** option in the Quartus II Analysis & Synthesis settings.

All the signals included in the plug-in are added to the node list.

**Enabling Debug Ports to Preserve FPGA Memory**

You can configure the SignalTap II Logic Analyzer to store captured data in the device RAM or route captured data to I/O pins to analyze with an external logic analyzer. The following factors can affect the mode of operation you choose:

- The availability of device RAM and I/O pins
- The number of trigger levels in use in the analysis
- Whether the SignalTap II Logic Analyzer is used in conjunction with external test equipment

When device RAM is limited, you can route internal signals to unused I/O pins for capture by an external logic analyzer. This method is useful for memory-intensive applications in which the amount of saved data exceeds the available device RAM. The Quartus II software automatically generates debugging port signals that connect internal FPGA signals to output pins. You must assign these signals to I/O pins. To use the SignalTap II Logic Analyzer debugging port configuration, perform the following steps:

1. In the SignalTap II file window, select one or more signals in the node list.

2. On the Edit menu, click **Enable Debug Port**, or right-click in the **Debug Port Out** column of the node list, and click **Enable Debug Port**.

   If you want to rename the debugging port pins, type the new name in the **Debug Port Out** column. The default signal name for the debugging ports is `auto_stp_debug_out_<m>_<n>`, where `m` refers to the instance number and `n` refers to the signal number. For example, if you enable the debugging port in the second instance for the fourth signal, the resulting signal name is `auto_stp_debug_out_2_4`.

3. Manually assign the debugging port signal name to an unused I/O pin.

   For information on assigning signals to pins, refer to the **I/O Management** chapter in volume 2 of the *Quartus II Handbook*. 
You can use this feature in conjunction with an external trigger out to synchronize an external logic analyzer with the SignalTap II Logic Analyzer.

To set up an external trigger out signal, refer to “Using External Triggers” on page 12–36.

**Specifying the Sample Depth**

The sample depth specifies the number of samples that are captured and stored for each signal. To set the sample depth, select the desired number of samples in the **Sample Depth** list. The sample depth ranges from 0 to 128K.

**Capturing Data to a Specific RAM Type**

When you use the SignalTap II Logic Analyzer with some devices, you have the option to select the RAM type where acquisition data is stored. RAM selection allows you to preserve a specific memory block for your design and allocate another portion of memory for SignalTap II data acquisition. For example, if your design implements a large buffering application such as a system cache, it is ideal to place this application into M-RAM blocks so that the remaining M512 or M4K blocks are used for SignalTap II data acquisition.

To select the RAM type to use for the SignalTap II buffer, select it from the **RAM type** list. Use this feature when the acquired data (as reported by the SignalTap II resource estimator) is not larger than the available memory of the memory type that you have selected in the FPGA.

**Choosing the Buffer Acquisition Mode**

The buffer acquisition type selection feature in the SignalTap II Logic Analyzer lets you choose how the captured data buffer is organized and can potentially reduce the amount of memory that is required for SignalTap II data acquisition. You can choose to use either a circular buffer, specifying how much data is captured before and after a trigger occurs, or a segmented buffer, useful for capturing triggers that occur periodically. **Figure 12–9** illustrates the differences between the two buffer types.
Circular Buffer

The circular buffer is the default buffer type used by the SignalTap II Logic Analyzer. While the logic analyzer is running, data is stored in the buffer until it fills up, at which point new data replaces the oldest data. This continues until a specified trigger event occurs. When this happens, the logic analyzer continues to capture data after the trigger event until the buffer is full, based on the circular buffer trigger position setting in the Signal Configuration pane in the SignalTap II file. Select a setting from the list to choose whether to capture the majority of the data before (Post trigger position) or after (Pre trigger position) the trigger occurs or to center the trigger position in the data (Center trigger position). You can also choose to continuously capture data until the logic analyzer is stopped.

For more information, refer to “Specifying the Trigger Position” on page 12–36.

Segmented Buffer

The segmented buffer organizes the buffer into a number of separate, evenly sized segments. This type of buffer organization makes it easier to debug systems that contain relatively infrequent periodic events. Figure 12–10 shows an example of this type of buffer system.
The SignalTap II Logic Analyzer verifies the functionality of the design shown in Figure 10–9 to ensure that the correct data is written to the SRAM controller. The buffer acquisition in the SignalTap II Logic Analyzer allows you to monitor the RDATA port when $H'0F0F0F0F$ is sent into the RADDR port. You can monitor multiple read transactions from the SRAM device without running the SignalTap II Logic Analyzer again. The buffer acquisition feature allows you to segment the memory so that you can capture the same event multiple times without wasting the allocated memory. The number of cycles that are captured depends on the number of segments that you have specified in the Signal Configuration settings.

To enable and configure buffer acquisition, select Segmented in the SignalTap II window, and select the number of segments to use. In the example, selecting sixty-four 64-bit segments allows you to capture 64 read cycles when the RADDR signal is $H'0F0F0F0F$.

For more information on the buffer acquisition mode, refer to Setting the Buffer Acquisition Mode in the Quartus II Help.

Managing Multiple SignalTap II Files & Configurations

In many instances, you can have more than one SignalTap II file in one design. Each file potentially has a different group of monitored signals. These signals groups make it possible to debug different blocks in your design. Along with each SignalTap II file, there is an associated programming file (SRAM Object File (SOF)). Managing all of the
SignalTap II files and their associated programming files is a challenging task. To help you manage these files, you can use the **Data Log** feature and the **SOF Manager**.

The **Data Log** allows you to store multiple SignalTap II configurations. **Figure 12–11** shows two signal set configurations with multiple trigger conditions in one SignalTap II file. To toggle between the active configurations, double-click on an entry in the **Data Log**. As you toggle between the different configurations, the signal list and trigger conditions change in the **Setup** tab of the SignalTap II file. The active configuration displayed in the SignalTap II file is indicated by the blue square around the signal set in the **Data log**. To store a configuration in the data log, on the Edit menu, click **Save to Data Log**, or click **Save to Data Log** at the top of the Data Log.

**Figure 12–11. Data Log**
The SOF Manager allows you to embed multiple SOF into one SignalTap II file. To embed a new SOF in the SignalTap II file, right-click in the SOF Manager, and click Attach SOF File (Figure 12–12).

**Figure 12–12. SOF Manager**

As you switch between configurations in the Data Log, you can extract the SOF associated with that particular configuration and use the programmer in the SignalTap II Logic Analyzer to download the new SOF to the FPGA.

**Define Triggers**

To capture the data you want at the right time, you need to specify conditions under which the signals you are monitoring display that data. In the SignalTap II Logic Analyzer, these conditions are referred to as triggers, just as they are in conventional external logic analyzers and oscilloscopes. You have many options for creating different types of triggers to help in your debugging.
Creating Basic Triggers

The simplest kind of trigger you can use is a basic trigger. You select this from the list at the top of the *Trigger Levels* column in the node list in the SignalTap II file window. With the trigger type set to *Basic*, you must set the trigger pattern for each signal you’ve added in the SignalTap II file. To set the trigger pattern, right-click in the *Trigger Levels* column and click the desired pattern. You can set the trigger pattern to any of the following conditions:

- Don’t Care
- Low
- High
- Falling Edge
- Rising Edge
- Either Edge

For buses, you can type in a pattern in binary, or right-click and select *Insert Value* to enter the pattern in other number formats. For signals added to the SignalTap II file through the use of a plug-in or any signals with an associated mnemonic table, you can right-click and select a mnemonic to set pre-defined conditions for the trigger. Data capture begins when the logical AND of all the signals for a given level evaluates to TRUE.

Creating Advanced Triggers

Along with the SignalTap II Logic Analyzer’s basic triggering capabilities, you can build more complex triggers utilizing extra logic that enable you to capture data when a particular combination of conditions exist. If you set the trigger type to *Advanced* at the top of the *Trigger Levels* column in the node list of the SignalTap II file window, a new tab named *Advanced Trigger* appears where you can build a complex trigger expression using a simple GUI. You can drag and drop operators into the Advanced Trigger Configuration Editor window to build the complex trigger condition in an expression tree. *Table 12–5* lists the operators you can use.

<table>
<thead>
<tr>
<th>Name of Operator</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Less Than</td>
<td>Comparison</td>
</tr>
<tr>
<td>Less Than or Equal To</td>
<td>Comparison</td>
</tr>
<tr>
<td>Equality</td>
<td>Comparison</td>
</tr>
<tr>
<td>Inequality</td>
<td>Comparison</td>
</tr>
</tbody>
</table>

*Table 12–5. Advanced Triggering Operators*  
*Note (1) (Part 1 of 2)*
### Table 12–5. Advanced Triggering Operators

<table>
<thead>
<tr>
<th>Name of Operator</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Greater Than</td>
<td>Comparison</td>
</tr>
<tr>
<td>Greater Than or Equal To</td>
<td>Comparison</td>
</tr>
<tr>
<td>Logical NOT</td>
<td>Logical</td>
</tr>
<tr>
<td>Logical AND</td>
<td>Logical</td>
</tr>
<tr>
<td>Logical OR</td>
<td>Logical</td>
</tr>
<tr>
<td>Logical XOR</td>
<td>Logical</td>
</tr>
<tr>
<td>Reduction AND</td>
<td>Reduction</td>
</tr>
<tr>
<td>Reduction OR</td>
<td>Reduction</td>
</tr>
<tr>
<td>Reduction XOR</td>
<td>Reduction</td>
</tr>
<tr>
<td>Left Shift</td>
<td>Shift</td>
</tr>
<tr>
<td>Right Shift</td>
<td>Shift</td>
</tr>
<tr>
<td>Bitwise Complement</td>
<td>Bitwise</td>
</tr>
<tr>
<td>Bitwise AND</td>
<td>Bitwise</td>
</tr>
<tr>
<td>Bitwise OR</td>
<td>Bitwise</td>
</tr>
<tr>
<td>Bitwise XOR</td>
<td>Bitwise</td>
</tr>
<tr>
<td>Edge and Level Detector</td>
<td>Signal Detection</td>
</tr>
<tr>
<td>Continuous Counter</td>
<td>Counter</td>
</tr>
<tr>
<td>State Counter</td>
<td>Counter</td>
</tr>
<tr>
<td>Event Counter</td>
<td>Counter</td>
</tr>
</tbody>
</table>

**Note to Table 12–5:**

(1) For more information on each of these operators, refer to the Quartus II Help.

You can configure some of the operators at run time. This enables you to change one operator type to another operator type without recompiling your design. Operators that have a white background are run-time configurable.

Adding many objects to the Advanced Trigger Condition Editor can make the workspace cluttered and difficult to read. To keep objects organized while you build your advanced trigger condition, use the right-click menu and select **Arrange All Objects**. You can also use the **Zoom-Out** command to fit more objects into the Advanced Trigger Condition editor window.
Examples of Advanced Triggering Expressions

The following examples show how to use Advanced Triggering:

- Trigger when bus outa is greater than or equal to outb (Figure 12–13).

**Figure 12–13. Bus outa is Greater Than or Equal to Bus outb**

```
Advanced Trigger Condition Editor Level 1
Result: outa>=outb
```

- Trigger when bus outa is greater than or equal to bus outb, and when the enable signal has a rising edge (Figure 12–14).

**Figure 12–14. Enable Signal has a Rising Edge**

```
Result: outa>=outb&&EDL((enable))
```
Trigger when bus `outa` is greater than or equal to bus `outb`, or when the enable signal has a rising edge. Or, when a bitwise AND operation has been performed with bus `outc` and bus `outd`, and all bits of the result of that operation are equal to 1 (Figure 12–15).

**Figure 12–15. Bitwise AND Operation**

Result: `outa >= outb | | ELD({enable}) | | (outc & outd)`

---

**Advanced Triggering Using Post-Fitting & Incrementally Routed Pre-Synthesis Nodes**

If you are not using the Quartus II Incremental Compilation feature on your design, you can use the advanced triggering capability only with pre-synthesis nodes that are not set to be incrementally routed. Post-fitting nodes and incrementally routed pre-synthesis nodes are only used for basic trigger operations. However, you can create an advanced trigger that uses the results of a basic trigger created with post-fitting and incrementally routed pre-synthesis nodes. Set the trigger type to Basic and create basic trigger settings for the post-fitting and incrementally routed pre-synthesis nodes, then set the trigger type to Advanced. The post-fitting and incrementally routed pre-synthesis nodes are not shown in the node list in the Advanced Trigger tab, but a special symbol is automatically placed in the Advanced Trigger Condition Editor that represents the basic trigger you created (Figure 12–16).
Figure 12–16. Symbol for SignalTap II File Containing Post-Fitting Nodes

The output of this node can be combined with any of the operators listed in Table 12–5.

The special symbol for post-fitting and incrementally routed pre-synthesis nodes is only shown when you are not using the Quartus II incremental compilation feature on your design. If you are using incremental compilation, pre-synthesis nodes that were not preserved through synthesis to become post-fitting nodes are not available for monitoring or triggering. However, with incremental compilation, all post-fitting nodes are available for advanced triggering and appear in the node list in the Advanced Trigger tab. To learn about the use of incremental compilation with SignalTap II, refer to “Faster Compilations Using SignalTap II Incremental Compilation” on page 12–40.

For information about using the incremental routing feature in the SignalTap II Logic Analyzer, refer to the Quartus II Help.

Creating a Power-Up Trigger

Typically, the SignalTap II Logic Analyzer is used to trigger on events that occur during normal device operation. You start an analysis manually once the target device is fully powered on and the device’s JTAG connection is available. However, there may be cases when you would like to capture trigger events that occur during device initialization immediately after the FPGA is powered on or reset. With the SignalTap II Power-Up Trigger feature, you can capture data from triggers that occur after device programming but before the logic analyzer is started manually.
Enabling a Power-Up Trigger

A different Power-Up Trigger can be added to each logic analyzer instance in the SignalTap II Instance Manager. To enable the Power-Up Trigger for a logic analyzer instance, right-click the instance, and click Enable Power-Up Trigger, or select the instance, and on the Edit menu, click Enable Power-Up Trigger. To disable a Power-Up Trigger, click Disable Power-Up Trigger in the same locations. Power-Up Trigger is shown as a child instance below the name of the selected instance with the default trigger conditions set in the node list. Figure 12–17 shows the SignalTap II file window when a Power-Up Trigger is enabled.

Managing & Configuring Power-Up & Run-Time Trigger Conditions

When the Power-Up Trigger is enabled for a logic analyzer instance, you create basic and advanced trigger conditions for it in the same way you do with the regular trigger, also called the Run-Time Trigger. Power-Up Trigger conditions that you can adjust are color coded light blue, while Run-Time Trigger conditions remain white. Since each instance now has two sets of trigger conditions, the Power-Up Trigger and the Run-Time Trigger, you can differentiate between the two with the color coding. To switch between the trigger conditions of the Power-Up Trigger and the Run-Time Trigger, double-click the instance name or the Power-Up Trigger name in the Instance Manager.
When setting the trigger conditions for the Power-Up Trigger, you can only make changes that would not normally require recompilation when made in the Run-Time Trigger conditions. You cannot make changes that would require a full recompile, such as adding signals, deleting signals, or changing between basic and advanced triggers. To perform these actions, switch to the Run-Time Trigger conditions. However, any change made to the Power-Up Trigger conditions requires the SignalTap II Logic Analyzer to be recompiled even if such a change in the Run-Time Trigger conditions does not require a recompilation.

While creating or making changes to the trigger conditions for the Run-Time Trigger or the Power-Up Trigger, you may want to copy these conditions to the other trigger. This makes it easy to look for the same trigger during both power-up and run-time. To do this, right-click the instance name or the Power-Up Trigger name in the Instance Manager, and click Duplicate Trigger, or select the instance name or the Power-Up Trigger name and, on the Edit menu, click Duplicate Trigger. For information about running the SignalTap II Logic Analyzer instance with a Power-Up Trigger enabled, refer to “Running with a Power-Up Trigger” on page 12–47.

**Using Multiple Trigger Levels**

The multiple trigger level feature gives you precise control over the trigger conditions that you build. This feature enables you to give more complex data capture commands to the logic analyzer, providing greater accuracy and problem isolation. You can create up to ten trigger levels.

The SignalTap II Logic Analyzer first evaluates the trigger patterns associated with trigger level 1. When the expression for trigger level 1 evaluates to TRUE, the logic analyzer evaluates the expression for trigger level 2. This process continues until all trigger levels are processed and the final trigger level evaluates to TRUE. You can use the multiple trigger level feature with basic triggers, advanced triggers, or a mix of both.

Select the desired number of trigger levels in the Trigger Levels list when viewing Run-Time Trigger conditions. You cannot adjust the number of trigger levels when viewing a Power-Up Trigger. Switch to the Run-Time Trigger conditions to make this change. The number of Trigger levels is always the same between the Run-Time Trigger and a Power-Up Trigger. If you do not require an extra trigger level in either the Run-Time or Power-Up Triggers, disable the trigger level. To disable a level, turn off the desired Trigger Level column by clicking on the checkbox at the top of the column in the node list.
Specifying the Trigger Position

When using the circular buffer acquisition mode, you can specify the amount of data that is acquired before and after a trigger event. You can set the trigger position independently between a Run-Time and Power-Up Trigger. Select the desired ratio of pre-trigger data to post-trigger data by selecting one of the following ratios:

- **Pre**—This selection saves signal activity that occurred after the trigger (12% pre-trigger, 88% post-trigger).
- **Center**—This selection saves 50% pre-trigger and 50% post-trigger data.
- **Post**—This selection saves signal activity that occurred before the trigger (88% pre-trigger, 12% post-trigger).
- **Continuous**—This selection saves signal activity indefinitely (until stopped manually).

Using External Triggers

You can create a trigger input that allows you to trigger the SignalTap II Logic Analyzer from an external source. The analyzer can also supply a signal to trigger external devices or other SignalTap II instances. These features enable you to synchronize external logic analysis equipment with the internal logic analyzer. Power-Up Triggers can use the external triggers feature, but they must use the same source or target signal as their associated Run-Time Trigger.

**Trigger In**

To use Trigger In, perform the following steps:

1. In the **SignalTap II** window, click the **Setup** tab.
2. If a Power-Up Trigger is enabled, make sure you are viewing the Run-Time Trigger conditions.
3. In the Signal Configuration pane, turn on **Trigger In**.
4. In the **Pattern** list, select the condition you want to act as your trigger event. You can set this separately for a Run-Time or a Power-Up Trigger.
5. Click **Browse** next to the **Source** field in the Trigger In pane (Figure 12–19 on page 12–39). The **Node Finder** dialog box appears.
6. In the **Node Finder** dialog box, select the signal (either an input pin or an internal signal) that you want to drive the Trigger In source, and click **OK**.

**Trigger Out**

To use Trigger Out, perform the following steps:

1. In the **SignalTap II** dialog box, click the **Setup** tab.

2. If a Power-Up trigger is enabled, make sure you are viewing the Run-Time Trigger conditions.

3. In the Signal Configuration pane, turn on **Trigger Out**.

4. In the **Level** list, select the condition you want to signify that the trigger event is occurring. You can set this separately for a Run-Time or a Power-Up Trigger.

5. Click **Browse** next to the **Target** field in the Trigger Out pane (Figure 12–18). The **Node Finder** dialog box appears.

6. In the **Node Finder** dialog box, select the signal (either an output pin or an internal signal) that you want to drive the Trigger Out, and click **OK**.

**Using the Trigger Out of One Analyzer as the Trigger In of Another Analyzer**

An advanced feature of the SignalTap II Logic Analyzer is the ability to use the Trigger Out of one analyzer as the Trigger In to another analyzer. This feature allows you to synchronize and debug events that occur across multiple clock domains.

To perform this operation, first enable the **Trigger Out** of the first analyzer and specify the name for the Trigger Out signal (Figure 12–18).
Figure 12–18. Enabling the Trigger Out Signal
Next, turn on the **Trigger In** of the second analyzer, and specify the name of the Trigger In of the second analyzer as the Trigger Out of the first analyzer (Figure 12–19).

**Figure 12–19. Enabling the Trigger In Signal**

![Image showing the enabling of the Trigger In signal]

---

**Compile the Design**

When you add a SignalTap II file to your project, the SignalTap II Logic Analyzer becomes part of your design. Because of this, you must compile your project to incorporate the SignalTap II logic and enable the JTAG connection that is used to control the logic analyzer. When you are debugging with a traditional external logic analyzer, it is often necessary to make changes to the signals monitored as well as the trigger conditions. Since these types of adjustments often translate into recompilation time when using the SignalTap II Logic Analyzer, you can use the SignalTap II Incremental Compilation feature along with incremental compilation in the Quartus II software to reduce time spent recompiling.
Compiling without Incremental Compilation

Once you've configured your SignalTap II file and defined triggers, compile your project to incorporate the SignalTap II Logic Analyzer. On the Processing menu, click Start Compilation, or click Start Compilation on the toolbar to begin the compilation.

When you compile your design with a SignalTap II file, the sld_signaltap and sld_hub entities are automatically added to the compilation hierarchy. These two entities are the main components of the SignalTap II Logic Analyzer, providing the JTAG interface required for operation.

You can prevent full recompilations when incremental compilation is not used by using the SignalTap II incremental routing feature. With this feature, you add extra post-fitting nodes to the node list during the debugging process by reserving them ahead of time for incremental routing. You can also replace existing pre-synthesis nodes later with post-fitting nodes by enabling the pre-synthesis nodes for incremental routing.

For information about using the SignalTap II Incremental Routing feature, refer to the Quartus II Help.

Faster Compilations Using SignalTap II Incremental Compilation

SignalTap II Incremental Compilation enables you to preserve the synthesis and fitting results of your original design and add the SignalTap II Logic Analyzer to your design without recompiling your original source code. This feature is also useful when you want to modify the configuration of the SignalTap II file. For example, you can modify the buffer sample depth or memory type without performing a full compilation after the change is made. Only the SignalTap II Logic Analyzer, configured as its own design partition, needs to be recompiled.

To use SignalTap II Incremental Compilation, you must first enable Full Incremental Compilation for your design and assign design partitions. Once your design is set up to use full incremental compilation, you enable the SignalTap II Incremental Compilation function in the SignalTap II file (Figure 12–20). This turns the SignalTap II Logic Analyzer into its own separate design partition.
Enable Incremental Compilation for your Design

To enable Incremental Compilation, perform the following steps:

1. On the Assignments menu, click **Design Partitions window**.

2. In the **Incremental Compilation** list, select **Full Incremental Compilation**.

3. Create user-defined partitions and set the **Netlist Type** to **Post-fit**.

4. On the Processing menu, click **Start Compilation**, or click **Start Compilation** on the toolbar.

Your project is fully compiled the first time, establishing the design partitions you’ve created.

For more information on performing Incremental Compilation, refer to the *Quartus II Incremental Compilation for Hierarchical & Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*. 
Enable SignalTap II Incremental Compilation

To enable the SignalTap II Incremental Compilation, perform the following steps:

1. For each instance in your SignalTap II file, turn on **Incremental Compilation** in the Instance Manager.

   When you enable Incremental Compilation, all existing pre-synthesis signals are converted into post-fitting signals. You can use only post-fitting signals with the SignalTap II Incremental Compilation feature. Any pre-synthesis signals that do not have post-fitting equivalents or have not been preserved with synthesis attributes become invalid, indicated by the signal name color changing to red. Invalid signals must be removed from the node list before you can perform a successful compilation.

2. Add SignalTap II Post-Fitting nodes to your SignalTap II file.

3. On the Processing menu, click **Start Compilation**, or click **Start Compilation** on the toolbar.

   To verify that your original design was not modified, examine the messages in the Partition Merge section of the Compilation Report. Figure 12–21 shows an example of the messages displayed.

![Compilation Report Messages](image-url)
Unless you make changes to your design partitions that require recompilation, only the SignalTap II design partition is recompiled. If you make subsequent changes to only the SignalTap II file, only the SignalTap II design partition must be recompiled, reducing your recompilation time.

**Preventing Changes Requiring Recompilation**

You can configure the SignalTap II file to prevent changes that normally require a recompilation. You do this by setting a lock mode in the node list in the Setup tab. If you are not using incremental compilation, you can lock your configuration by choosing to allow only incremental routing changes or only trigger condition changes. With incremental compilation enabled, there are no incrementally routed nodes, so the only lock mode available prevents any configuration changes other than changes to the basic trigger conditions.

For more information about the use of lock modes, see Quartus II Help.

**Timing Preservation with the SignalTap II Logic Analyzer**

In addition to verifying functionality, timing closure is one of the most crucial processes in successfully completing a design. When you compile a project with a SignalTap II Logic Analyzer without the use of incremental compilation, you add IP to your existing design. Therefore, you can affect the existing placement, routing, and timing of your design. To minimize the effect that the SignalTap II Logic Analyzer has on your design, Altera recommends that you use incremental compilation for your project. With the SignalTap II Logic Analyzer in its own design partition, it has little to no affect on your design. If incremental compilation cannot be implemented in your design, back-annotate your design prior to inserting the SignalTap II Logic Analyzer. Back-annotation minimizes the impact of the logic analyzer on your design performance.

Besides back-annotating your design, you can use the following techniques to help maintain timing:

- Avoid adding critical path signals to your SignalTap II file.
- Minimize the number of signals that have Trigger Enable selected. By default, all of the signals that you add to the SignalTap II file have the Trigger Enable turned on. Turn off Trigger Enable for signals you do not plan to use as triggers.
- Use the Basic Trigger whenever possible. Using the Advanced Trigger increases the amount of logic, which may add extra delay to your circuit.
Minimize the number of combinational signals you add to your SignalTap II file, and add registers whenever possible.

Specify an $f_{\text{MAX}}$ constraint for each clock in your design.

Back-annotate your design prior to compiling with the SignalTap II Logic Analyzer.

For an example of timing preservation with the SignalTap II Logic Analyzer, refer to *Area & Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

### Program the Target Device(s)

Once your project including the SignalTap II Logic Analyzer is compiled, you must configure the FPGA target device. When you are using the SignalTap II Logic Analyzer for debugging, you configure the device from the SignalTap II file instead of the Quartus II Programmer. Because you configured from the SignalTap II file, you can open more than one SignalTap II file and program multiple devices to debug multiple designs simultaneously.

#### Programming a Single Device

To configure a single device for use with the SignalTap II Logic Analyzer perform the following steps:

1. In the JTAG Chain Configuration pane in the SignalTap II file window, select the connection you use to communicate with the device from the Hardware list. If you need to add your communication cable to the list, click Setup to configure your connection.

2. Browse to and select the SOF file that includes the SignalTap II Logic Analyzer in the JTAG Chain Configuration panel.

3. Click Scan Chain.

4. In the Device list, select the device to which you want to download the design.

5. Click the Program Device icon.

#### Programming Multiple Devices to Debug Multiple Designs

You can simultaneously debug multiple designs using one instance of the Quartus II software by performing the following steps:

1. Create, configure, and compile each project that includes a SignalTap II file.
2. Open each SignalTap II file.

   ![Tip Icon] You do not have to open a Quartus II project to open a SignalTap II file.

3. Use the **JTAG Chain Configuration** panel controls to select the target device in each SignalTap II file.

4. Program each FPGA.

5. Run each analyzer independently.

Figure 12–22 shows a JTAG chain and its associated SignalTap II files.

---

**Figure 12–22. JTAG Chain**

![JTAG Chain Diagram]
Run the SignalTap II Logic Analyzer

After the device is configured with your design that includes the SignalTap II Logic Analyzer, you can perform debugging operations in a manner similar to the use of an external logic analyzer. You “arm” the logic analyzer by starting an analysis. When your trigger event occurs, the captured data is stored in the memory buffer on the device and then transferred to the SignalTap II file over the JTAG connection. You can also perform the equivalent of a “force trigger” that lets you view the captured data currently in the buffer without a trigger event occurring. Figure 12–23 illustrates a flow that shows how you operate the SignalTap II Logic Analyzer. The flowchart indicates where Power-Up and Run-Time Trigger events occur and when captured data from these events is available for analysis.

Figure 12–23. Power-Up & Run-Time Trigger Events Flowchart
The SignalTap II toolbar in the Instance Manager has four options for running the analyzer:

- **Run Analysis**—The SignalTap II Logic Analyzer runs until the trigger event occurs. When the trigger event occurs, monitoring and data capture stops once the acquisition buffer is full.
- **AutoRun Analysis**—The SignalTap II Logic Analyzer continuously captures data until the **Stop Analysis** button is clicked, ignoring all trigger event conditions.
- **Stop Analysis**—SignalTap II analysis stops. The acquired data does not appear automatically if the trigger event has not occurred.
- **Read Data**—Captured data is displayed. This button is useful if you want to view the acquired data even if the trigger has not occurred.

### Running with a Power-Up Trigger

If you have enabled and set up a Power-Up Trigger for an instance of the SignalTap II Logic Analyzer, the captured data may already be available for viewing if the trigger event occurred after device configuration. To download the captured data or to check if the Power-Up Trigger is still running, click **Run Analysis** in the Instance Manager. If the Power-Up Trigger occurred, the logic analyzer immediately stops, and the captured data is downloaded from the device. The data can now be viewed on the **Data** tab of the SignalTap II file window. If the Power-Up Trigger did not occur, no captured data is downloaded, and the logic analyzer continues to run. You can wait for the Power-Up Trigger event to occur, or, to stop the logic analyzer, click **Stop Analysis**.

### Running with Run-Time Triggers

You can arm and run the SignalTap II Logic Analyzer manually after device configuration to capture data samples based on the Run-Time Trigger. You can do this immediately if there is no Power-Up Trigger enabled. If a Power-Up Trigger is enabled, you can do this after the Power-Up Trigger data is downloaded from the device or once the logic analyzer is stopped because the Power-Up Trigger event did not occur. Click **Run Analysis** in the SignalTap II window to start monitoring for the trigger event. You can start multiple SignalTap II instances at the same time by selecting all of the required instances before you click **Run Analysis** on the toolbar.

Unless the logic analyzer is stopped manually, data capture begins when the trigger event evaluates to **true**. When this happens, the captured data is downloaded from the buffer. You can view the data in the **Data** tab of the SignalTap II file window.
Performing a Force Trigger

Sometimes when you use an external logic analyzer or oscilloscope, you want to see the current state of signals without setting up or waiting for a trigger event to occur. This is referred to as a “force trigger” operation because you are forcing the test equipment to capture data without regard to any set trigger conditions. With the SignalTap II Logic Analyzer, you can choose to run the analyzer and capture data immediately or run the analyzer and capture data when you want.

To run the analyzer and immediately capture data, disable the trigger conditions in all trigger levels by turning off each Trigger Level column in the node list. This operation does not require a recompilation. Click Run Analysis in the Instance Manager. The SignalTap II Logic Analyzer immediately triggers, captures, and downloads the data to the Data tab of the SignalTap II file window. If the data does not download automatically, click Read Data in the Instance Manager.

If you want to choose when to capture data manually, it is not required that you disable the trigger conditions. Click Autorun Analysis to start the logic analyzer, and click Stop Analysis to capture data. If the data does not download to the Data tab of the SignalTap II file window automatically, click Read Data.

Finally, you can choose to capture data manually after a trigger event has occurred. This is useful if you still want the trigger event to occur, but you want to capture data about the signals at some point after the trigger without capturing the trigger event itself. To do this, set the Buffer acquisition mode to Circular and Continuous, and click Run Analysis. When the trigger event occurs, the status in the SignalTap II Health Monitor is shown as Acquiring post-trigger data, but the logic analyzer does not stop. When you want to capture and download the data, click Stop Analysis. If the data does not download automatically, click Read Data.
SignalTap II Status Messages

Table 12–6 describes the text messages that may appear in the SignalTap II Health Monitor in the Instance Manager before, during, and after a data acquisition. Use these messages to know the state of the logic analyzer or what operation it is performing.

<table>
<thead>
<tr>
<th>Message</th>
<th>Message Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Not running</td>
<td>The SignalTap II Logic Analyzer is not running. There is no connection to a device or the device is not configured.</td>
</tr>
<tr>
<td>(Power-Up Trigger) Waiting for clock (1)</td>
<td>The SignalTap II Logic Analyzer is performing a Run-Time or Power-Up Trigger acquisition and is waiting for the clock signal to transition.</td>
</tr>
<tr>
<td>Acquiring (Power-Up) pre-trigger data (1)</td>
<td>The trigger condition has not been evaluated yet. A full buffer of data is collected if the circular buffer acquisition mode is selected.</td>
</tr>
<tr>
<td>Trigger In conditions met</td>
<td>Trigger In condition has occurred. The SignalTap II Logic Analyzer is waiting for the condition of the first trigger level to occur. This can appear if Trigger In is specified.</td>
</tr>
<tr>
<td>Waiting for (Power-up) trigger (1)</td>
<td>The SignalTap II Logic Analyzer is now waiting for the trigger event to occur.</td>
</tr>
<tr>
<td>Trigger level &lt;x&gt; met</td>
<td>The condition of trigger level x has occurred. The SignalTap II Logic Analyzer is waiting for the condition specified in level x+1 to occur.</td>
</tr>
<tr>
<td>Acquiring (power-up) post-trigger data (1)</td>
<td>The whole trigger event has occurred. The SignalTap II Logic Analyzer is acquiring the post-trigger data. The amount of post-trigger data collected is user-defined between 12%, 50%, and 88% when the circular buffer acquisition mode is selected.</td>
</tr>
<tr>
<td>Offload acquired (Power-Up) data (1)</td>
<td>Data is being transmitted to the Quartus II software through the JTAG chain.</td>
</tr>
<tr>
<td>Ready to acquire</td>
<td>The SignalTap II Logic Analyzer is waiting for the user to arm the analyzer.</td>
</tr>
</tbody>
</table>

Note to Table 12–6:
(1) This message can appear for both Run-Time and Power-Up Trigger events. When referring to a Power-Up Trigger, the text in parentheses is added.

In segmented acquire mode, pre-trigger and post-trigger do not apply.
View, Analyze & Use Captured Data

Once a trigger event has occurred or you capture data manually, you can use the SignalTap II interface to examine the data, and use your findings to help debug your design. The SignalTap II Logic Analyzer provides a number of features that makes it easy to do this.

Viewing Captured Data

You can view captured SignalTap II data in the Data tab of the SignalTap II file (Figure 12–24). Each row of the Data tab displays the captured data for one signal or bus. Buses can be expanded to show the data for each individual signal on the bus. Click on the data waveforms to zoom in on the captured data samples, and right-click to zoom out.

Figure 12–24. Captured SignalTap II Data

When you are viewing captured data, it is often useful to know the time interval between two events. Time bars enable you to see the number of clock cycles between two samples of captured data in your system. There are two types of time bars:

- **Master Time Bar**—The master time bar’s label displays the absolute time of its location in bold. The master time bar is a thick black line in the Data tab. The captured data has only one master time bar.
- **Reference Time Bar**—The reference time bar’s label displays the time relative to the master time bar. You can create an unlimited number of reference time bars.

To help you find a transition of signals relative to the master time bar location, use either the Next Transition or the Previous Transition button. This lines the master time bar up with the next or previous
transition of a selected signal or group of selected signals. This feature is very useful when the sample depth is very large and the rate at which signals toggle is very low.

Creating Mnemonics for Bit Patterns

The mnemonic table feature allows you to assign a meaningful name to a set of bit patterns, such as a bus. To create a mnemonic table, right-click in the Setup or Data tab of a SignalTap II file, and click Mnemonic Table Setup. You create a mnemonic table by entering sets of bit patterns and specifying a label to represent each pattern. Once you have created a mnemonic table, you assign it to a group of signals. To assign a mnemonic table, right-click on the group, click Bus Display Format, and select the desired mnemonic table.

Automatic Mnemonics with a Plug-In

When you use a plug-in to add signals to a SignalTap II file, mnemonic tables for the added signals are automatically created and assigned to the signals defined in the plug-in. If you ever need to manually enable these mnemonic tables, right-click on the name of the signal or signal group. On the Bus Display Format submenu, click the name of the mnemonic table that matches the plug-in.

Locating a Node in the Design

When you find the source of a bug in your design using the SignalTap II Logic Analyzer, you can use the node locate feature to locate that signal in many of the tools found in the Quartus II software, as well as in your design files. This lets you find the source of the problem quickly so you can modify your design to correct the flaw. To locate a signal from the SignalTap II Logic Analyzer in one of the Quartus II software tools or your design files, right-click on the signal in the SignalTap II file, and click Locate in <tool name>. You can locate a signal from the node list in any of the following locations:

- Assignment Editor
- Pin Planner
- Timing Closure Floorplan
- Chip Editor
- Resource Property Editor
- Technology Map Viewer
- RTL Viewer
- Design File

For more information on using these tools, refer to the appropriate chapters in the Quartus II Handbook.
Saving Captured Data

The data log shows the history of captured data and the triggers used to capture the data. The analyzer acquires data, stores it in a log, and displays it as waveforms. When the logic analyzer is in auto-run mode and a trigger event occurs more than once, captured data for each time the trigger occurred is stored as a separate entry in the data log. This makes it easy to go back and review the captured data for each trigger event. The default name for a log is based on the time when the data was acquired. Altera recommends that you rename the data log with a more meaningful name.

The logs are organized in a hierarchical manner; similar logs of captured data are grouped together in trigger sets. To enable data logging, turn on the checkbox in the Data Log of the SignalTap II file. To recall a data log for a given trigger set and make it active, double-click the name of the data log in the list.

The Data Log feature is useful for organizing different sets of trigger conditions and different sets of signal configurations. Refer to "Managing Multiple SignalTap II Files & Configurations" on page 12–26.

Converting Captured Data to Other File Formats

You can export captured data in the following file formats, some of which can be used with other EDA simulation tools:

- Comma Separated Values File (.csv)
- Table File (.tbl)
- Value Change Dump File (.vcd)
- Vector Waveform File (.vwf)
- Graphics format files (.jpg, .bmp)

To export the SignalTap II Logic Analyzer's captured data, on the File menu, click Export and specify the File Name, the Export Format, and the Clock Period.
Creating a SignalTap II List File

Captured data can also be viewed in a SignalTap II list file. A SignalTap II list file is a text file that lists all the data captured by the logic analyzer for a trigger event. Each row of the list file corresponds to one captured sample in the buffer. Columns correspond to the value of each of the captured signals or signal groups for that sample. If a mnemonic table was created for the captured data, the numerical values in the list are replaced with a matching entry from the table. This is especially useful with the use of a plug-in that includes instruction code disassembly. You can immediately see the order by which the instruction code was executed around the time of the trigger event. To create a SignalTap II list file, on the File menu, select Create/Update, and click Create SignalTap II List File.

Other Features

The SignalTap II Logic Analyzer has a number of other features that do not necessarily belong to a particular task in the task flow.

Using the SignalTap II MATLAB MEX Function to Capture Data

If you use MATLAB for DSP design, you can call the MATLAB MEX function alt_signaltap_run, built into the Quartus II software, to acquire data from the SignalTap II Logic Analyzer directly into a matrix in the MATLAB environment. If you use the MEX function repeatedly in a loop, you can perform as many acquisitions as you can when using SignalTap II in the Quartus II software environment in the same amount of time.

The SignalTap II MATLAB MEX function is available only in the Windows version of the Quartus II software.

To set up the Quartus II software and the MATLAB environment to perform SignalTap II acquisitions, perform the following steps:

1. In the Quartus II software, create a SignalTap II file.

2. In the node list in the Data tab of the SignalTap II file window, organize the signals and groups of signals into the order in which you want them to appear in the MATLAB matrix. Each row of the imported matrix represents a single SignalTap II acquisition sample, while each column represents a signal or group of signals in the order they are organized in the Data tab.
Signal groups acquired into the MATLAB environment with the MEX function are limited to a width of 32 bits. If you want to use the MEX function with a bus or signal group that is more than 32 bits wide, split the group up into smaller groups that do not exceed the 32 signal limit.

3. Save the SignalTap II file and compile your design. Program your device and run the SignalTap II Logic Analyzer to make sure your trigger conditions and signal acquisition are working correctly.

4. In the MATLAB environment, add the Quartus II binary directory to your path with the following command:

   addpath `<Quartus install directory>`\win

   You can view the help file for the MEX function by entering `alt_signaltap_run` in MATLAB without any operators.

   You use the MEX function in the MATLAB environment to open the JTAG connection to the device and run the SignalTap II Logic Analyzer to acquire data. When you finish acquiring data, you must close the connection.

   To open the JTAG connection and begin acquiring captured data directly into a MATLAB matrix called .stp, use the following command:

   ```plaintext
   stp = alt_signaltap_run('<<stp filename>',['signed' | 'unsigned'], '<instance names>',
   '<signalset name>', '<trigger name>');
   ```

   When capturing data, you want to use a SignalTap II file named `<stp filename>`. This is required for using the MEX function. The other MEX function options are defined in Table 12–7.

### Table 12–7. SignalTap II MATLAB MEX Function Options (Part 1 of 2)

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>signed</td>
<td>'signed'</td>
<td>The <code>signed</code> option turns signal group data into two's complement signed integers. The most significant bit of the group as defined in the SignalTap II Data tab is the sign bit. The <code>unsigned</code> option keeps the data as an unsigned integer. The default is <code>signed</code>.</td>
</tr>
<tr>
<td>unsigned</td>
<td>'unsigned'</td>
<td></td>
</tr>
</tbody>
</table>

Add the Quartus II binary directory to your MATLAB path with the following command:

```plaintext
addpath `<Quartus install directory>`\win
```
You can enable or disable verbose mode to see the status of the logic analyzer while it is acquiring data. To enable or disable verbose mode, use the following commands:

```
alt_signaltap_run('VERBOSE_ON');
alt_signaltap_run('VERBOSE_OFF');
```

When you finish acquiring data, you must close the JTAG connection. Use the following command to close the connection:

```
alt_signaltap_run('END_CONNECTION');
```

For more information about the use of MEX functions in MATLAB, refer to the MATLAB Help.

### Using SignalTap II in a Lab Environment

You can install a stand-alone version of the SignalTap II Logic Analyzer. This version is particularly useful in a lab environment where you do not have a workstation that meets the requirements for a complete Quartus II installation, or if you do not have a license for a full installation of the Quartus II software. The stand-alone version of the SignalTap II Logic Analyzer is included with the Quartus II stand-alone Programmer and is available from the Downloads page of the Altera web site, www.altera.com.

### Remote Debugging Using the SignalTap II Logic Analyzer

You can use the SignalTap II Logic Analyzer to debug a design that is running on a device attached to a PC in a remote location.

To perform a remote debugging session, you must have the following setup:

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;instance name&gt;</td>
<td>'auto_signaltap_0'</td>
<td>Specify a SignalTap II instance if more than one instance is defined. The default is the first instance in the SignalTap II file, auto_signaltap_0.</td>
</tr>
<tr>
<td>&lt;signal set name&gt; &lt;trigger name&gt;</td>
<td>'my_signalset' 'my_trigger'</td>
<td>Specify the signal set and trigger from the SignalTap II data log if multiple configurations are present in the SignalTap II file. The default is the active signal set and trigger in the file.</td>
</tr>
</tbody>
</table>
Equipment Setup

On the PC, in the remote location, install the stand-alone version of the SignalTap II Logic Analyzer. This remote computer must have Altera programming hardware connected, such as the EthernetBlaster or USB-Blaster.

On the local PC, install the full version of the Quartus II software. This local PC must be connected to the remote PC across a LAN with the TCP/IP protocol.

Software Setup on the Remote PC

To setup the software on the remote PC, perform the following steps:

1. In the Quartus II programmer, click **Hardware Setup**.

2. Click the **JTAG Settings** tab (**Figure 12–25**).

**Figure 12–25. Configure JTAG on Remote PC**
3. Click Configure local JTAG server.

4. In the Configure Local JTAG Server dialog box (Figure 10–25), turn on Enable remote clients to connect to the local JTAG server, and type your password in the password box. Type your password again in the Confirm Password box and click OK.

---

**Figure 12–26. Configure Local JTAG Server on Remote**

---

**Software Setup on the Local PC**

To set up your software on your local PC, perform the following steps:

1. Launch the Quartus II programmer.

2. Click Hardware Setup.

3. On the JTAG settings tab, click Add server.

4. In the Add Server dialog box (Figure 12–27), type the network name or IP address of the server you want to use and the password for the JTAG server that you created on the remote PC.

---

**Figure 12–27. Add Server Dialog Box**

---

5. Click OK.
SignalTap II Setup on the Local PC

To connect to the hardware on the remote PC, perform the following steps:

1. Click the **Hardware Setup** tab and select the hardware on the remote PC (Figure 12–28).

![Figure 12–28. Selecting Hardware on Remote PC](image)

2. Click **Close**.

SignalTap II Scripting Support

You can run procedures and make settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II Command-Line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp
```
The *Quartus II Software Command-Line Operation & TCL Scripting Manual* includes the same information in PDF form. For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. Refer to the *Quartus II Settings File Reference Manual* for information about all settings and constraints in the Quartus II software. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

**SignalTap II Command Line Options**

To compile your design with the SignalTap II Logic Analyzer using the command prompt, you must use the `quartus_stp` command. *Table 10–8* shows the options that help you better understand how to use the `quartus_stp` executable.

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>stp_file</code></td>
<td><code>quartus_stp --stp_file &lt;stp_filename&gt;</code></td>
<td>Assigns the specified SignalTap II file to the <code>USE_SIGNALTAP_FILE</code> in the Quartus II Settings File (QSF).</td>
</tr>
<tr>
<td><code>enable</code></td>
<td><code>quartus_stp --enable</code></td>
<td>Creates assignments to the specified SignalTap II file in the QSF, and changes <code>ENABLE_SIGNALTAP</code> to ON. The SignalTap II Logic Analyzer is included in your design the next time the project is compiled. If no SignalTap II file is specified in the QSF, the <code>--stp_file</code> option must be used. If the <code>--enable</code> option is omitted, the current value of <code>ENABLE_SIGNALTAP</code> in the QSF is used.</td>
</tr>
<tr>
<td><code>disable</code></td>
<td><code>quartus_stp --disable</code></td>
<td>Removes the SignalTap II file reference from the QSF and changes <code>ENABLE_SIGNALTAP</code> to OFF. The SignalTap II Logic Analyzer is removed from the design database the next time you compile your design. If the <code>--disable</code> option is omitted, the current value of <code>ENABLE_SIGNALTAP</code> in the QSF is used.</td>
</tr>
</tbody>
</table>
The following example illustrates how to compile a design with the SignalTap II Logic Analyzer at the command line:

```
quartus_stp filtref --stp_file stp1.stp --enable
quartus_map filtref --source=filtref.bdf --family=CYCLONE
quartus_fit filtref --part=EP1C12Q240C6 --fmax=80MHz --tsu=8ns
quartus_tan filtref
quartus_asm filtref
quartus_stp filtref --verify_connections
```

The `quartus_stp --stp_file stp1.stp --enable` command creates the QSF variable and instructs the Quartus II software to compile the `stp1.stp` file with your design.

The `quartus_stp --verify_connections` command must be run after the `quartus_fit` command. The `--verify_connections` option verifies that all signals in the SignalTap II file were routed correctly to the logic analyzer.

### Table 12–8. SignalTap II Command-Line Options (Part 2 of 2)

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>verify_connections</td>
<td><code>quartus_stp --verify_connections</code></td>
<td>Once a compilation with SignalTap II Logic Analyzer is complete, you must use this option to ensure that all signals that you wanted to tap in your design were properly connected to the logic analyzer.</td>
</tr>
<tr>
<td>create_signaltap_hdl_file</td>
<td><code>quartus_stp --create_signaltap_hdl_file</code></td>
<td>Creates a SignalTap II file representing the SignalTap II instance in the design generated by the SignalTap II Logic Analyzer megafunction created with the MegaWizard Plug-in Manager. The file is based on the last compilation. You must use the <code>--stp_file</code> option to properly create a SignalTap II file. Analogous to Create SignalTap II File from Design Instance(s) command in the Quartus II software.</td>
</tr>
</tbody>
</table>
Use the following example command to create a new SignalTap II file after building the SignalTap II Logic Analyzer instance with the MegaWizard Plug-In Manager:

```
quartus_stp filtref --create_signaltap_hdl_file --stp_file stp1.stp
```

For information on the other command line executables and options refer to the Command-Line Scripting chapter in volume 2 of the Quartus II Handbook.

**SignalTap II Tcl Commands**

The `quartus_stp` executable supports a Tcl interface that allows you to capture data without running the Quartus II GUI. To run a Tcl file that has SignalTap II Tcl commands, use the following command:

```
quartus_stp -t <Tcl file>
```

Table 12–9 shows the Tcl commands that you can use with SignalTap II.

<table>
<thead>
<tr>
<th>Command</th>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>open_session</td>
<td>--name &lt;stp_filename&gt;</td>
<td>Opens the specified SignalTap II file. All captured data is stored in this file.</td>
</tr>
<tr>
<td>run</td>
<td>--instance &lt;instance_name&gt;</td>
<td>Starts the analyzer. This command must be followed by all the required arguments to properly start the analyzer. You can optionally specify the name of the data log you want to create. If the Trigger condition is not met, you can specify a timeout value to stop the analyzer.</td>
</tr>
<tr>
<td></td>
<td>--signal_set &lt;signal_set&gt; (optional)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>--trigger &lt;trigger_name&gt; (optional)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>--data_log &lt;data_log_name&gt; (optional)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>--timeout &lt;seconds&gt; (optional)</td>
<td></td>
</tr>
<tr>
<td>run_multiple_start</td>
<td>None</td>
<td>Defines the start of a set of run commands. Use this command when multiple instances of data acquisition are started simultaneously. Add this command before the set of run commands that specify data acquisition. You must use this command with the run_multiple_end command. If the run_multiple_end command is not included, the run commands will not execute.</td>
</tr>
</tbody>
</table>
For more information on SignalTap II Tcl commands, refer to the Quartus II Help.

The following example is an excerpt from a script that is used to continuously capture data. Once the trigger condition is met, the data is captured and stored in the data log.

```
#opens signaltap session
open_session -name stp1.stp
#start acquisition of instance auto_signaltap_0 and auto_signaltap_1 at the same time
#calling run_multiple_end will start all instances
#run after run_multiple_start call
run_multiple_start
run -instance auto_signaltap_0 -signal_set signal_set_1 -trigger /trigger_1 -data_log log_1 -timeout 5
run -instance auto_signaltap_1 -signal_set signal_set_1 -trigger /trigger_1 -data_log log_1 -timeout 5
run_multiple_end
#close signaltap session
close_session
```

Once the script is completed, you should open the SignalTap II file that you used to capture data to examine the contents of the Data log.

### Table 12–9. SignalTap II Tcl Commands (Part 2 of 2)

<table>
<thead>
<tr>
<th>Command</th>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>run_multiple_end</td>
<td>None</td>
<td>Defines the end of a set of run commands. Use this command when multiple instances of data acquisition are started simultaneously. Add this command after the set of run_commands.</td>
</tr>
<tr>
<td>stop</td>
<td>None</td>
<td>Stops data acquisition</td>
</tr>
<tr>
<td>close_session</td>
<td>None</td>
<td>Closes the currently open SignalTap II file. You cannot run the analyzer after the SignalTap II file is closed.</td>
</tr>
</tbody>
</table>
Design Example: Using SignalTap II Logic Analyzers in SOPC Builder Systems

Altera Application Note, AN 323: Using SignalTap II Embedded Logic Analyzers in SOPC Builder Systems describes how to use the SignalTap II Logic Analyzer to monitor signals located inside a system module generated by SOPC Builder. The system in this example contains many components, including a Nios processor, a direct memory access (DMA) controller, on-chip memory, and an interface to external SDRAM memory. In this example, the Nios processor executes a simple C program from on-chip memory and waits for a button push. After a button is pushed, the processor initiates a DMA transfer, which you analyze using the SignalTap II Logic Analyzer.

For more information on this example, refer to AN 323: Using SignalTap II Embedded Logic Analyzers in SOPC Builder Systems which is available on the Literature page of the Altera website at www.altera.com.

Conclusion

As the FPGA industry continues to make technological advancements, outdated methodologies need to be replaced with new technologies that maximize productivity. The SignalTap II Logic Analyzer gives you the same benefits as a traditional logic analyzer, without the many shortcomings of a piece of dedicated test equipment. This version of the SignalTap II Logic Analyzer provides many new and innovative features that allow you to capture and analyze internal signals in your FPGA, allowing you to find the source of a design flaw in the shortest amount of time.