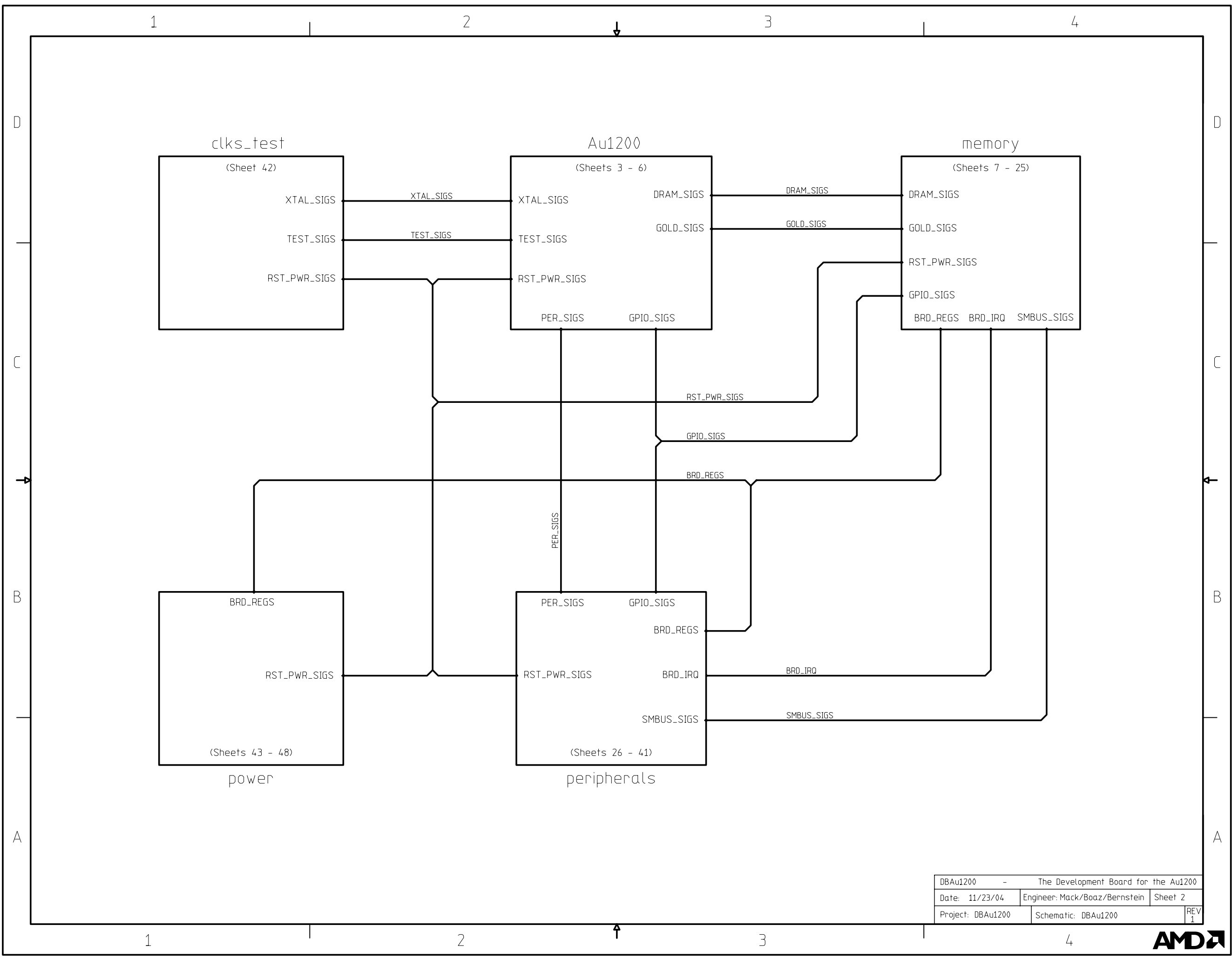


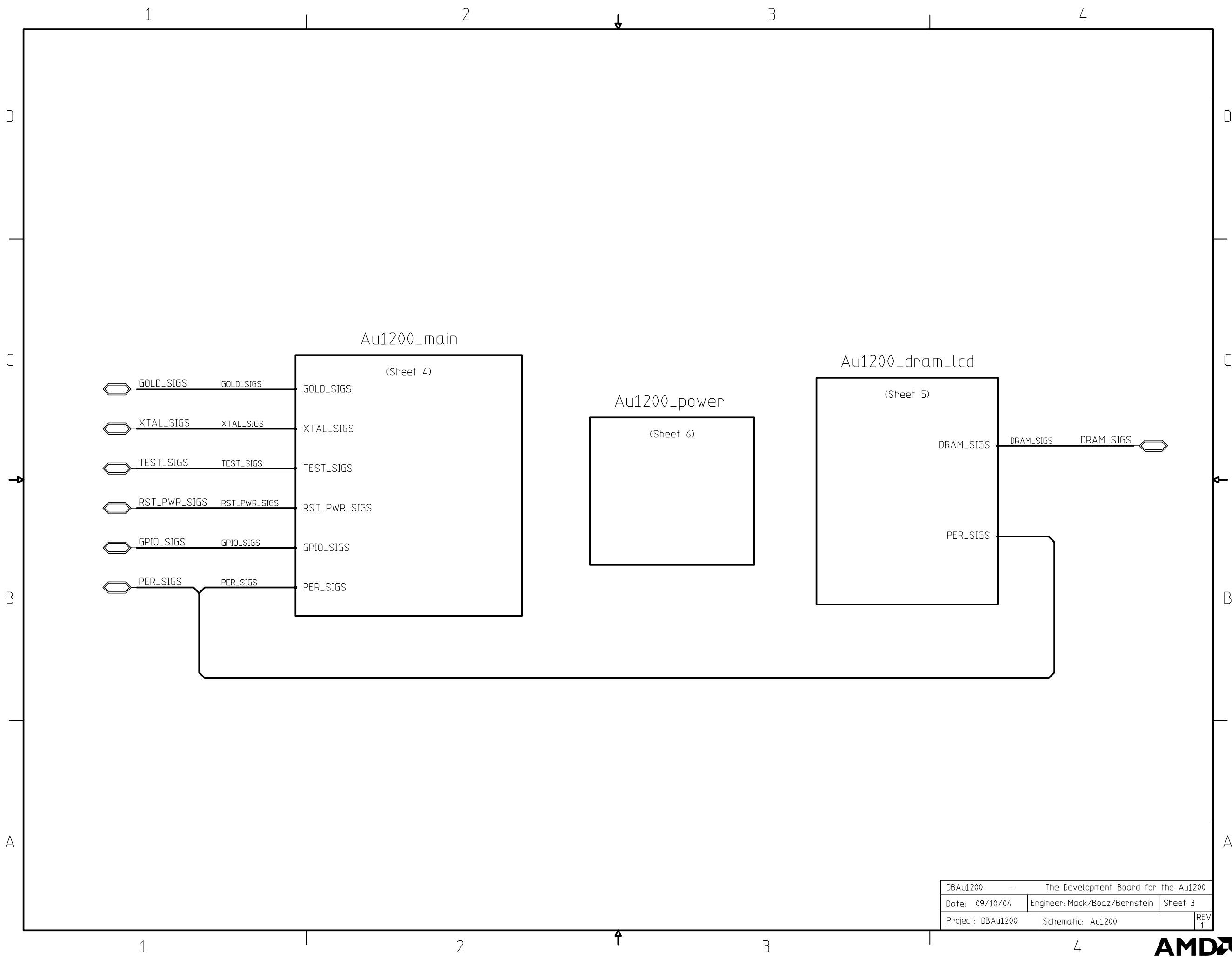
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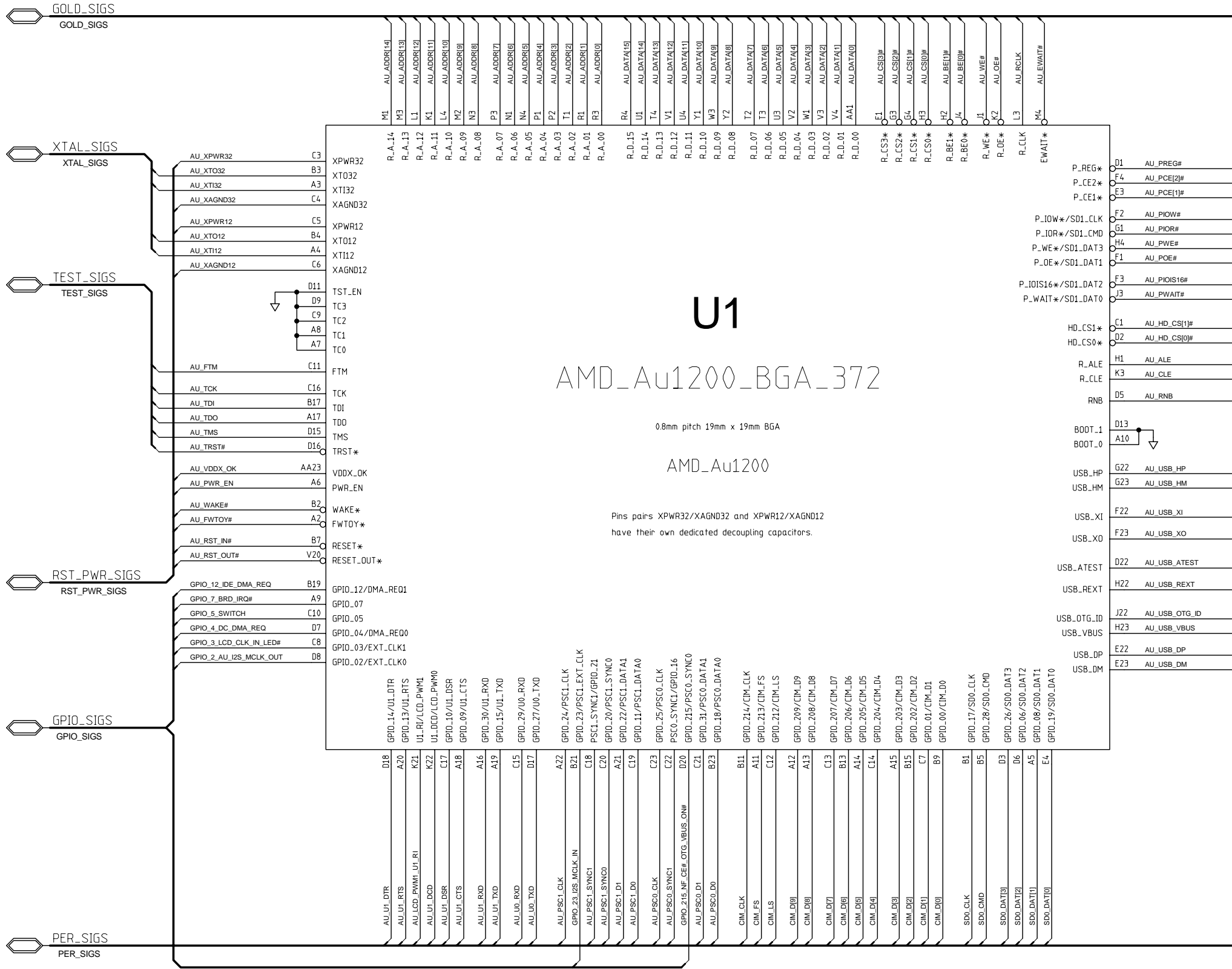
DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 2
Project: DBAu1200	Schematic: DBAu1200	REV 1





DBAu1200 - The Development Board for the Au1200	
Date: 09/10/04	Engineer: Mack/Boaz/Bernstein Sheet 3
Project: DBAu1200	Schematic: Au1200
	REV 1





R11
3.4Kohms
1% 125mW

DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: Au1200_main
Sheet 4	
REV 1	



1

2

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4

D

D

C

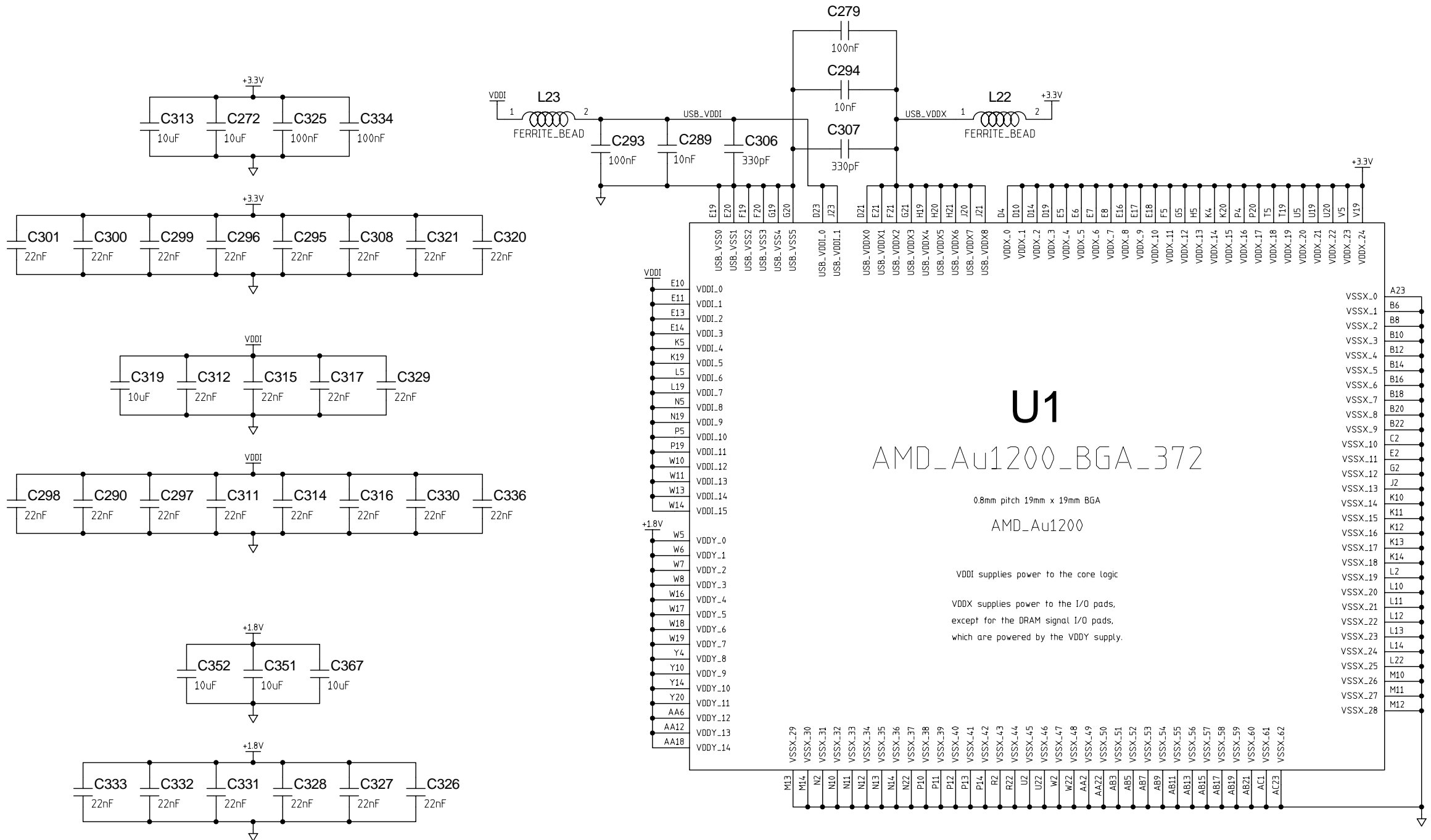
C

B

B

A

A



U1
 AMD_Au1200_BGA_372

0.8mm pitch 19mm x 19mm BGA

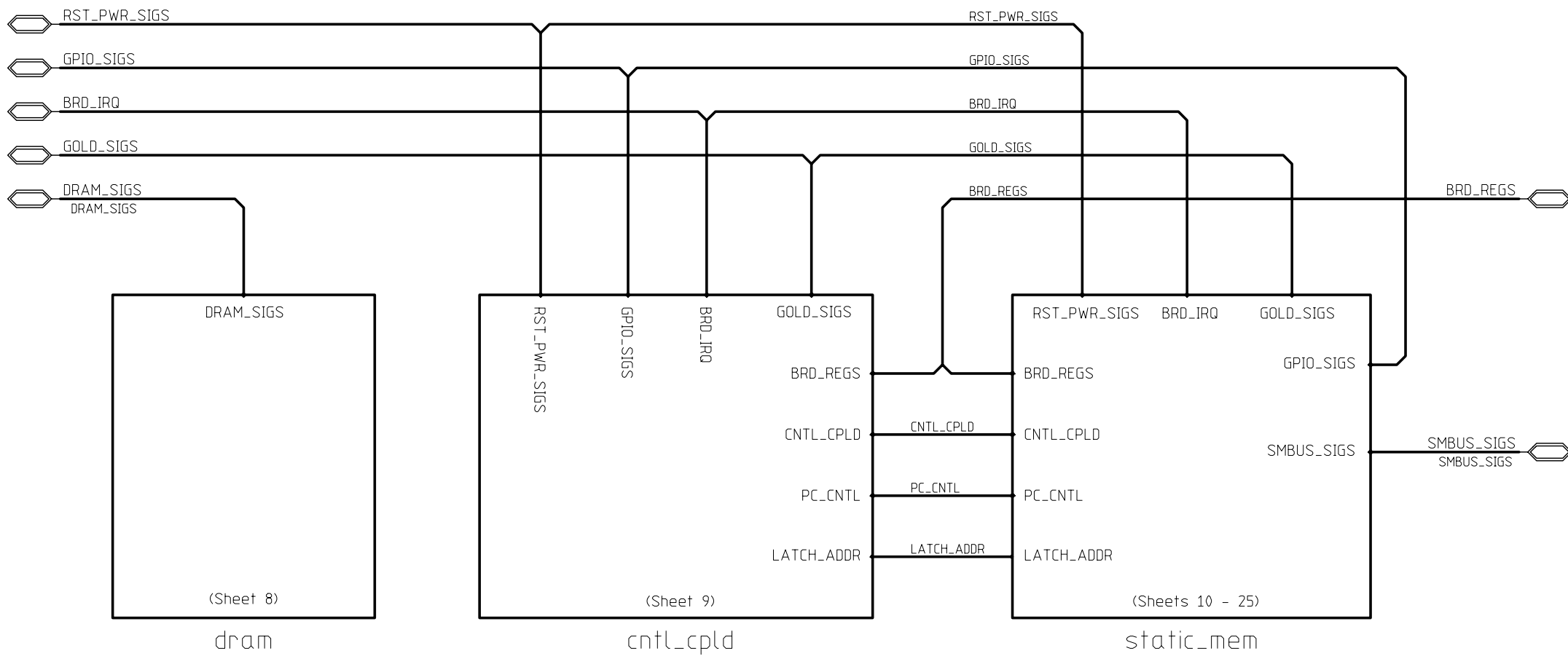
AMD_Au1200

VDDI supplies power to the core logic

VDDX supplies power to the I/O pads, except for the DRAM signal I/O pads, which are powered by the VDDY supply.

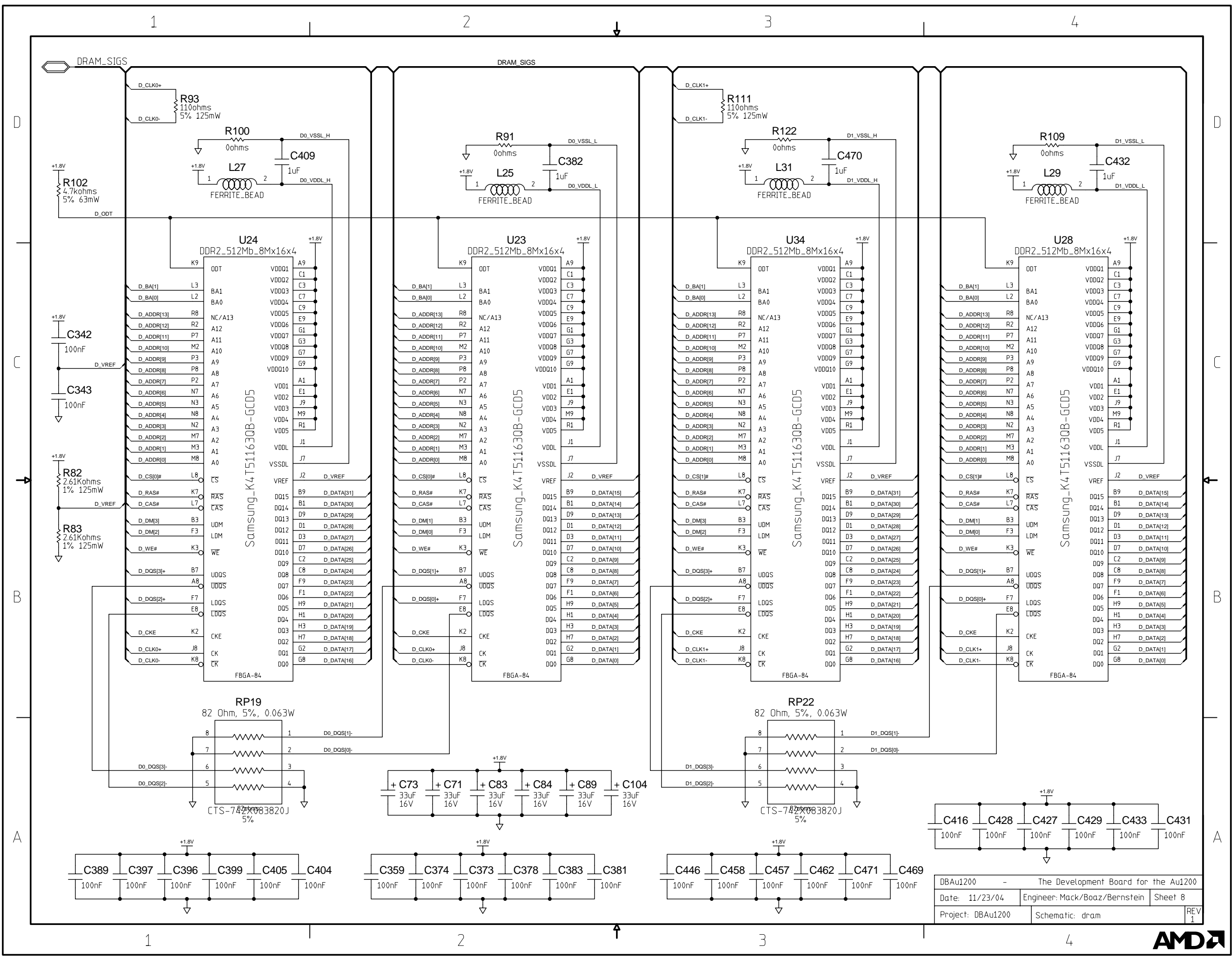
DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 6
Project: DBAu1200	Schematic: Au1200_power	REV 1





DBAu1200 - The Development Board for the Au1200			
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 7	
Project: DBAu1200	Schematic: memory	REV	1





DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 8
Project: DBAu1200	Schematic: dram	REV 1



1

2

3

4

CNTL_CPLD

CNTL_CPLD

PC_CNTL

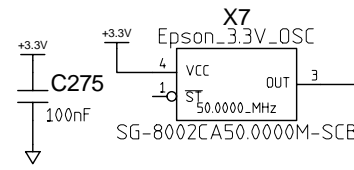
PC_CNTL

GOLD_SIGS

GOLD_SIGS

RST_PWR_SIGS

RST_PWR_SIGS



LATCH_ADDR LATCH_ADDR

GPIO_SIGS

+3.3V

RP16

10kohms

5%

CPLD_TMS

+3.3V

R73

10kohms

5% 63mW

CPLD_TDO_REG

+3.3V

R5

10kohms

5% 63mW

CPLD_TDO_CNTL_TDI_REG

+3.3V

RP16

10kohms

5%

CPLD_TDI_CNTL

+3.3V

RP16

10kohms

5%

CPLD_TCK

J7

Stake_Pins_1x7_w03

Samtec_TSM-107-01-L-SV-003

1

2

3

4

5

6

7

CPLD_TCK

CPLD_TMS

CPLD_TDI_CNTL

CPLD_TDO_REG

C243

10uF

+3.3V

BRD_REGS

GPIO_SIGS

GOLD_SIGS

LATCH_ADDR[28]

LATCH_ADDR[27]

LATCH_ADDR[26]

LATCH_ADDR[25]

LATCH_ADDR[24]

LATCH_ADDR[23]

LATCH_ADDR[22]

LATCH_ADDR[21]

AU_CS[3]#

AU_CS[2]#

AU_CS[1]#

AU_CS[0]#

AU_BE[1]#

AU_BE[0]#

AU_OE#

AU_WE#

AU_EWAIT#

AU_ALE

AU_CLE

AU_HD_CS[1]#

AU_HD_CS[0]#

AU_PCE[2]#

AU_PCE[1]#

AU_PWAIT#

AU_PIOIS16#

AU_POE#

BRD_REGS

BRD_REGS

TP4

SMT

CLK50

+3.3V

VCC1

VCC2

VCC3

VCC102.1

VCC102.2

VCC102.3

VCC102.4

GCK2_FB2_MC15

COMST_FB2_MC15

GCK1_FB2_MC14

GCK0_FB2_MC13

FB2_MC12

FB2_MC11

FB2_MC6

FB2_MC5

FB2_MC4

FB2_MC3

FB2_MC2

FB2_MC1

VCC1

VCC2

VCC3

FB1_MC1

FB1_MC2

FB1_MC3

FB1_MC4

FB1_MC5

FB1_MC6

FB1_MC11

FB1_MC12

FB1_MC13

FB1_MC14

FB1_MC15

FB1_MC16

FB3_MC1

GTS3_FB3_MC2

GTS2_FB3_MC3

GSR_FB3_MC4

FB3_MC5

FB3_MC6

FB3_MC7

FB3_MC11

FB3_MC12

FB3_MC13

FB3_MC14

FB3_MC15

FB3_MC16

FB7_MC16

FB7_MC15

FB7_MC14

FB7_MC13

FB7_MC12

FB7_MC11

FB7_MC7

FB7_MC6

FB7_MC5

FB7_MC4

FB7_MC3

FB7_MC2

FB7_MC1

FB5_MC16

FB5_MC15

FB5_MC14

FB5_MC13

FB6_MC12

FB6_MC11

FB6_MC6

FB6_MC5

FB6_MC4

FB6_MC3

FB6_MC2

FB6_MC1

AU_PWE#

AU_PIOR#

AU_PIOIW#

GPIO_12_IDE_DMA_REG

DC_IDI[8]

DC_IDI[2]

DC_IDI[1]

VALUX

CPLD_TDI_CNTL

CPLD_TMS

CPLD_TCK

CPLD_TDO_CNTL_TDI_REG

DC_IDI[0]

DC_WAIT#

SWAP_BOOT

PCI_ADDR_OE#

PCI_CD[2]#

PCI_CD[1]#

PCI_DHIGH_OE#

PCI_DLOW_OE#

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14

FB5_MC15

FB5_MC16

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14

FB5_MC15

FB5_MC16

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14

FB5_MC15

FB5_MC16

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14

FB5_MC15

FB5_MC16

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14

FB5_MC15

FB5_MC16

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14

FB5_MC15

FB5_MC16

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14

FB5_MC15

FB5_MC16

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14

FB5_MC15

FB5_MC16

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14

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FB5_MC16

FB5_MC1

FB5_MC2

FB5_MC3

FB5_MC4

FB5_MC5

FB5_MC6

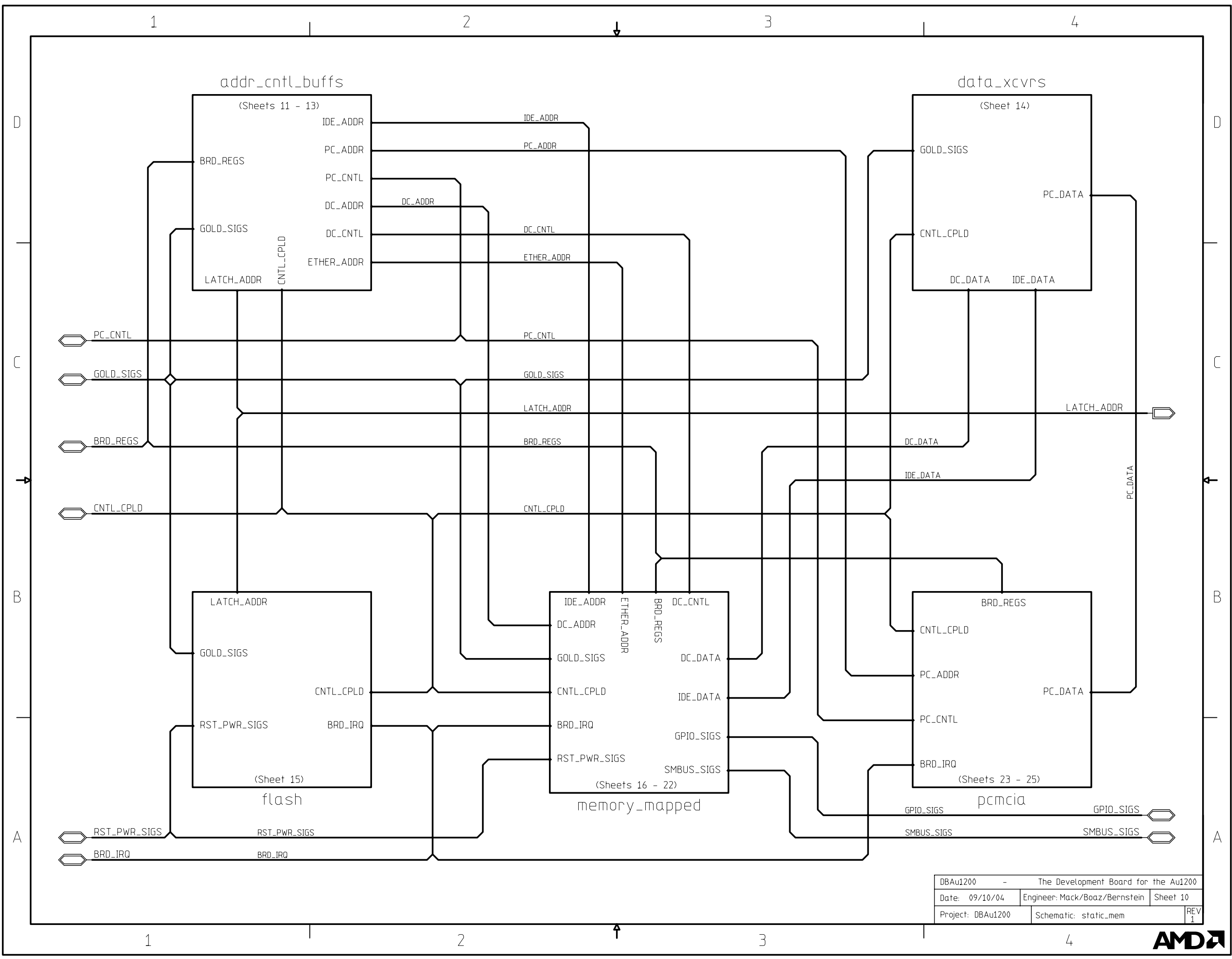
FB5_MC7

FB5_MC11

FB5_MC12

FB5_MC13

FB5_MC14



DBAu1200 - The Development Board for the Au1200			
Date: 09/10/04	Engineer: Mack/Boaz/Bernstein	Sheet 10	
Project: DBAu1200	Schematic: static_mem	REV	1



1

2

3

4

D

D

C

C

B

B

A

A

CNTL_CPLD

GOLD_SIGS

BRD_REGS

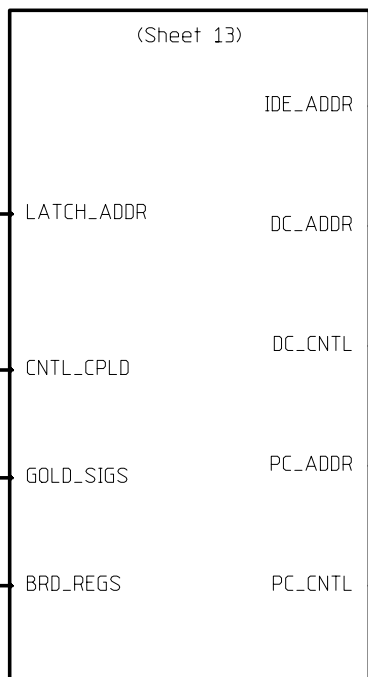
addr_latches

(Sheet 12)



static_addr_cntl

(Sheet 13)



ETHER_ADDR

LATCH_ADDR

IDE_ADDR

DC_ADDR

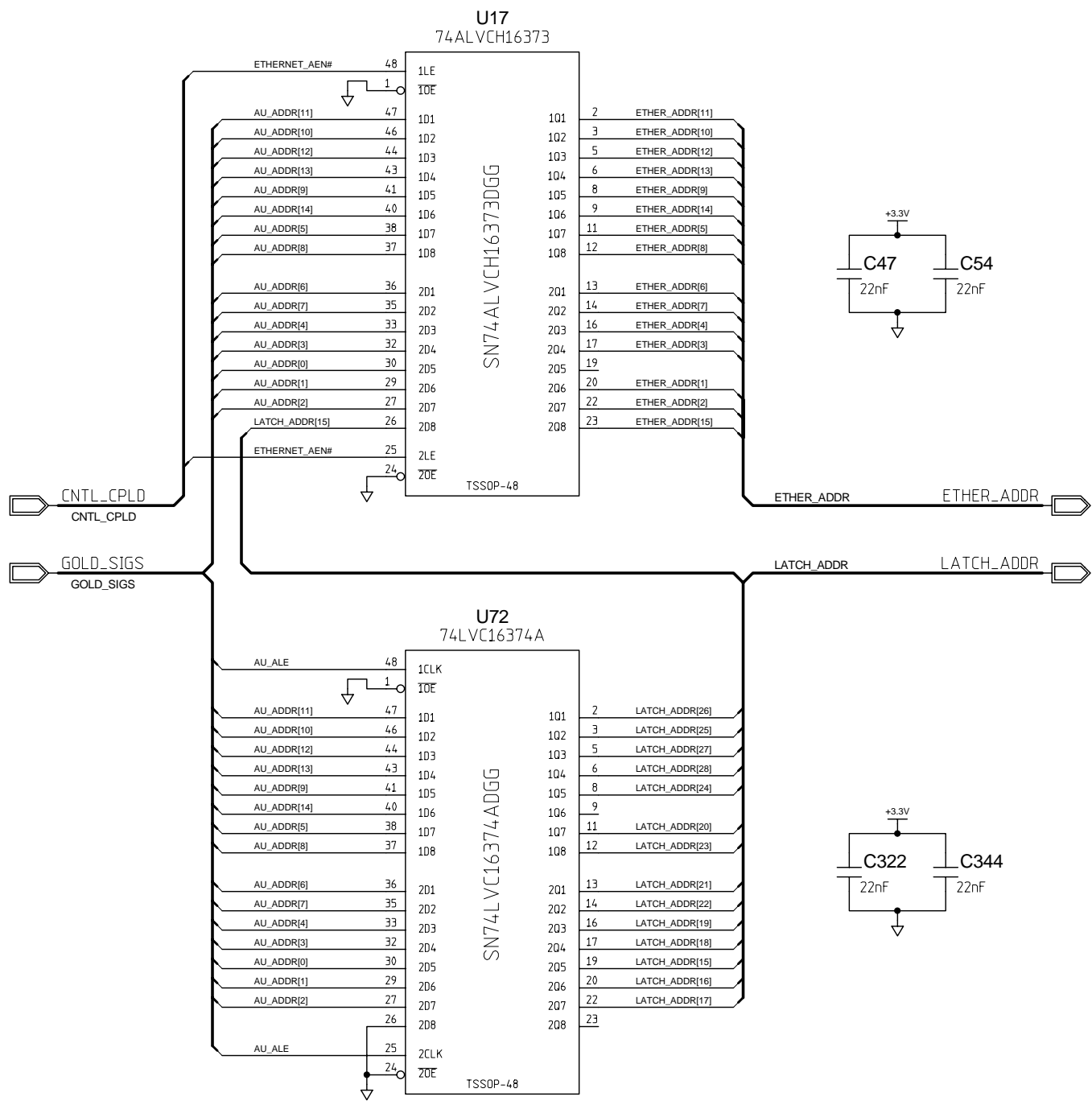
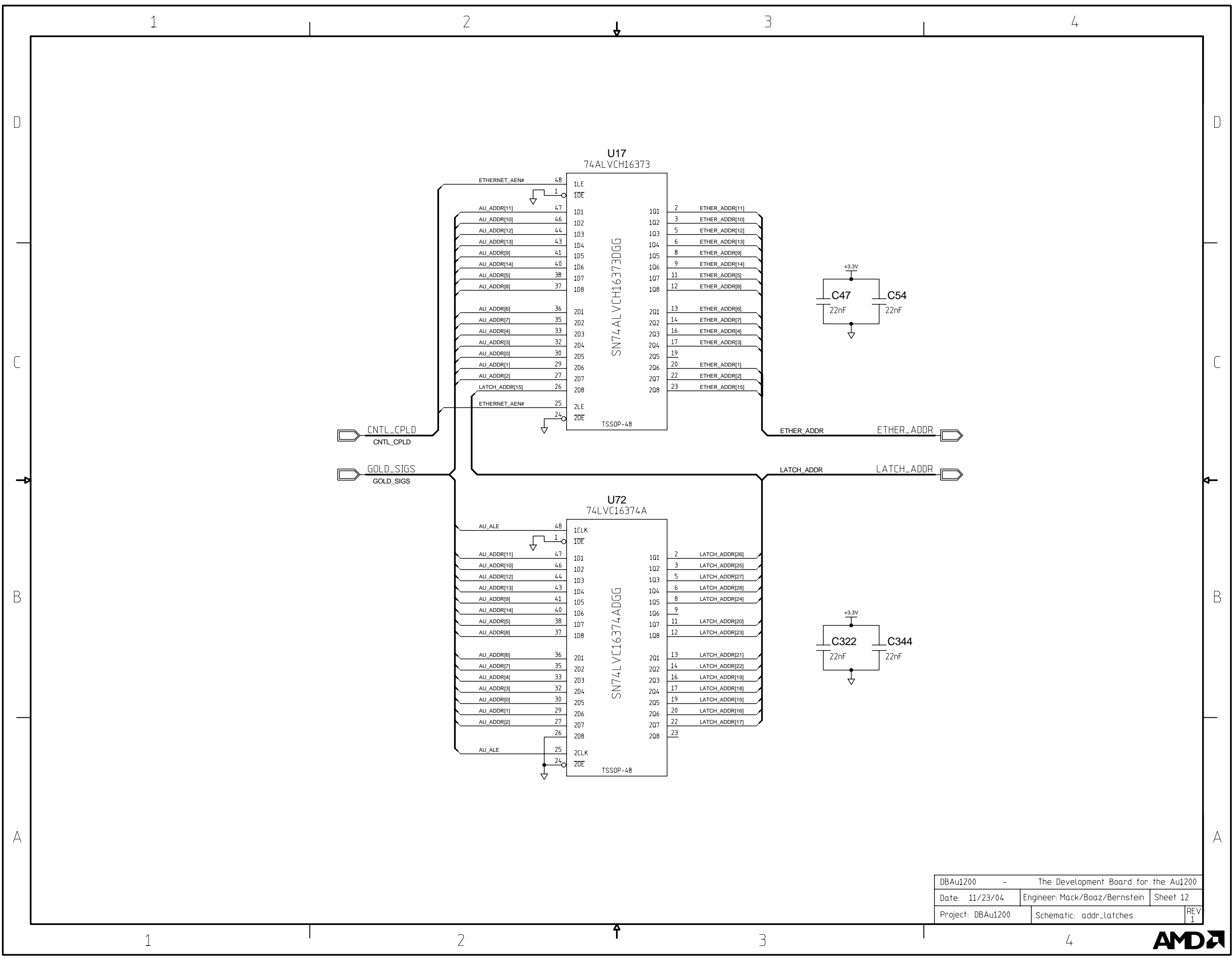
DC_CNTL

PC_ADDR

PC_CNTL

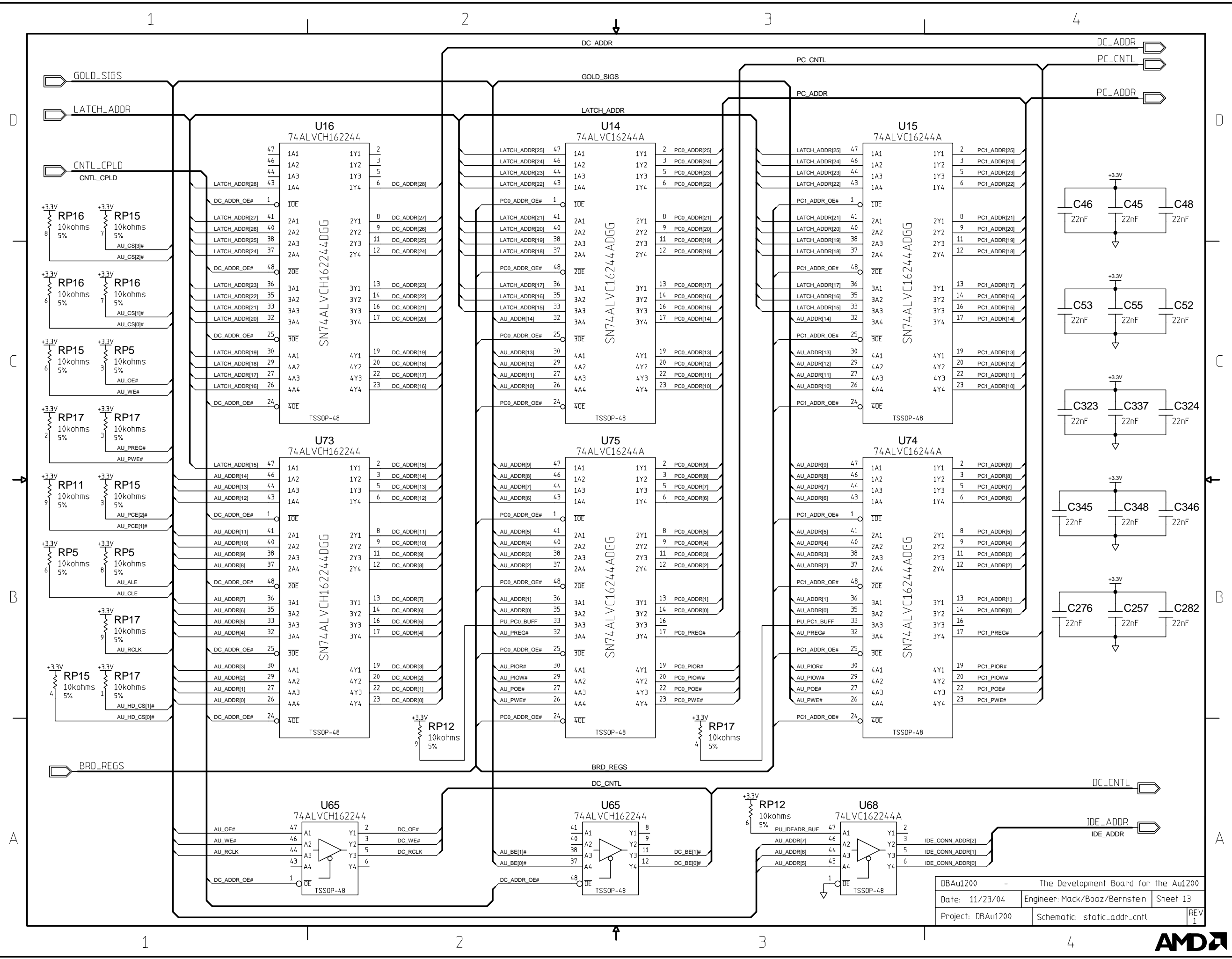
DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: addr_cntl_buffs
	Sheet 11
	REV 1





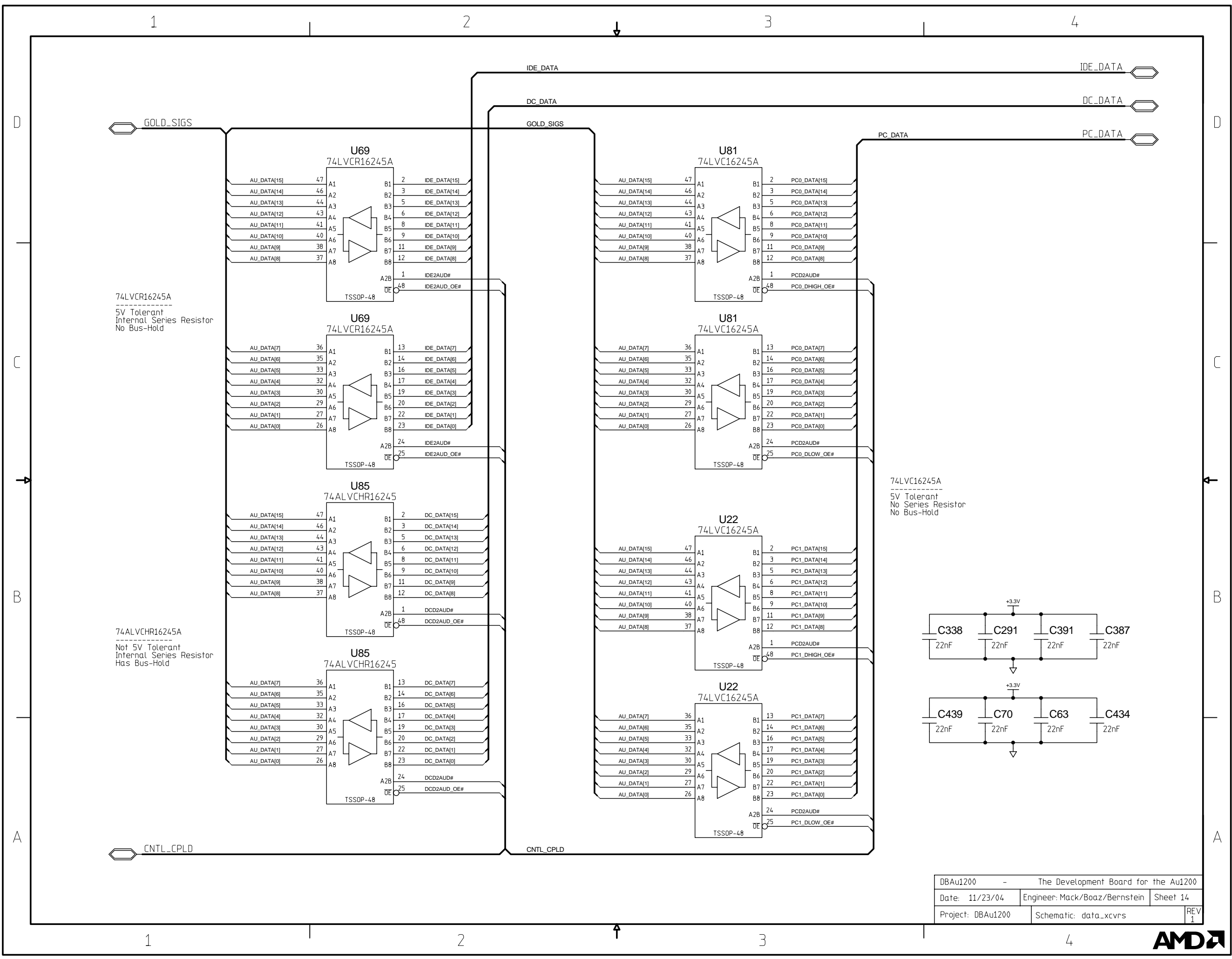
DBAu1200 - The Development Board for the Au1200			
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 12	
Project: DBAu1200	Schematic: addr_latches	REV	1

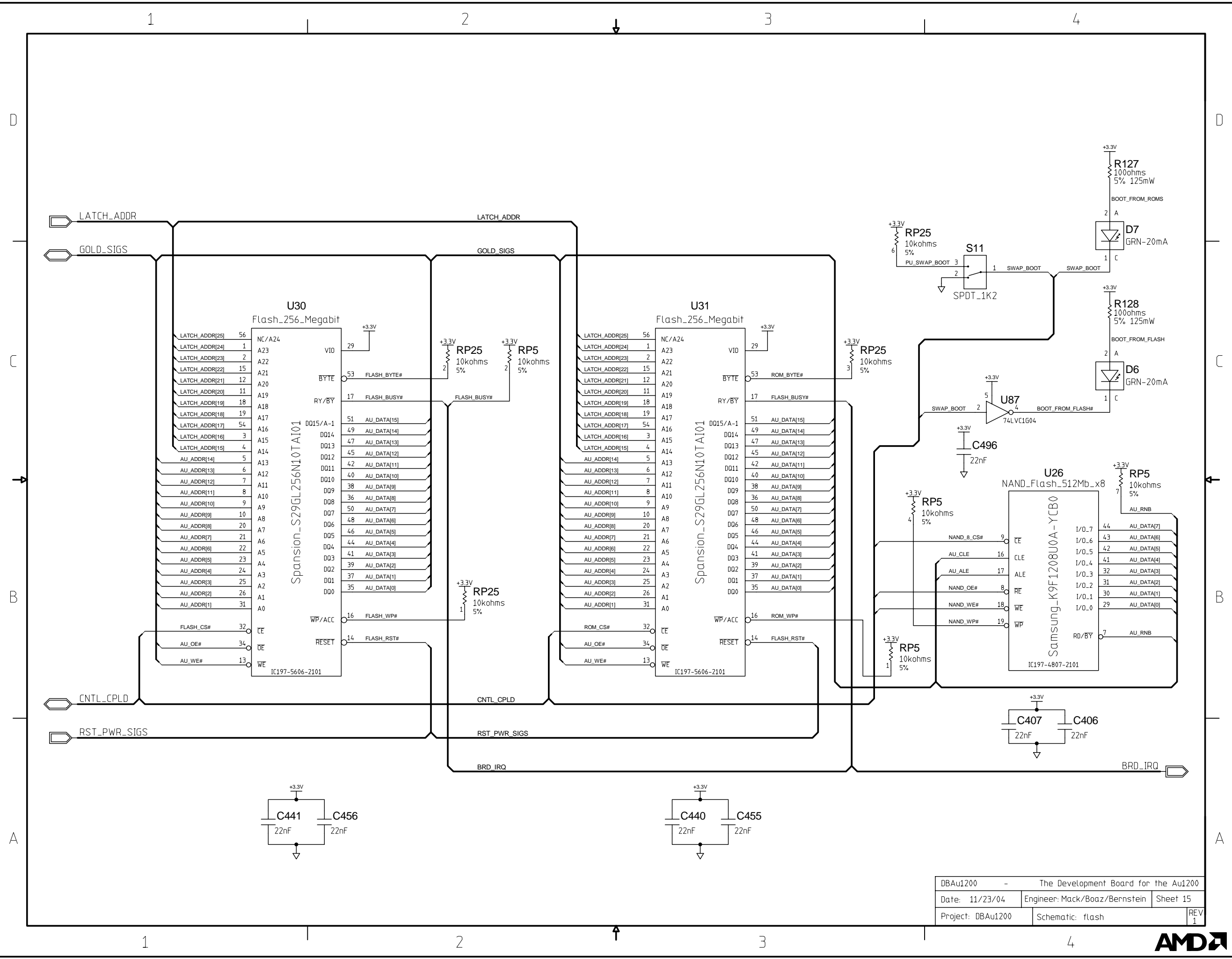




DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 13
Project: DBAu1200	Schematic: static_addr_cntl	REV 1

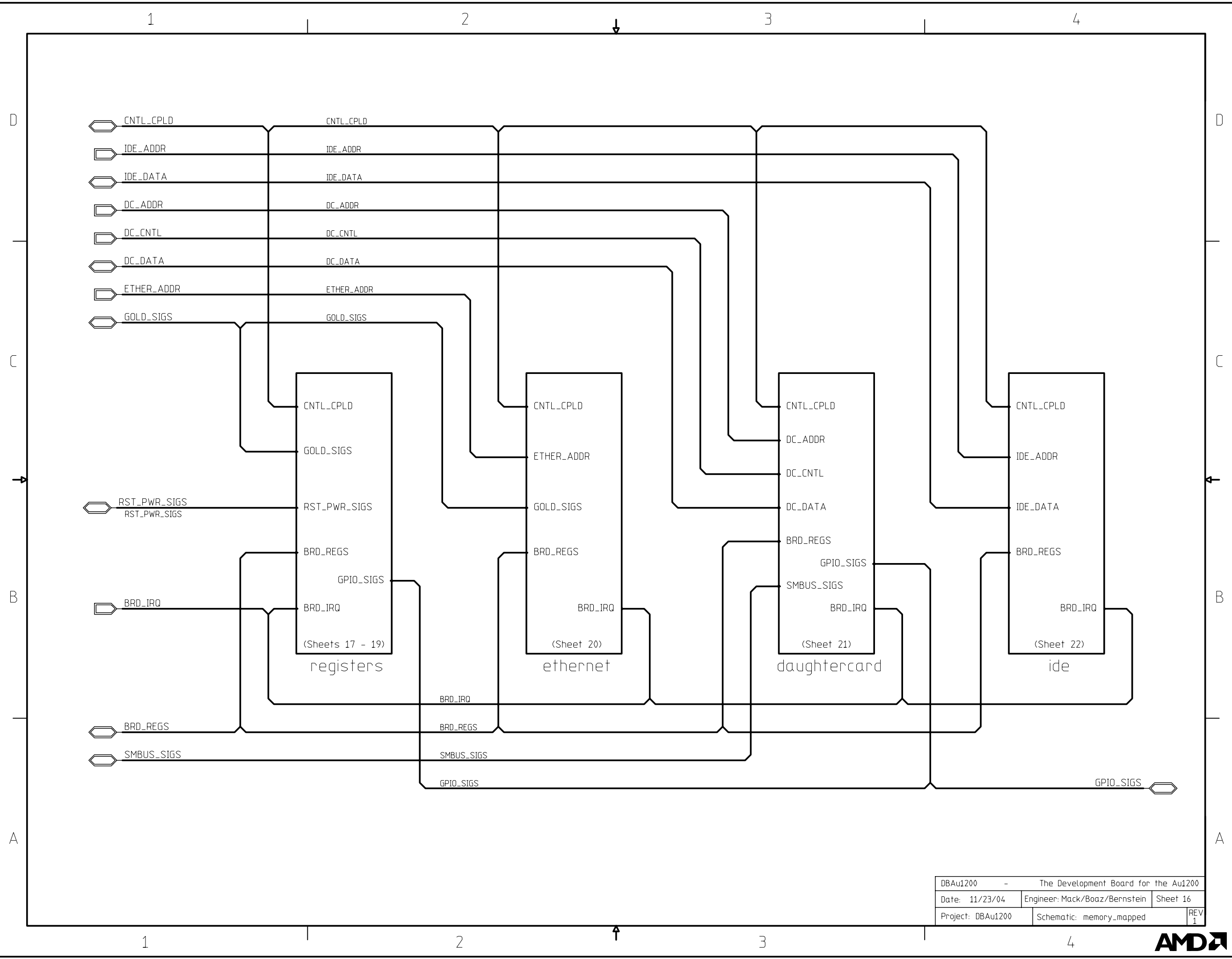






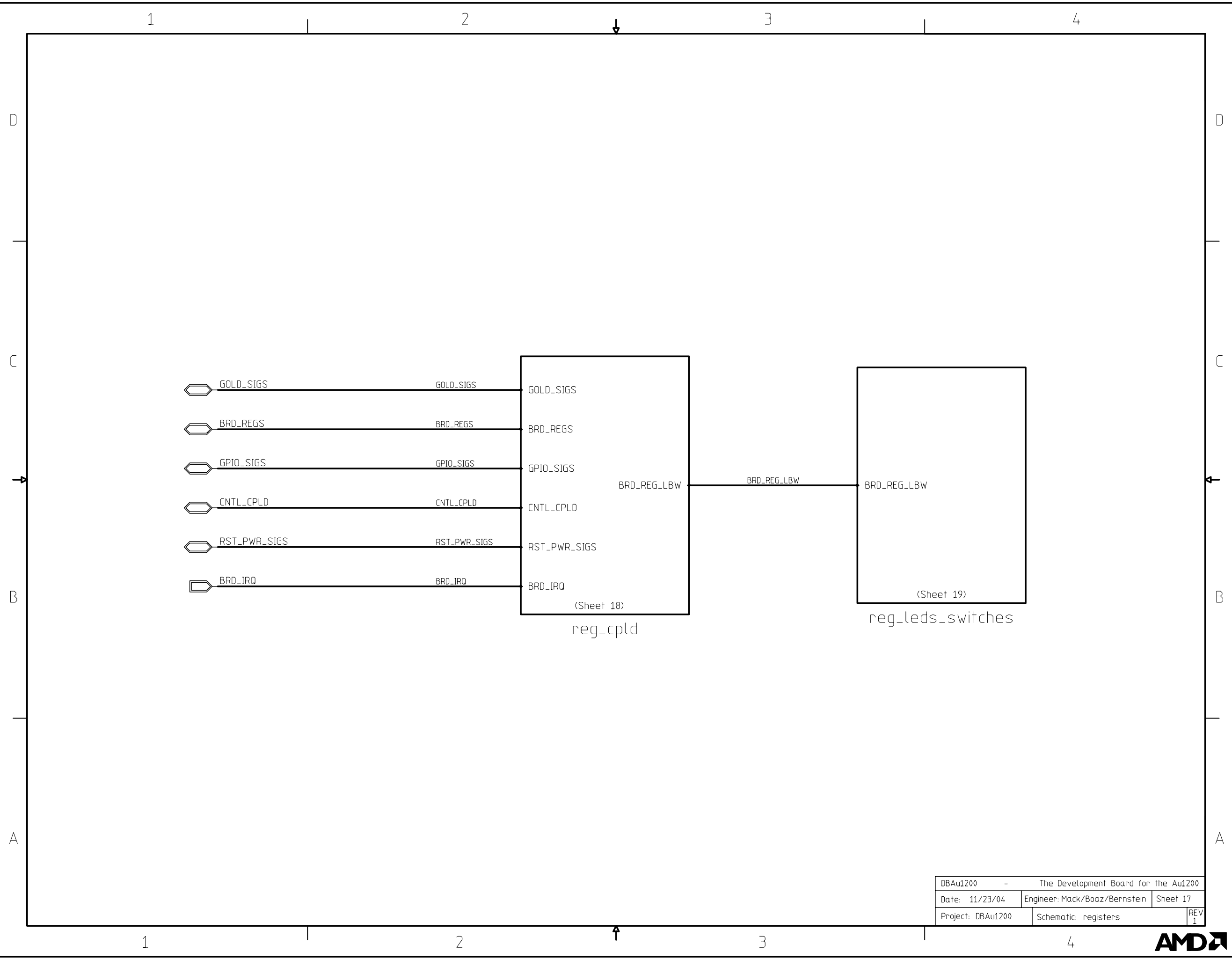
DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 15
Project: DBAu1200	Schematic: flash	REV 1





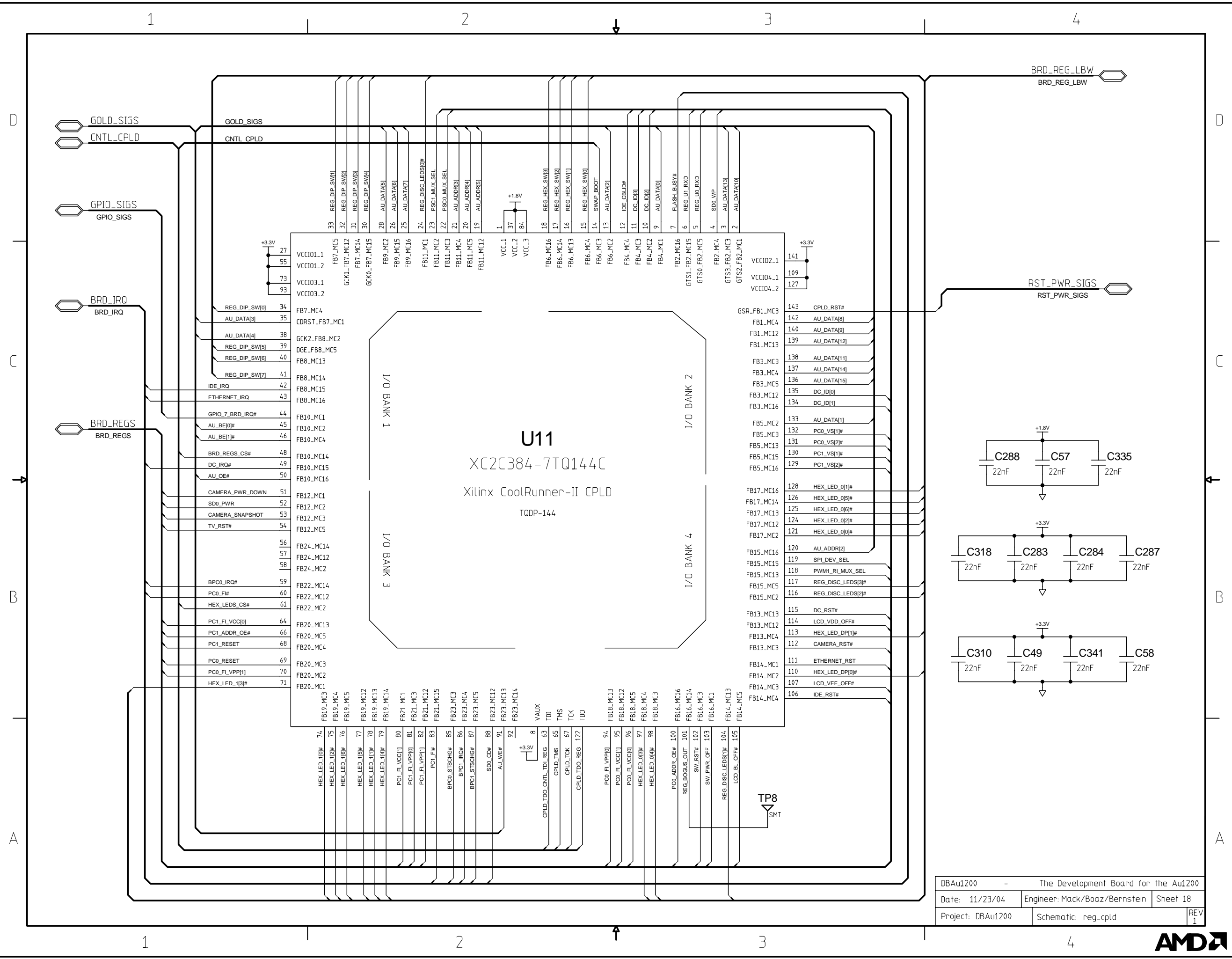
DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 16
Project: DBAu1200	Schematic: memory_mapped	REV 1





DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: registers
	REV 1





DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: reg_cpld
Sheet 18	
REV 1	



1

2

3

4

D

D

C

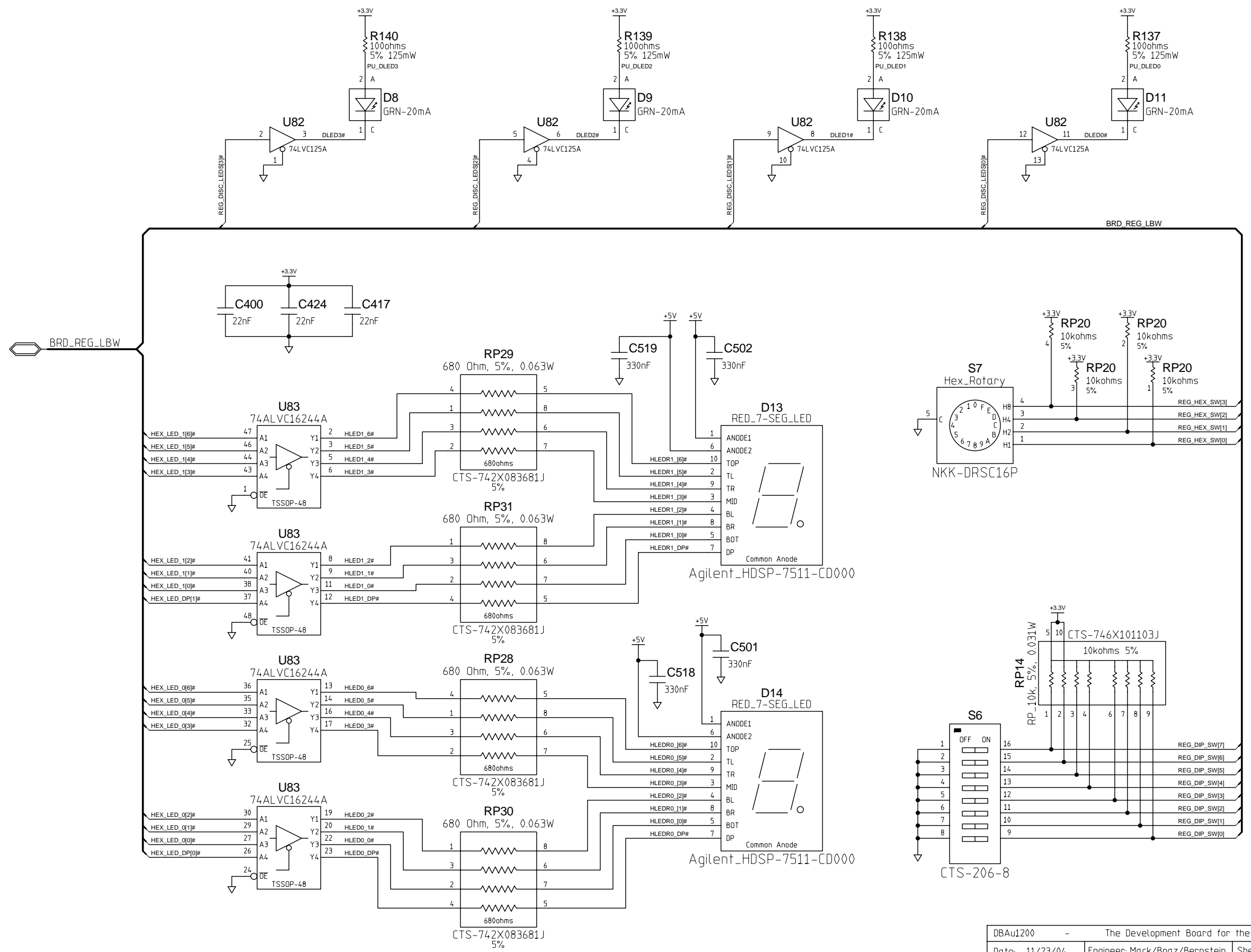
C

B

B

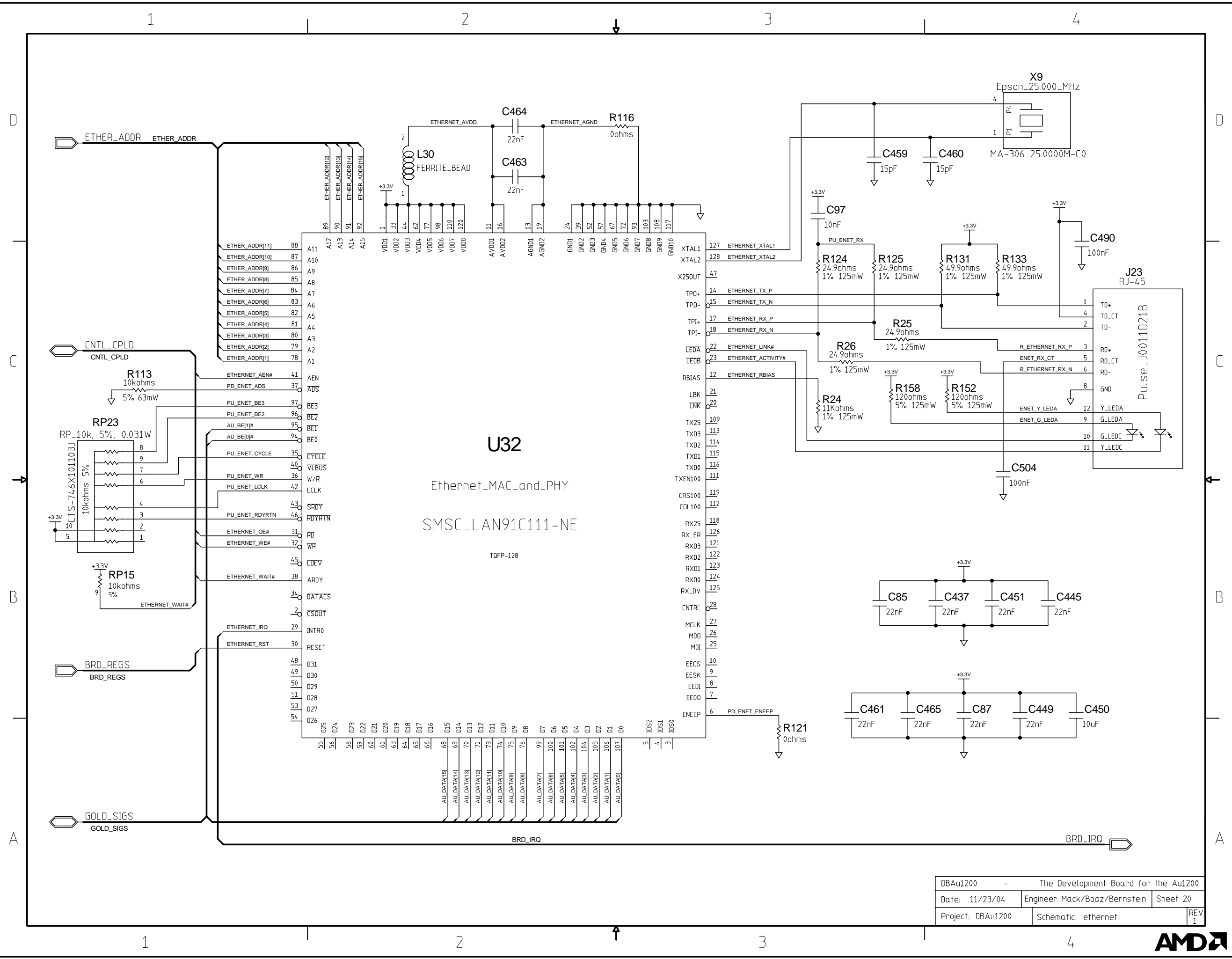
A

A



DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: reg_leds_switches
Sheet 19	REV 1

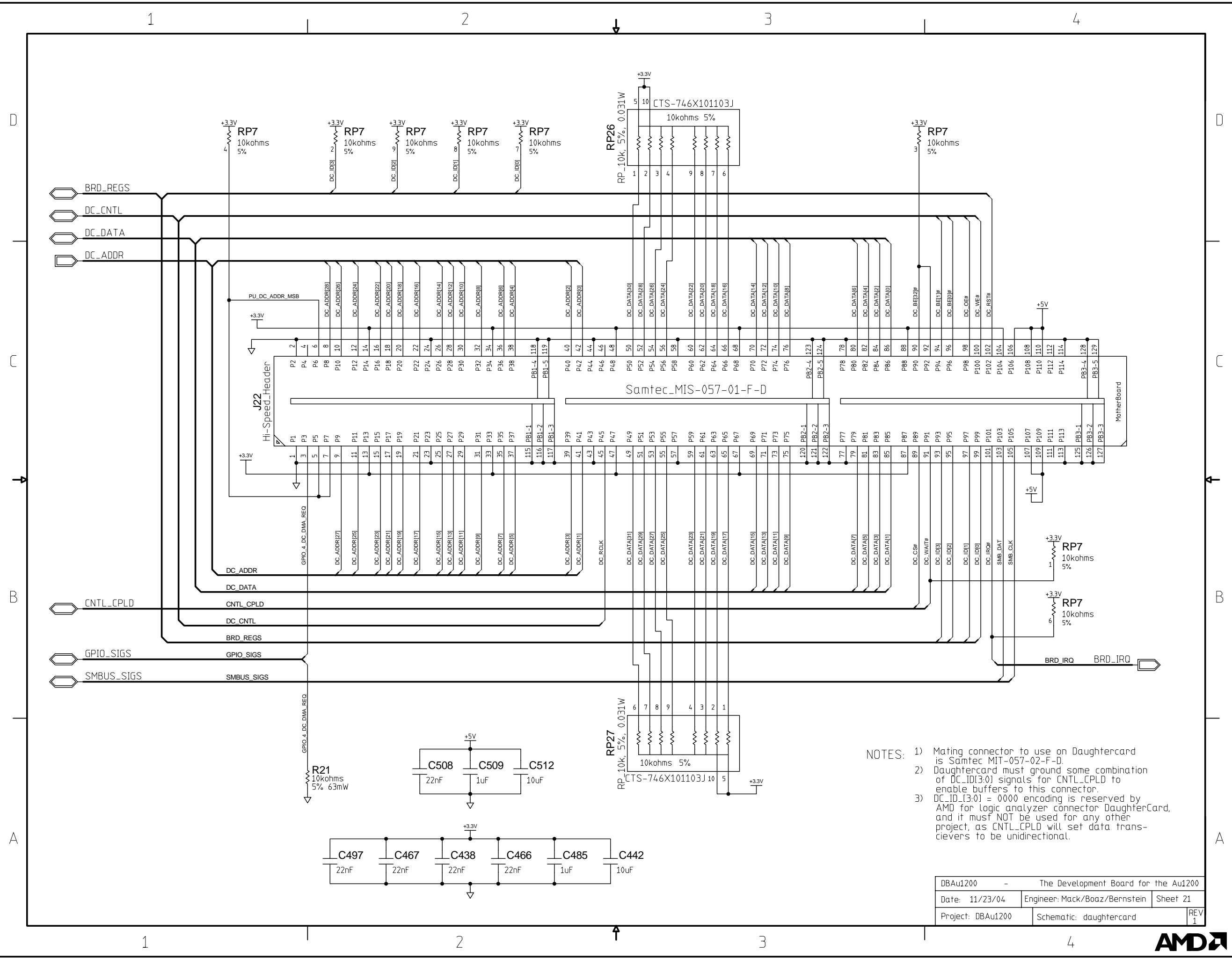




U32
Ethernet_MAC_and_PHY
SMSC_LAN91C111-NE
TQFP-128

DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: ethernet
Sheet 20	
REV 1	

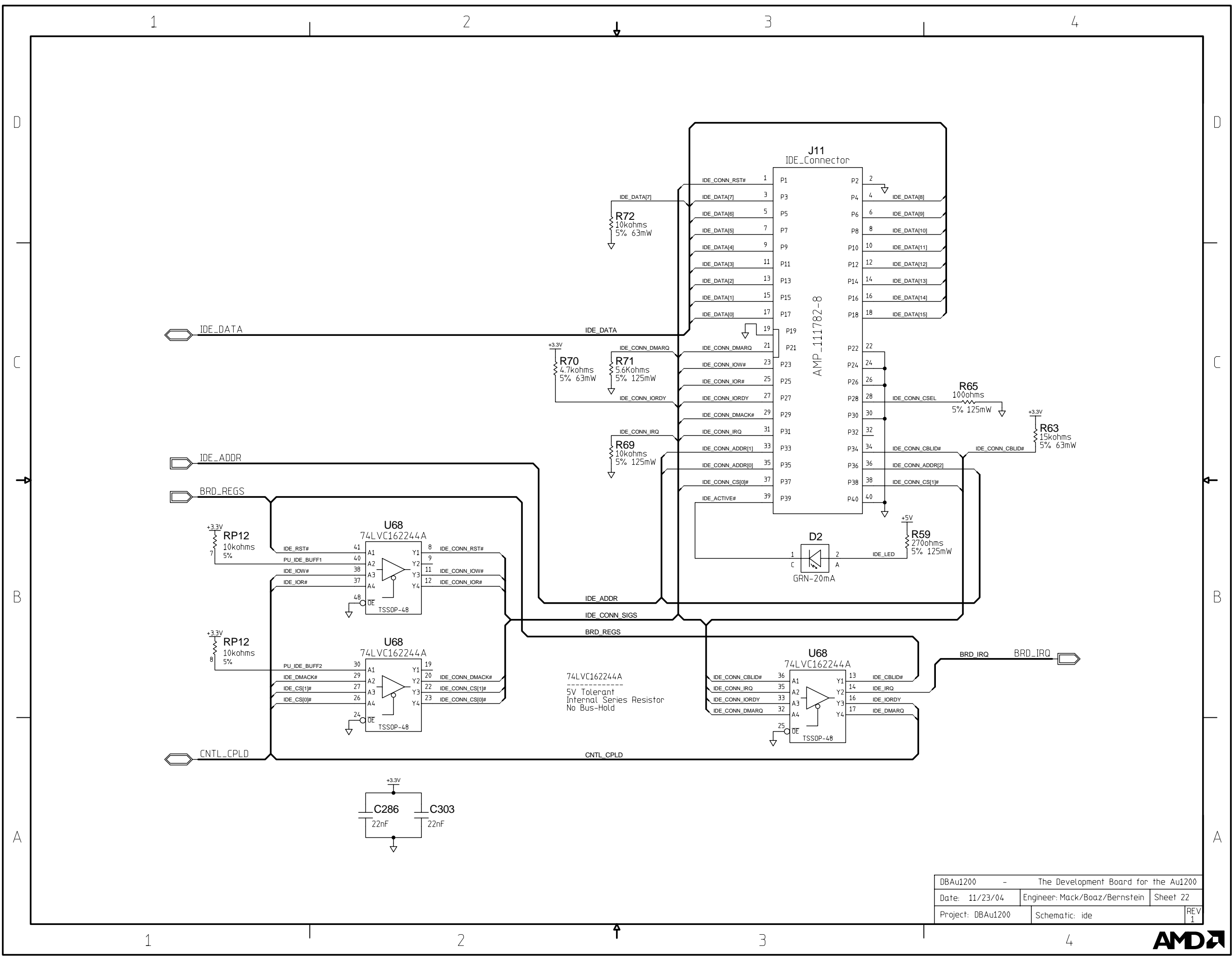




- NOTES:
- 1) Mating connector to use on Daughtercard is Samtec MIT-057-02-F-D.
 - 2) Daughtercard must ground some combination of DC_ID[3:0] signals for CNTL_CPLD to enable buffers to this connector.
 - 3) DC_ID[3:0] = 0000 encoding is reserved by AMD for logic analyzer connector DaughterCard, and it must NOT be used for any other project, as CNTL_CPLD will set data transceivers to be unidirectional.

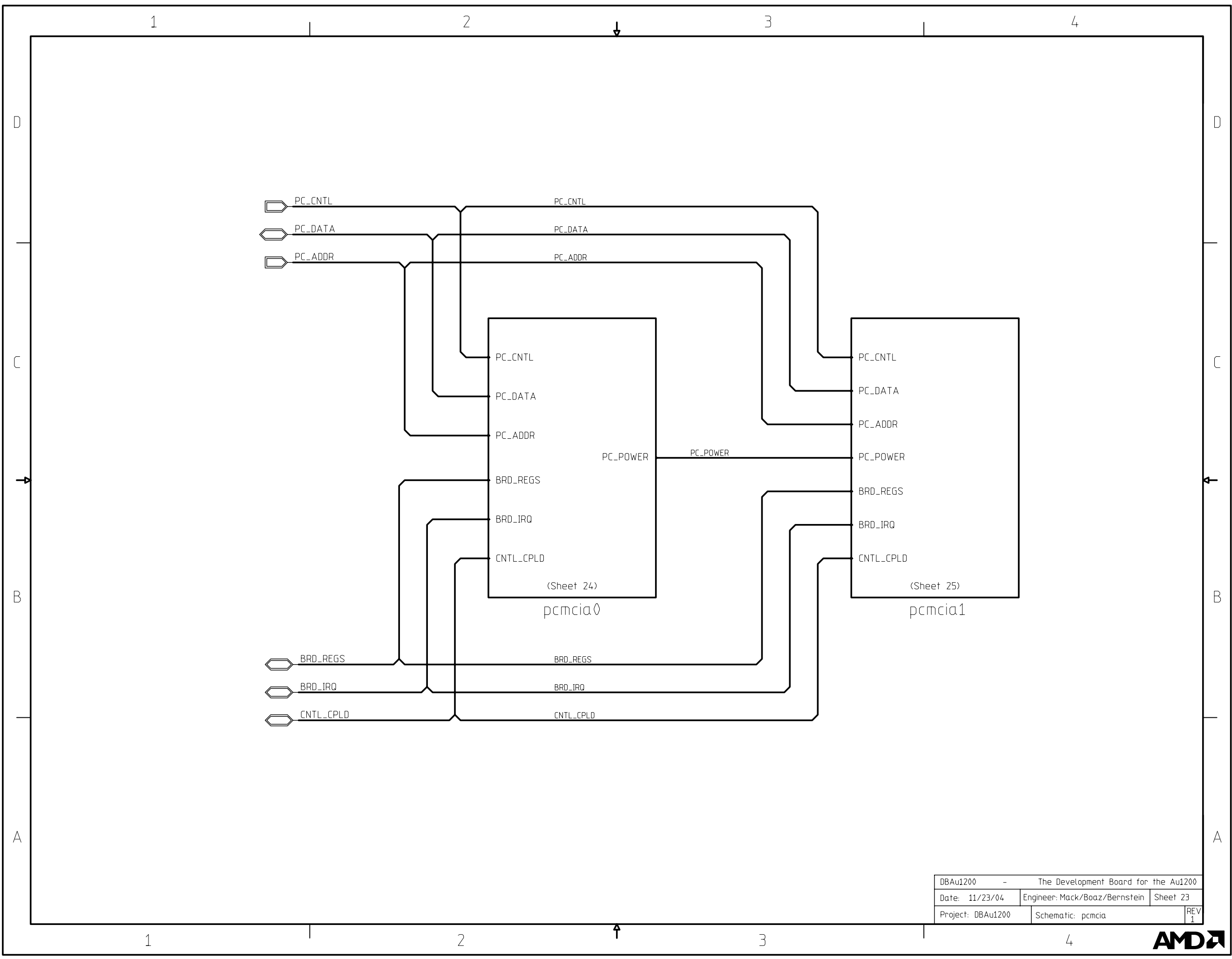
DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: daughtercard
Sheet 21	REV 1





DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: ide
Sheet 22	REV 1





DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: pcmcia
	Sheet 23
	REV 1



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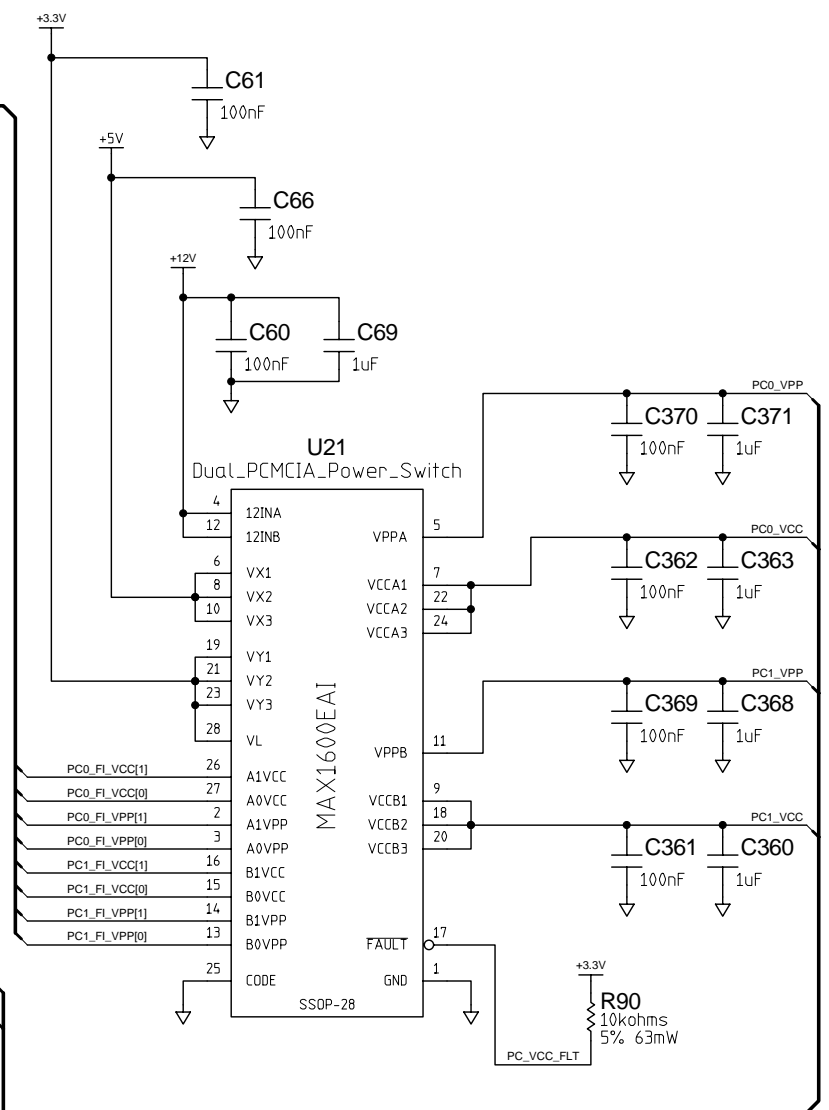
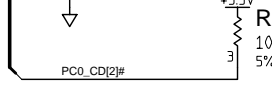
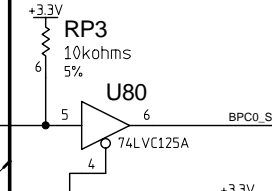
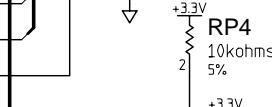
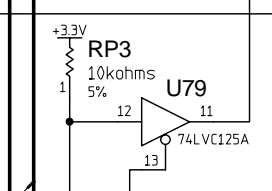
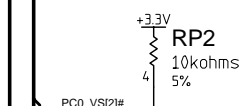
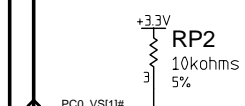
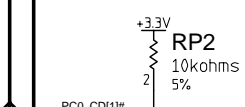
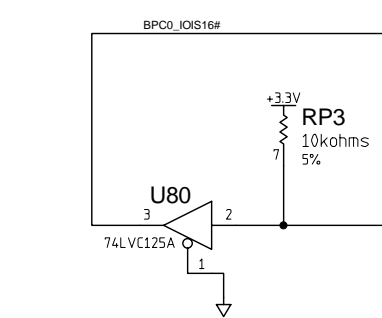
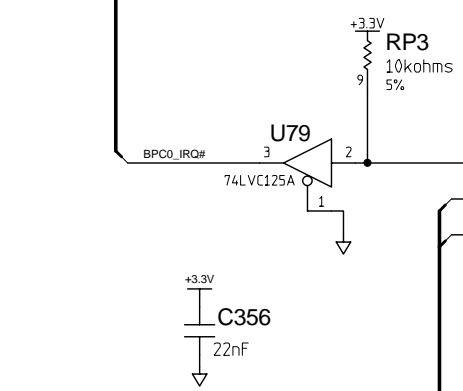
BRD_REGS
 CNTL_CPLD
 PC_ADDR
 PC_DATA
 PC_CNTL
 BRD_IRQ

BRD_REGS
 CNTL_CPLD
 PC_ADDR
 PC_DATA
 PC_CNTL
 BRD_IRQ

J16
 PCMCIA_SMT_Receptacle

1	P1-GND1	P35-GND3	51	PC0_CD[1]#
2	P2-D3	P36-C01#	52	PC0_DATA[11]
3	P3-D4	P37-D11	53	PC0_DATA[12]
4	P4-D5	P38-D12	54	PC0_DATA[13]
5	P5-D6	P39-D13	55	PC0_DATA[14]
6	P6-D7	P40-D14	56	PC0_DATA[15]
7	P7-CE1#	P41-D15	57	PC0_PCE[2]#
8	P8-A10	P42-CE2#	58	PC0_VS[1]#
9	P9-OE#	P43-VS1#	59	PC0_PIOR#
10	P10-A11	P44-IORD#	60	PC0_PIOW#
11	P11-A9	P45-IOWR#	61	PC0_ADDR[17]
12	P12-A8	P46-A17	62	PC0_ADDR[18]
13	P13-A13	P47-A18	63	PC0_ADDR[19]
14	P14-A14	P48-A19	64	PC0_ADDR[20]
15	P15-A9	P49-A20	65	PC0_ADDR[21]
16	P16-RDY/IRE0#	P50-A21	66	PC0_VCC
17	P17-VCC1	P51-VCC2	67	PC0_VPP
18	P18-VPP1	P52-VPP2	68	PC0_ADDR[22]
19	P19-A16	P53-A22	69	PC0_ADDR[23]
20	P20-A15	P54-A23	70	PC0_ADDR[24]
21	P21-A12	P55-A24	71	PC0_ADDR[25]
22	P22-A7	P56-A25	72	PC0_VS[2]#
23	P23-A6	P57-VS2#	73	PC0_RESET
24	P24-A5	P58-RESET	74	PC0_WAIT#
25	P25-A4	P59-WAIT#	75	PC0_INPACK#
26	P26-A3	P60-INPACK#	76	PC0_PREG#
27	P27-A2	P61-REG#	77	PC0_SPKR
28	P28-A1	P62-BVD2/SPKR#	78	PC0_STSCHG#
29	P29-A0	P63-BVD1/STSCHG#	79	PC0_DATA[8]
30	P30-D0	P64-D8	80	PC0_DATA[9]
31	P31-D1	P65-D9	81	PC0_DATA[10]
32	P32-D2	P66-D10	82	PC0_CD[2]#
33	P33-WP/IOIS16#	P67-CD2#	83	
34	P34-GND2	P68-GND4	84	
35			85	
36			86	
37			87	
38			88	
39			89	
40			90	
41			91	
42			92	
43			93	
44			94	
45			95	
46			96	
47			97	
48			98	
49			99	
50			100	

FCL-73277-10100



NOTE: PC0 is the bottom slot.

DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: pcmcia0
Sheet 24	REV 1



BRD_REGS
 CNTL_CPLD
 PC_ADDR
 PC_DATA
 PC_CNTL
 BRD_IRQ

BRD_REGS
 CNTL_CPLD
 PC_ADDR
 PC_DATA
 PC_CNTL
 BRD_IRQ

D

D

C

C

B

B

A

A

1

2

3

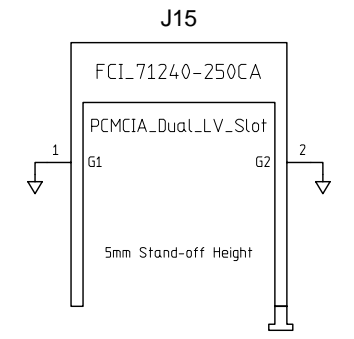
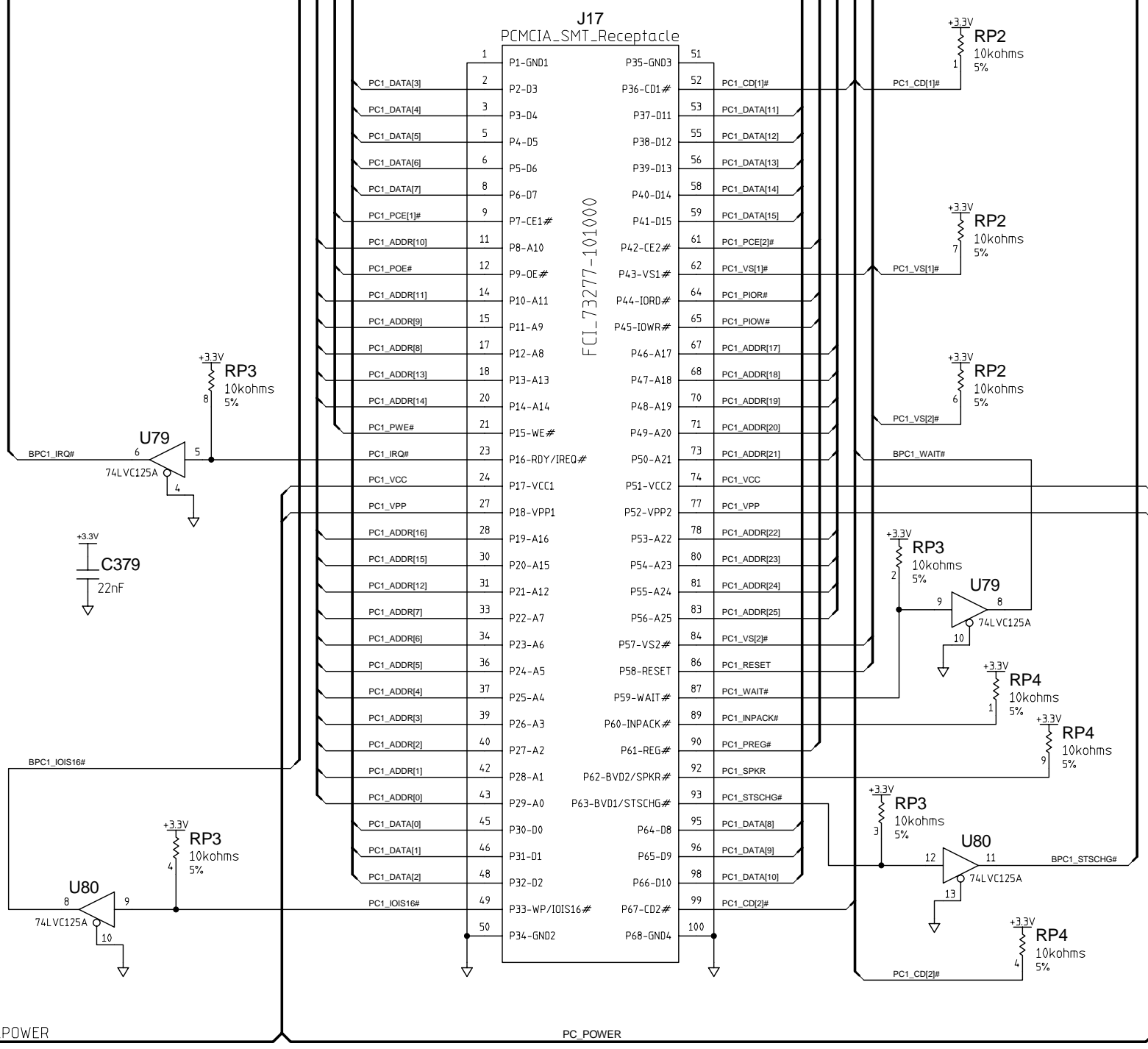
4

1

2

3

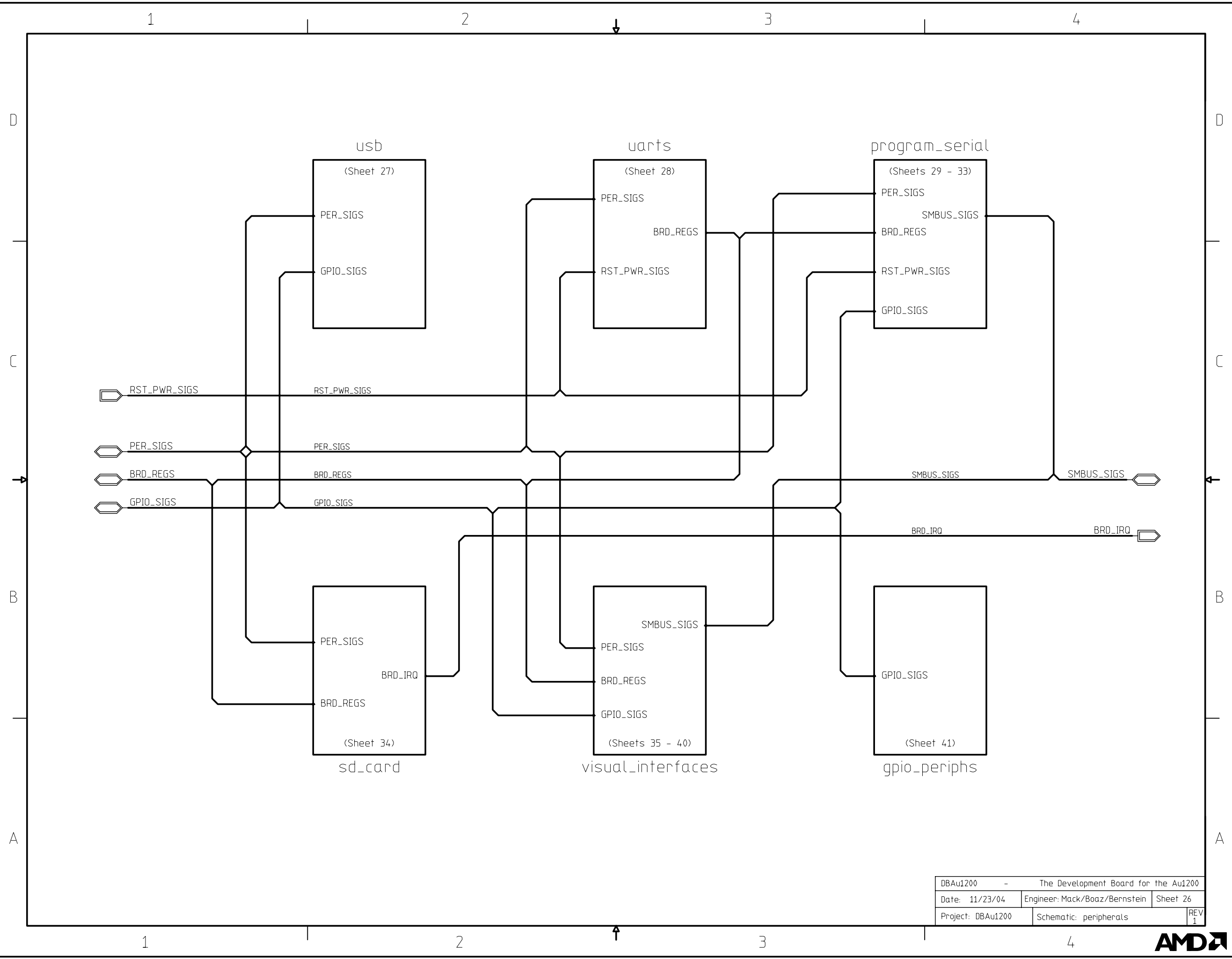
4



NOTE: PC1 is the top slot.

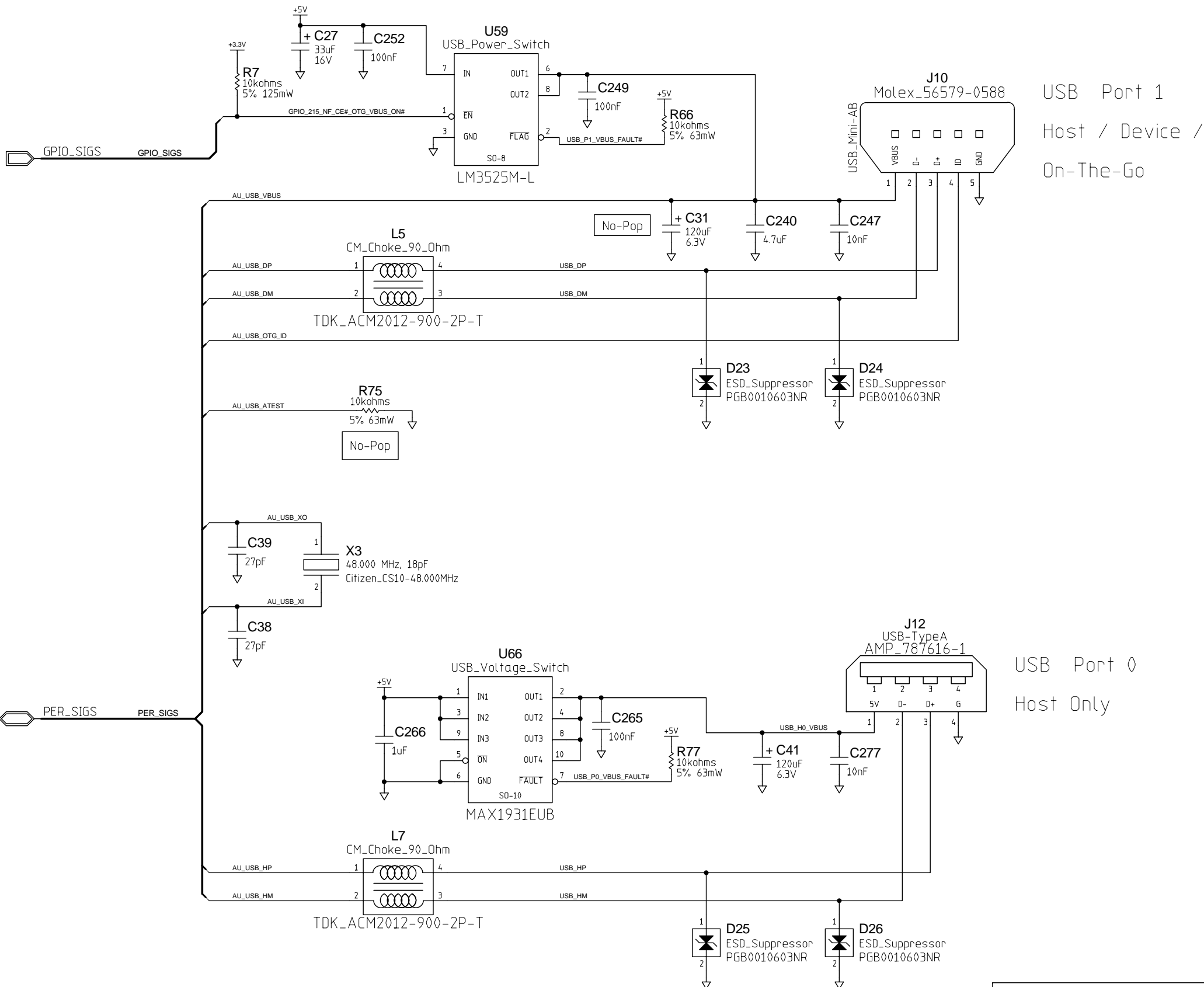
DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: pcmcia1
Sheet 25	REV 1





DBAu1200 - The Development Board for the Au1200			
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 26	
Project: DBAu1200	Schematic: peripherals	REV	1

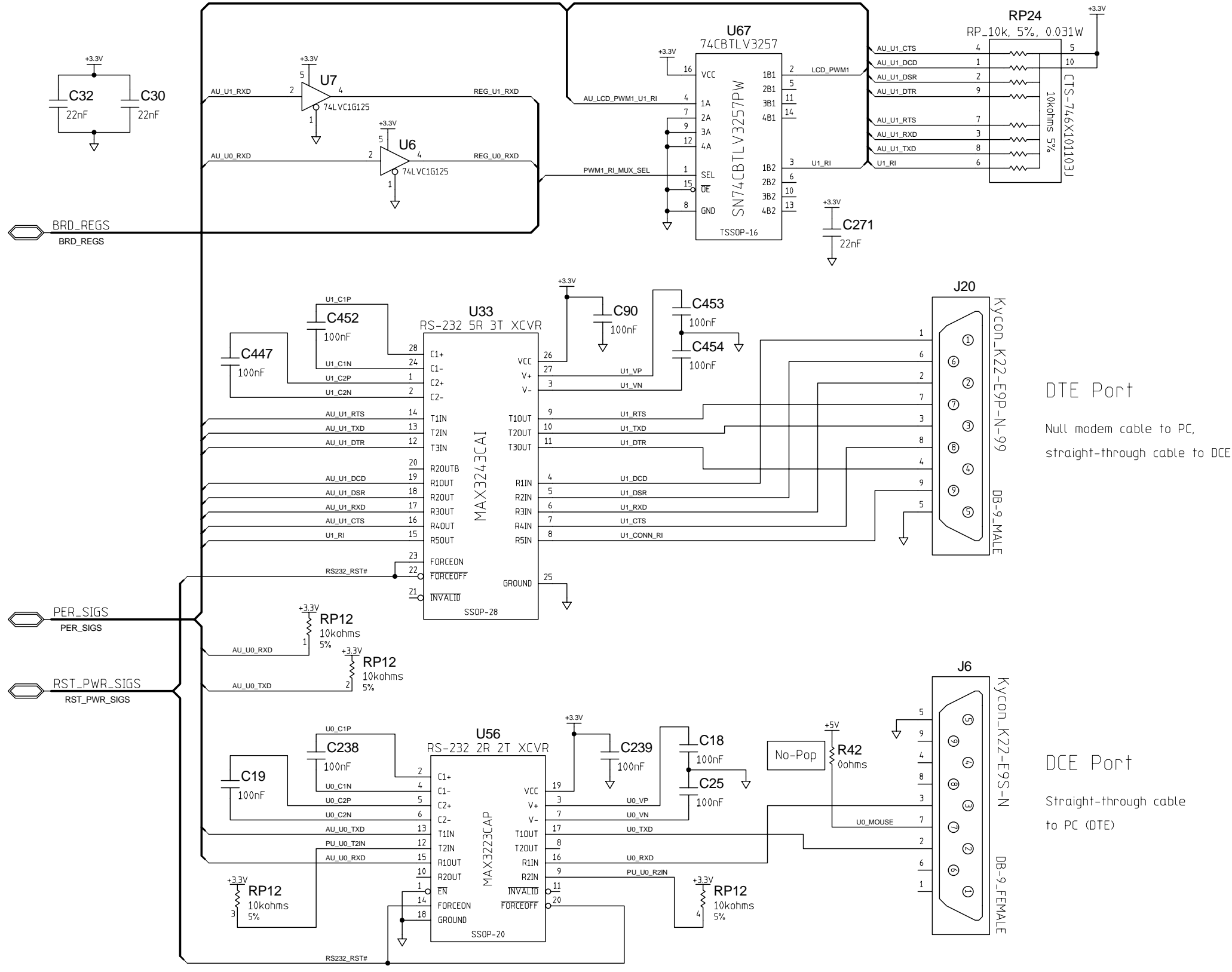




DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: usb
Sheet 27	REV 1



1 2 3 4



DTE Port
 Null modem cable to PC,
 straight-through cable to DCE

DCE Port
 Straight-through cable
 to PC (DTE)

DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: uarts
REV 1	



D
C
B
A

D
C
B
A

1 2 3 4

1

2

3

4

D

D

C

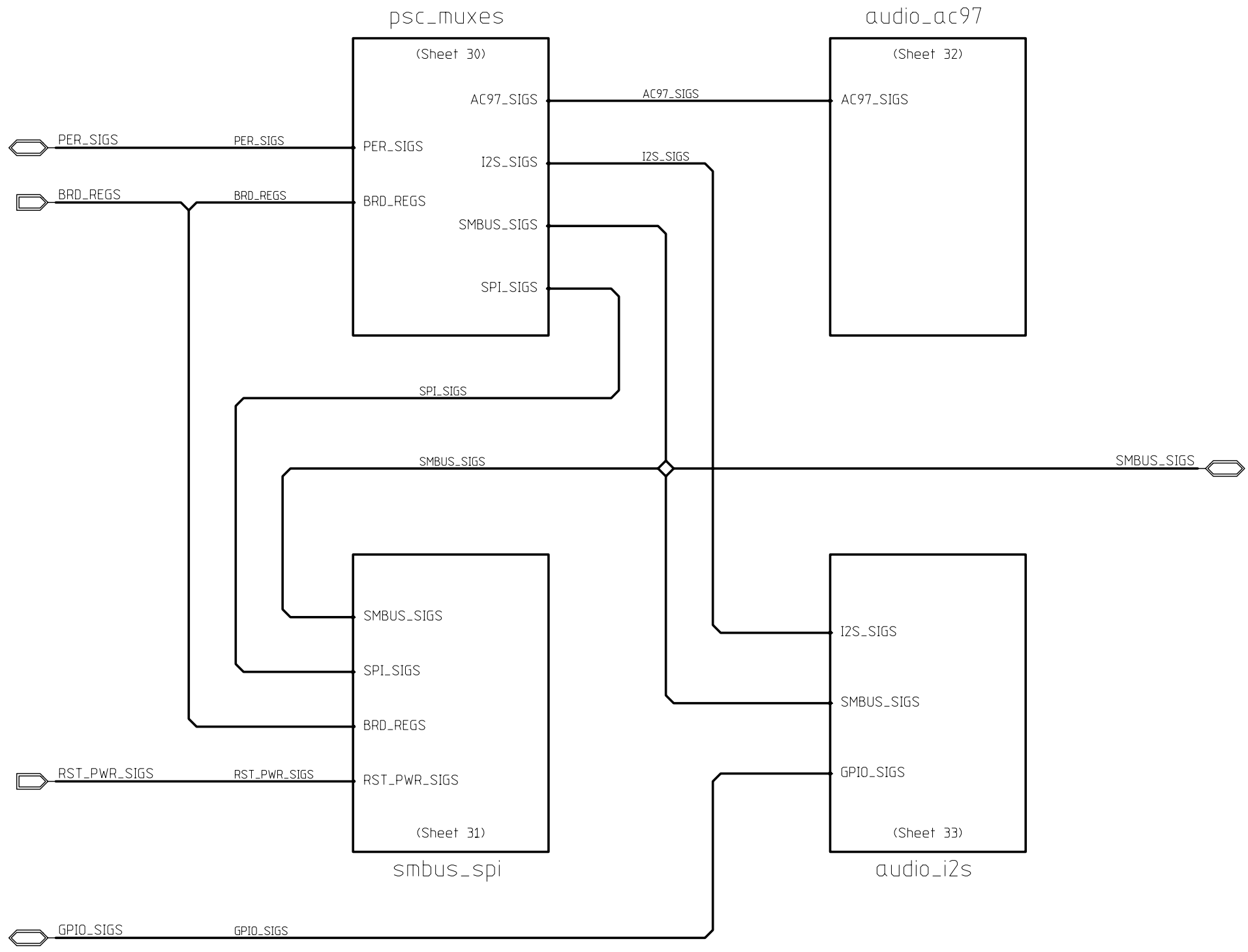
C

B

B

A

A



DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: program_serial
	Sheet 29
	REV 1



1

2

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D

D

C

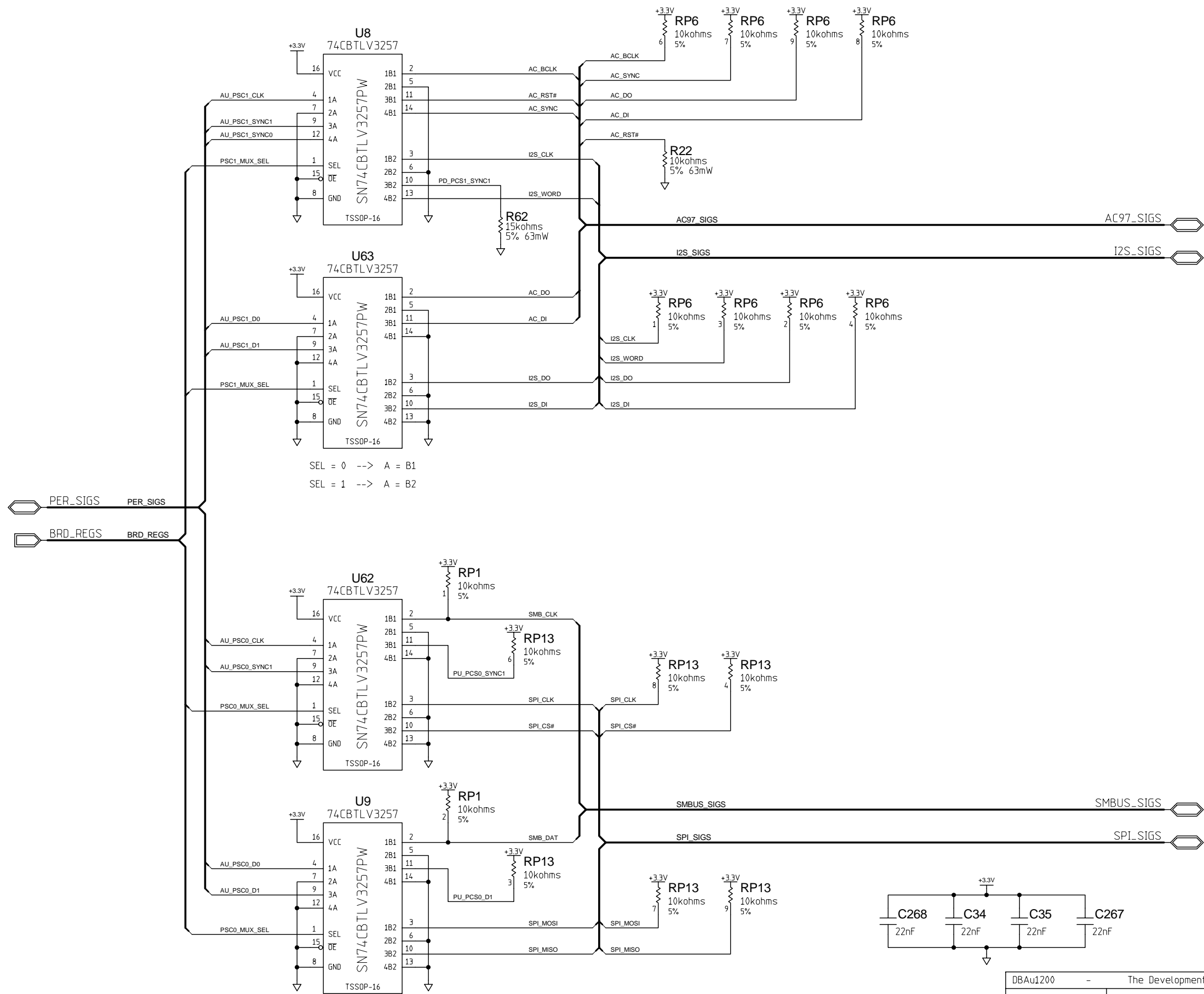
C

B

B

A

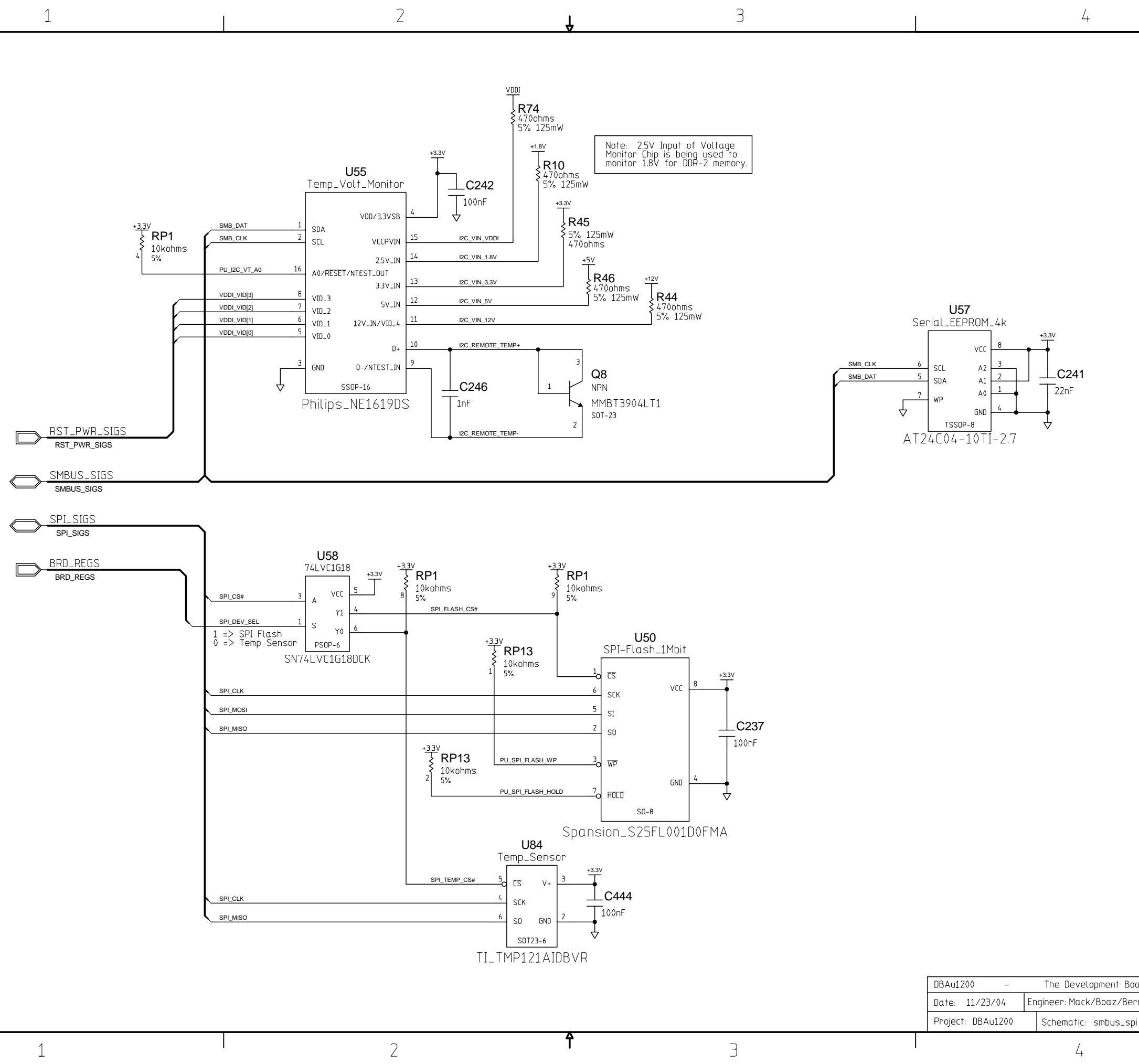
A



SEL = 0 --> A = B1
 SEL = 1 --> A = B2

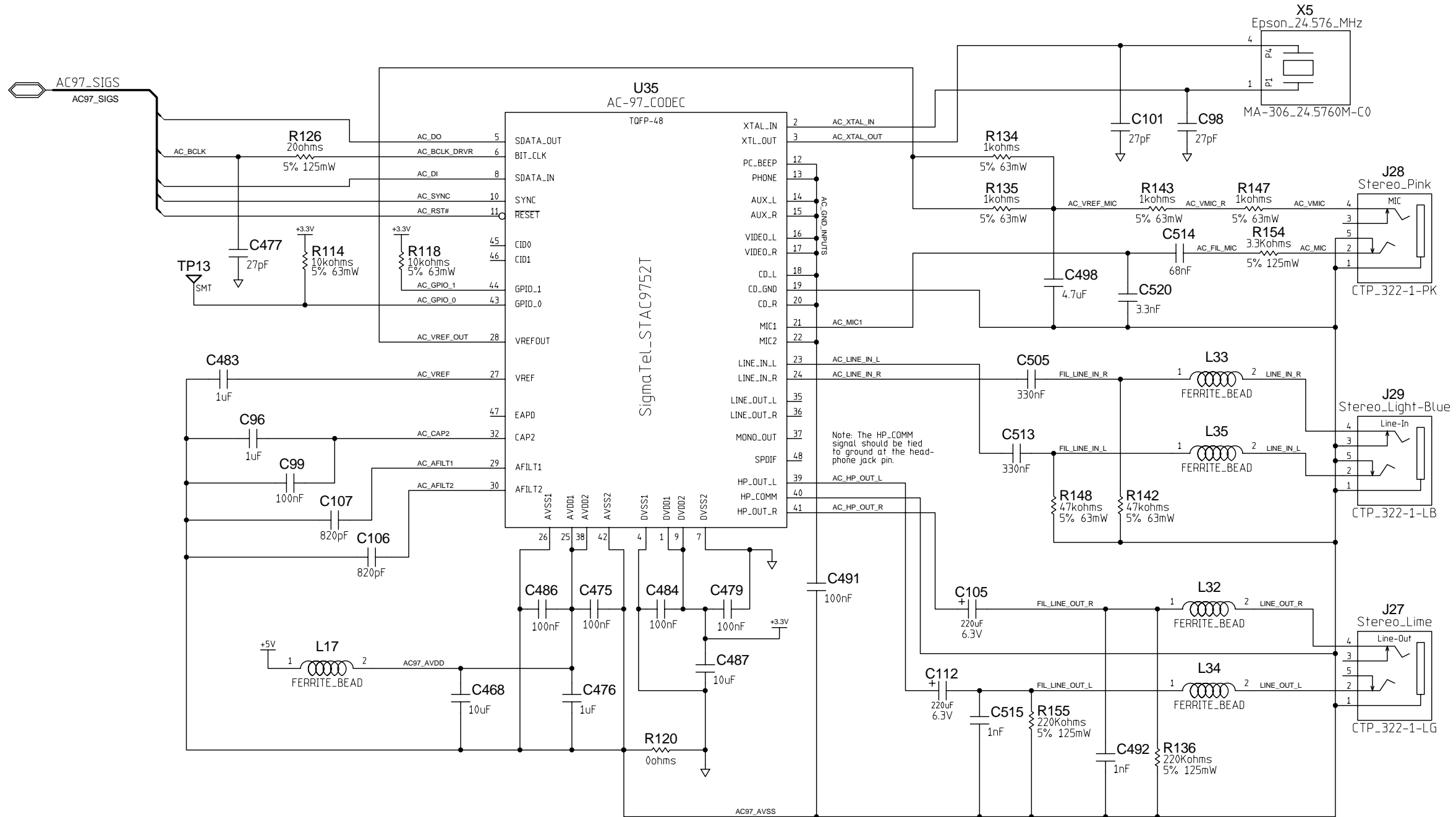
DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: psc-muxes
Sheet 30	REV 1





DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein Sheet 31
Project: DBAu1200	Schematic: smbus_spi
	REV 1





DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: audio_ac97
Sheet 32	REV 1

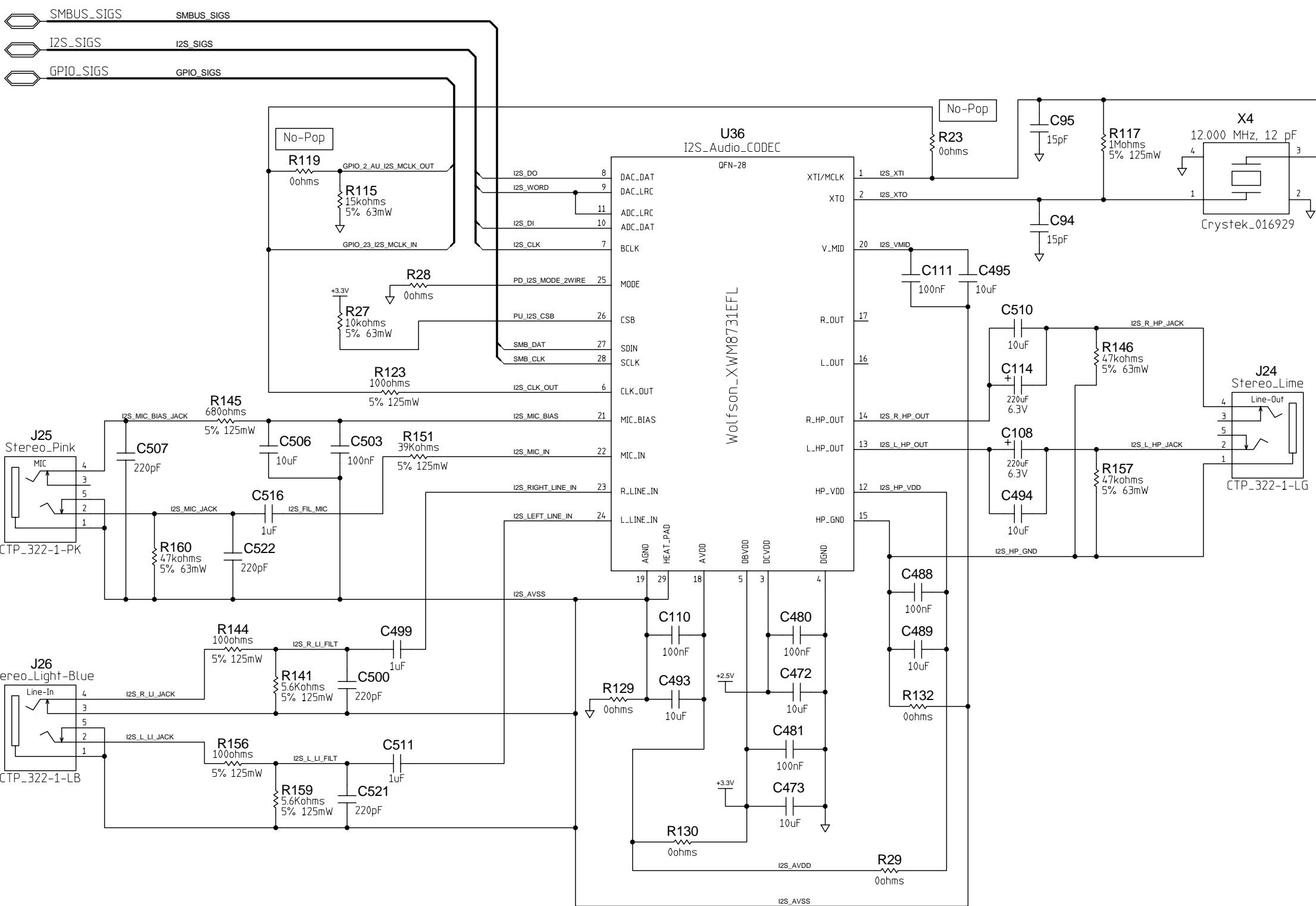


1

2

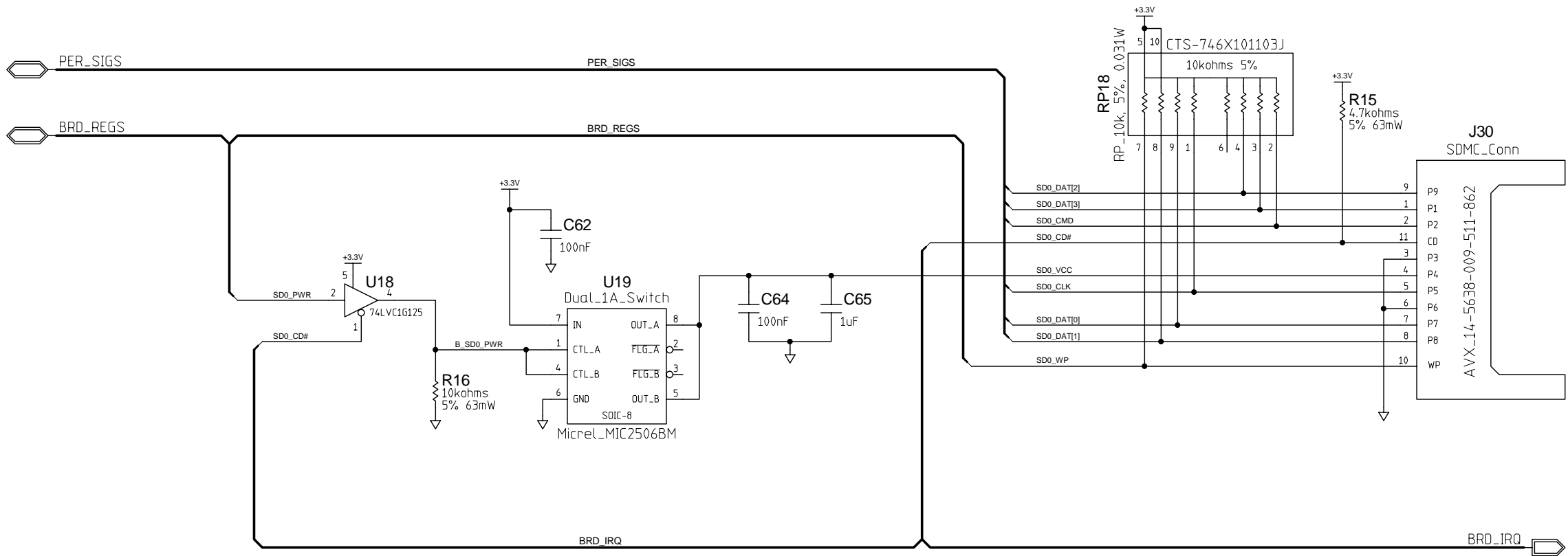
3

4



DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: audio_i2s
Sheet 33	
REV 1	



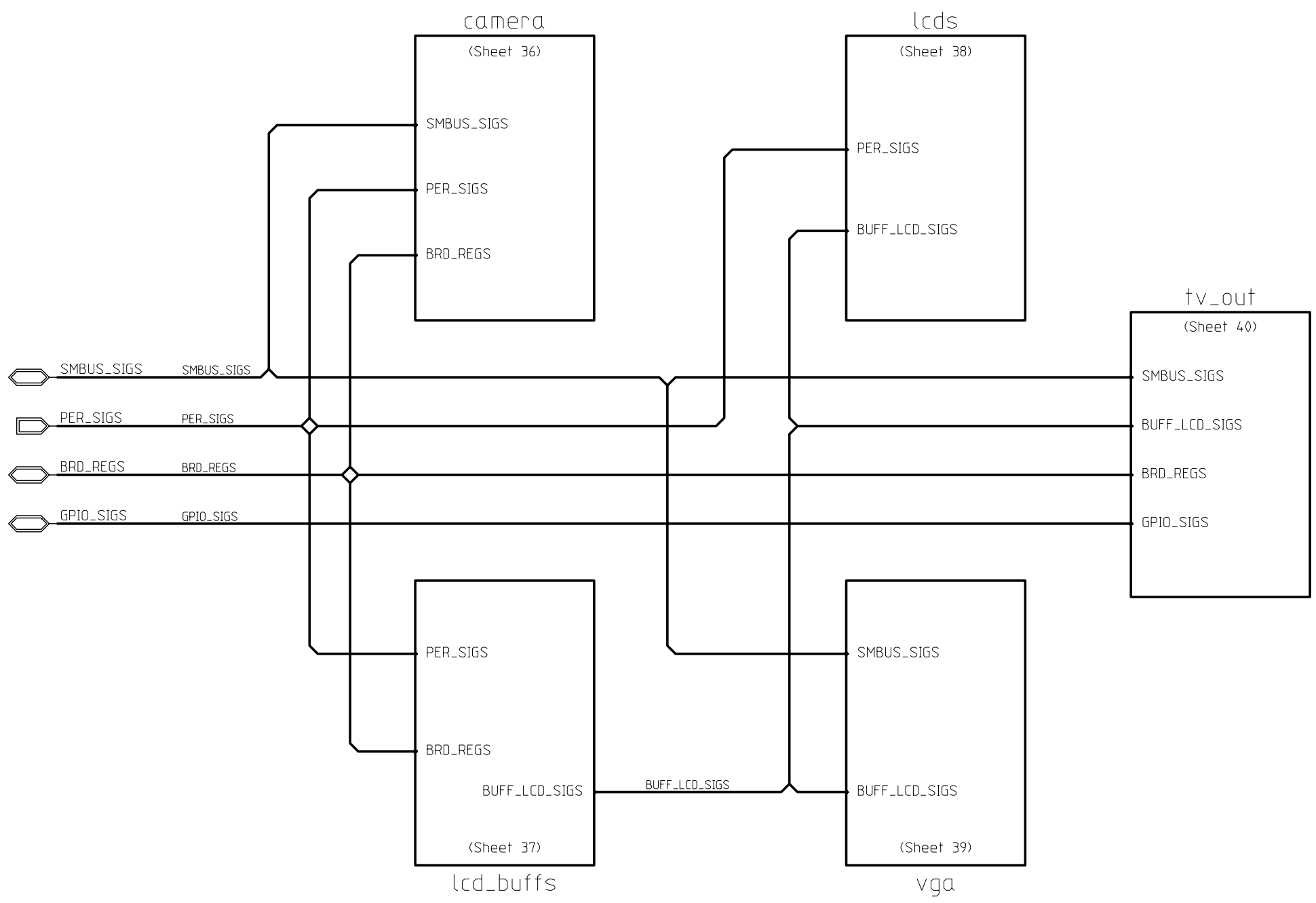


DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 34
Project: DBAu1200	Schematic: sd_card	REV 1



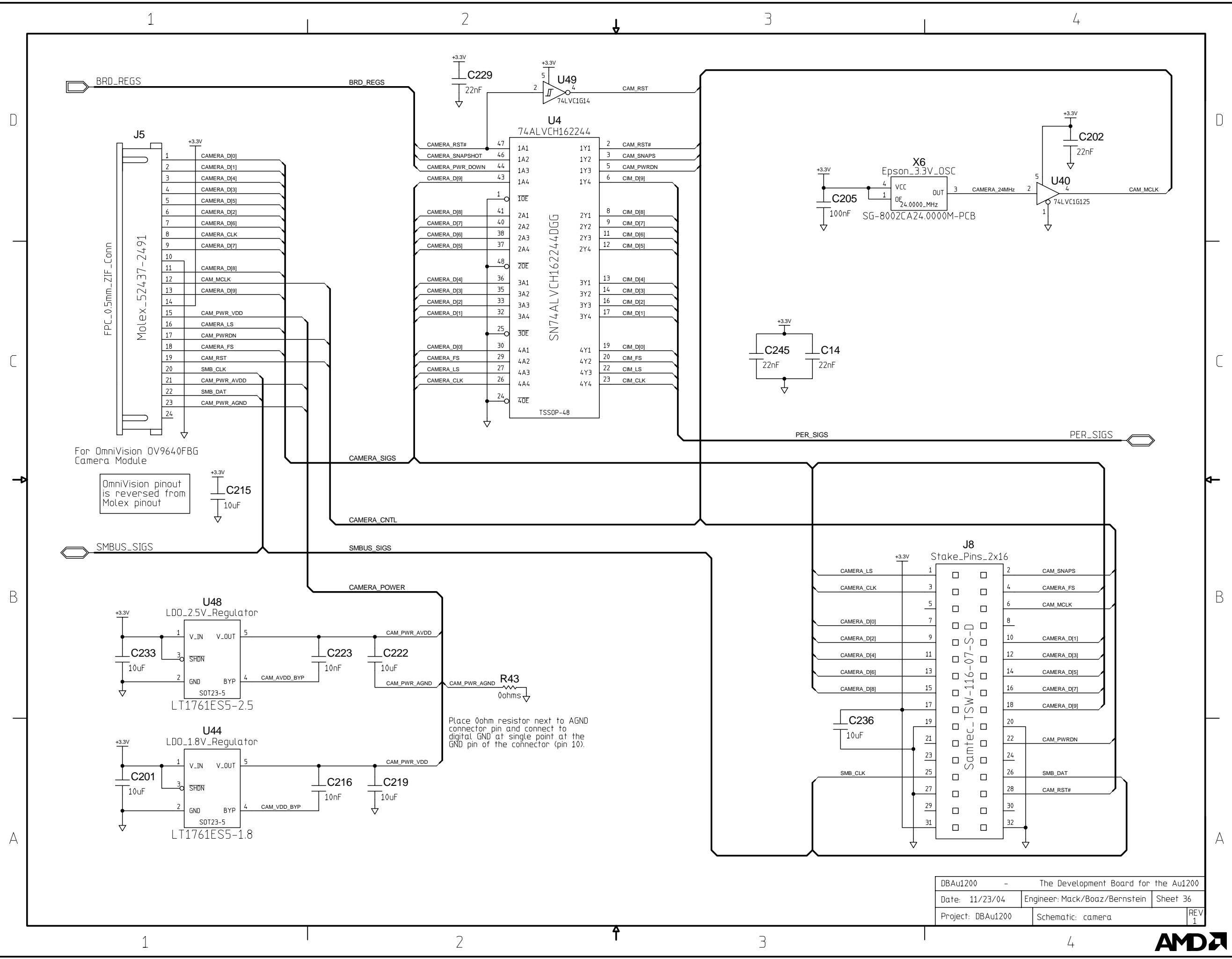
1 2 3 4

D C B A



DBAu1200 - The Development Board for the Au1200			
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 35	
Project: DBAu1200	Schematic: visual_interfaces	REV	1





DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: camera
REV 1	

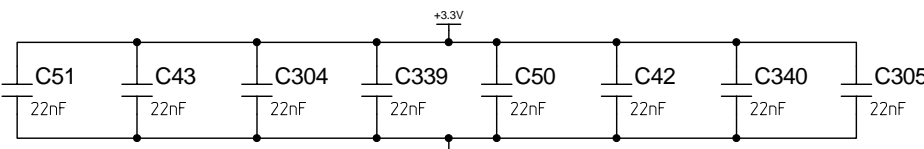
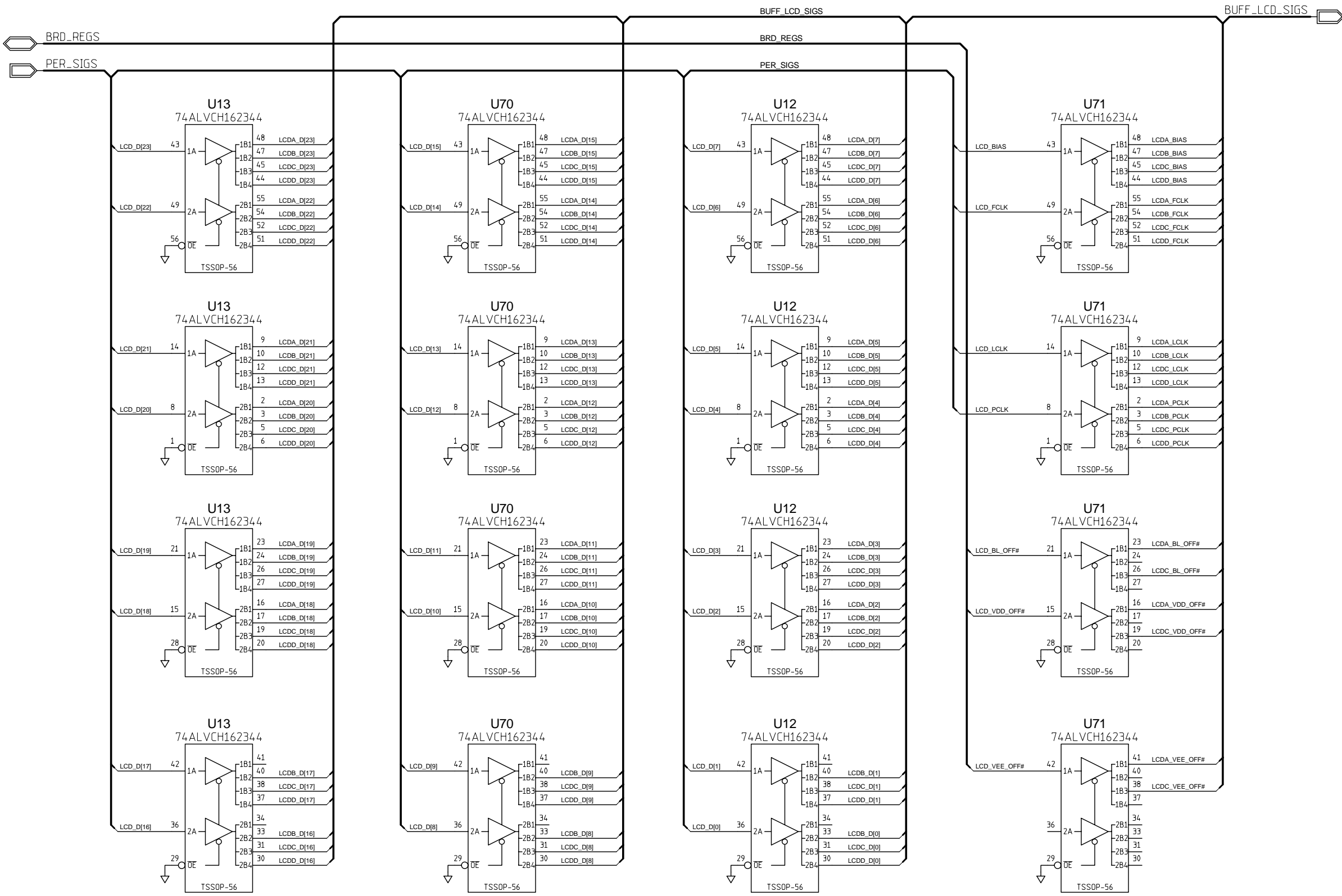


1

2

3

4



DBAu1200 - The Development Board for the Au1200			
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 37	
Project: DBAu1200	Schematic: lcd_buffers	REV 1	

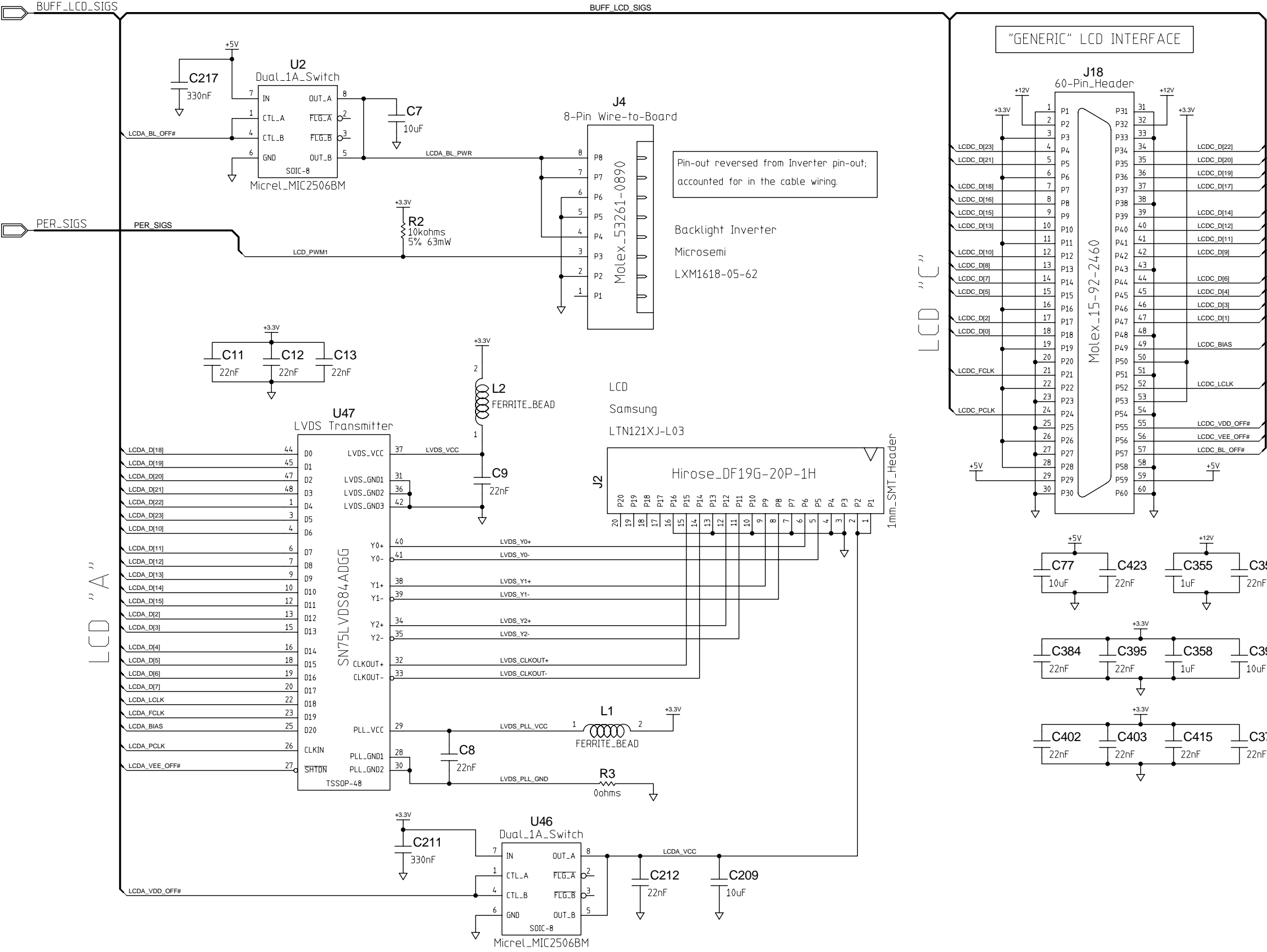


1

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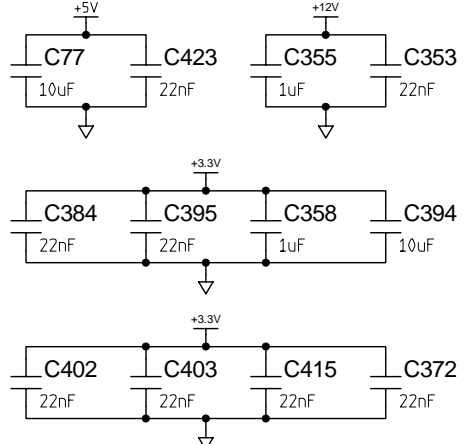
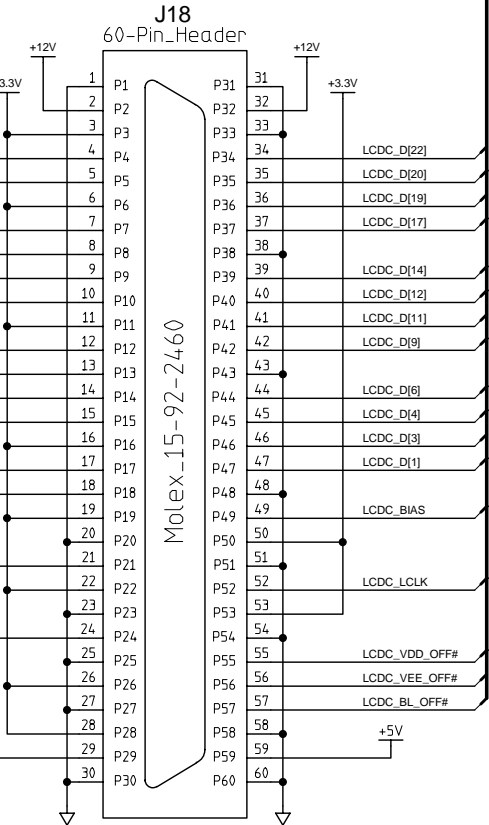


Pin-out reversed from Inverter pin-out;
accounted for in the cable wiring.

Backlight Inverter
Microsemi
LXM1618-05-62

LCD
Samsung
LTN121XJ-L03

"GENERIC" LCD INTERFACE



DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Sheet 38
Schematic: lcds	REV 1



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D

C

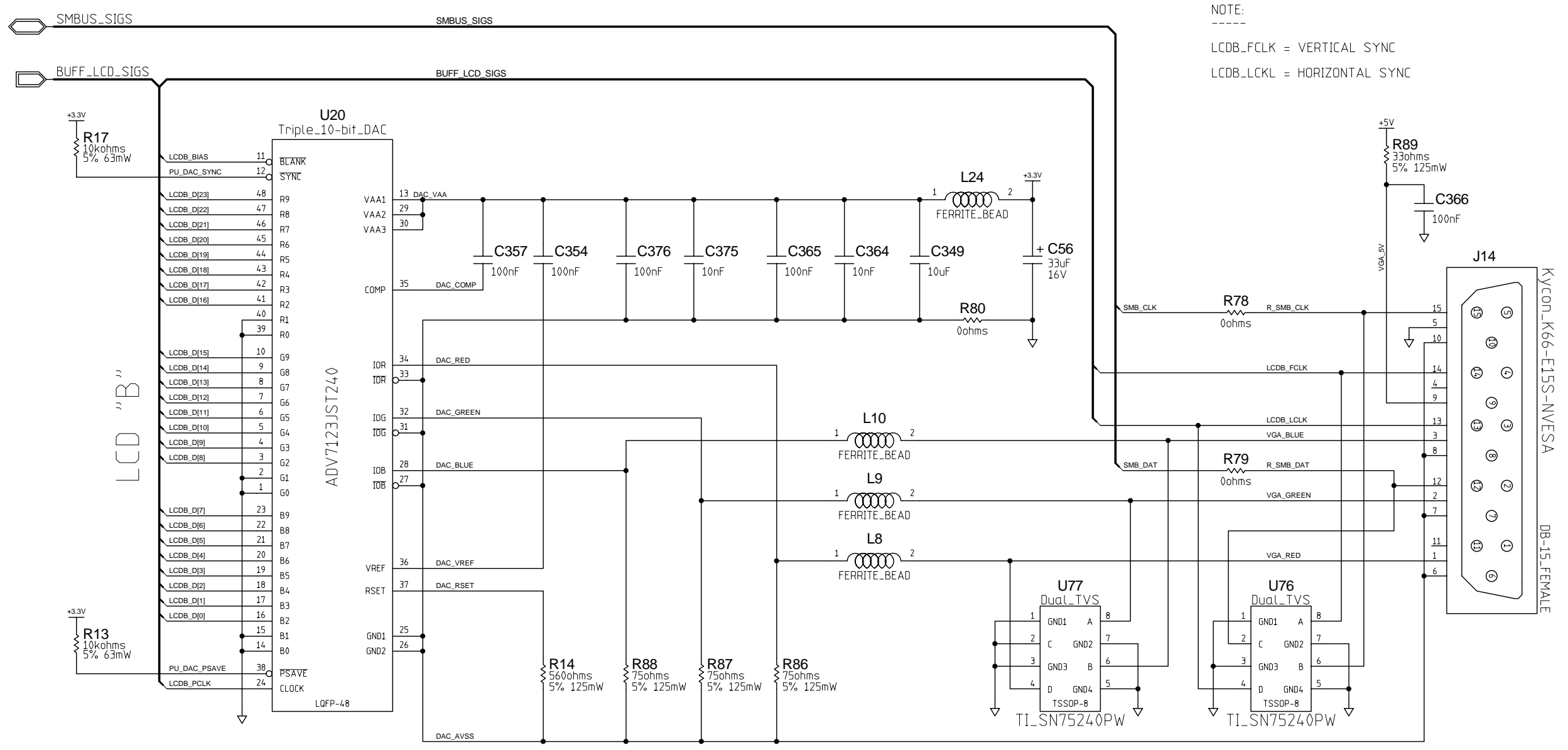
C

B

B

A

A



NOTE:

 LCDB_FCLK = VERTICAL SYNC
 LCDB_LCLK = HORIZONTAL SYNC

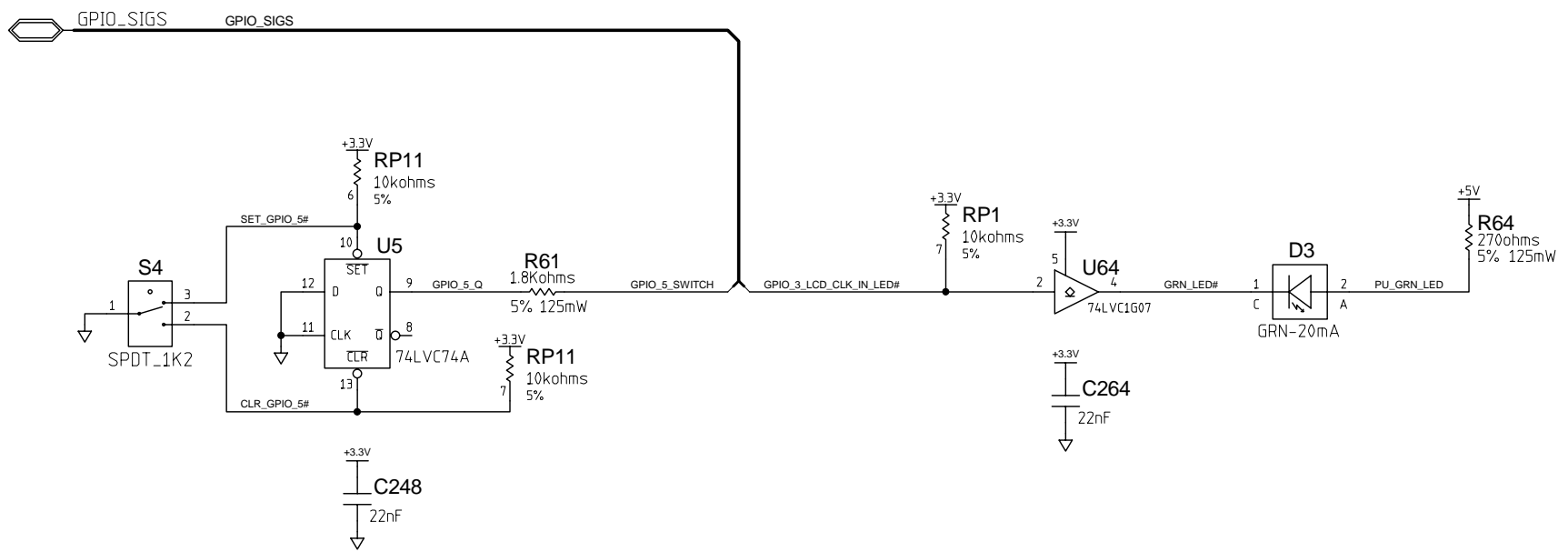
LCD "B"

ADV7123JST240

KYCON_K66-E15S-NVESA DB-15 FEMALE

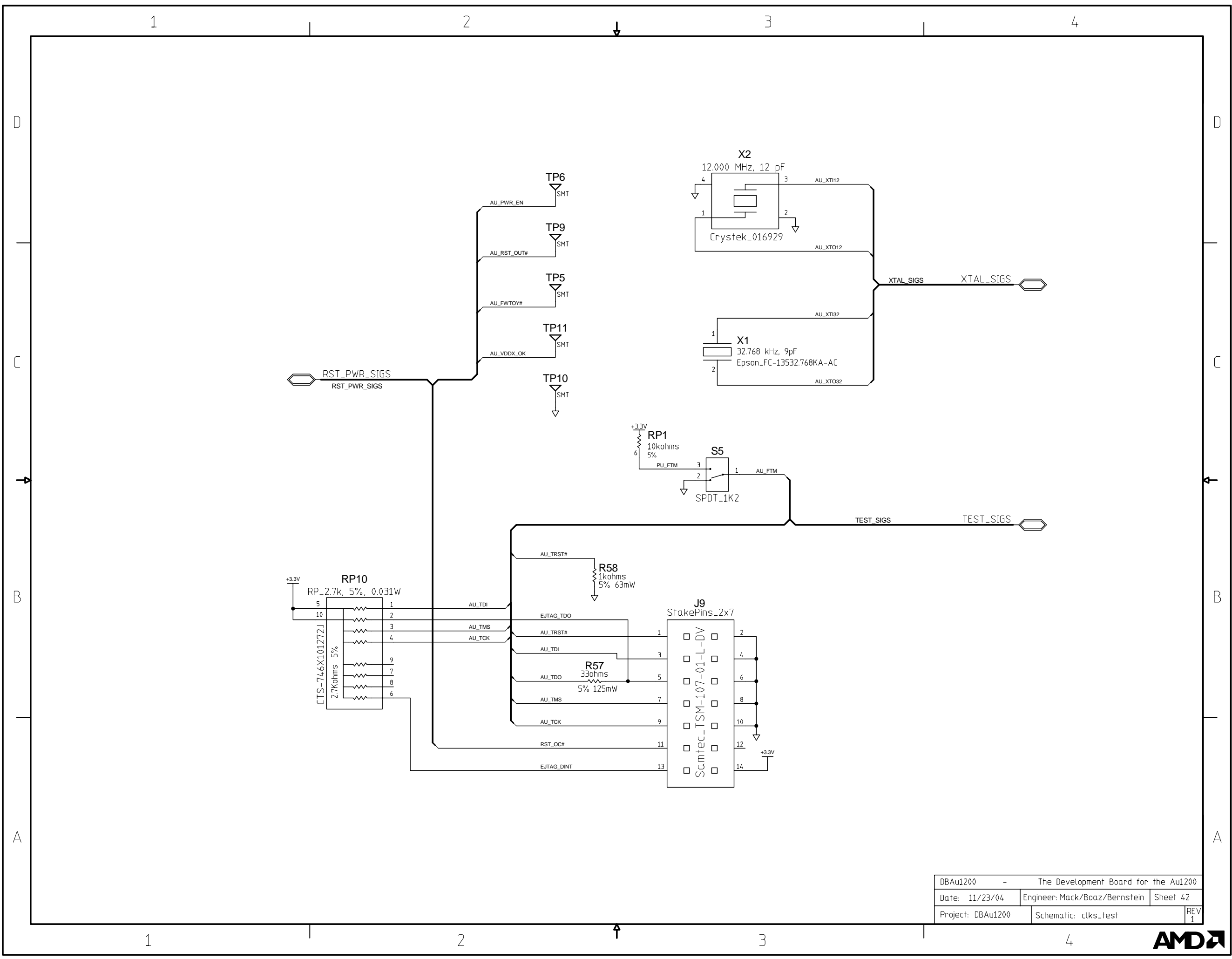
DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein Sheet 39
Project: DBAu1200	Schematic: vga
	REV 1





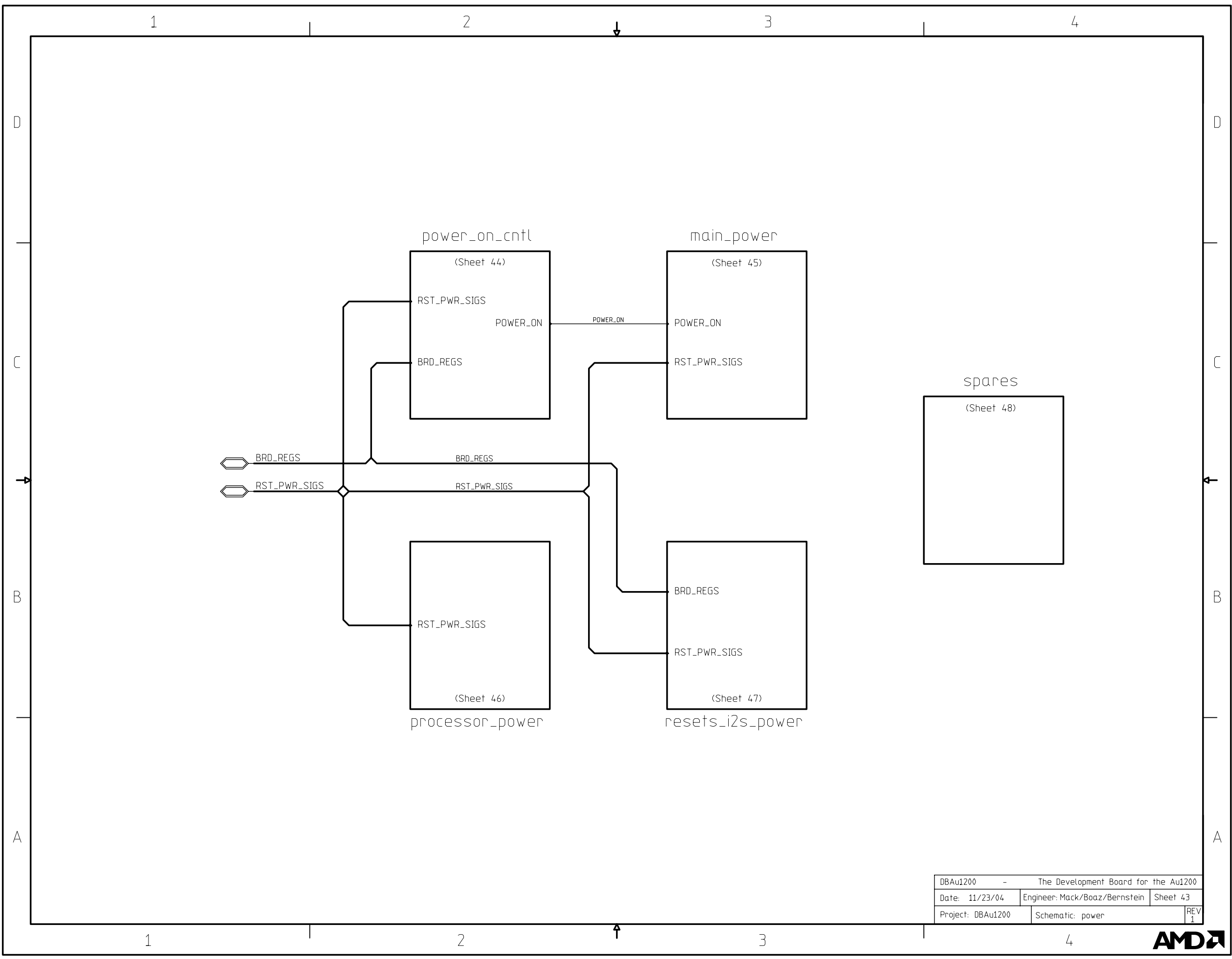
DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 41
Project: DBAu1200	Schematic: gpio_peripherals	REV 1





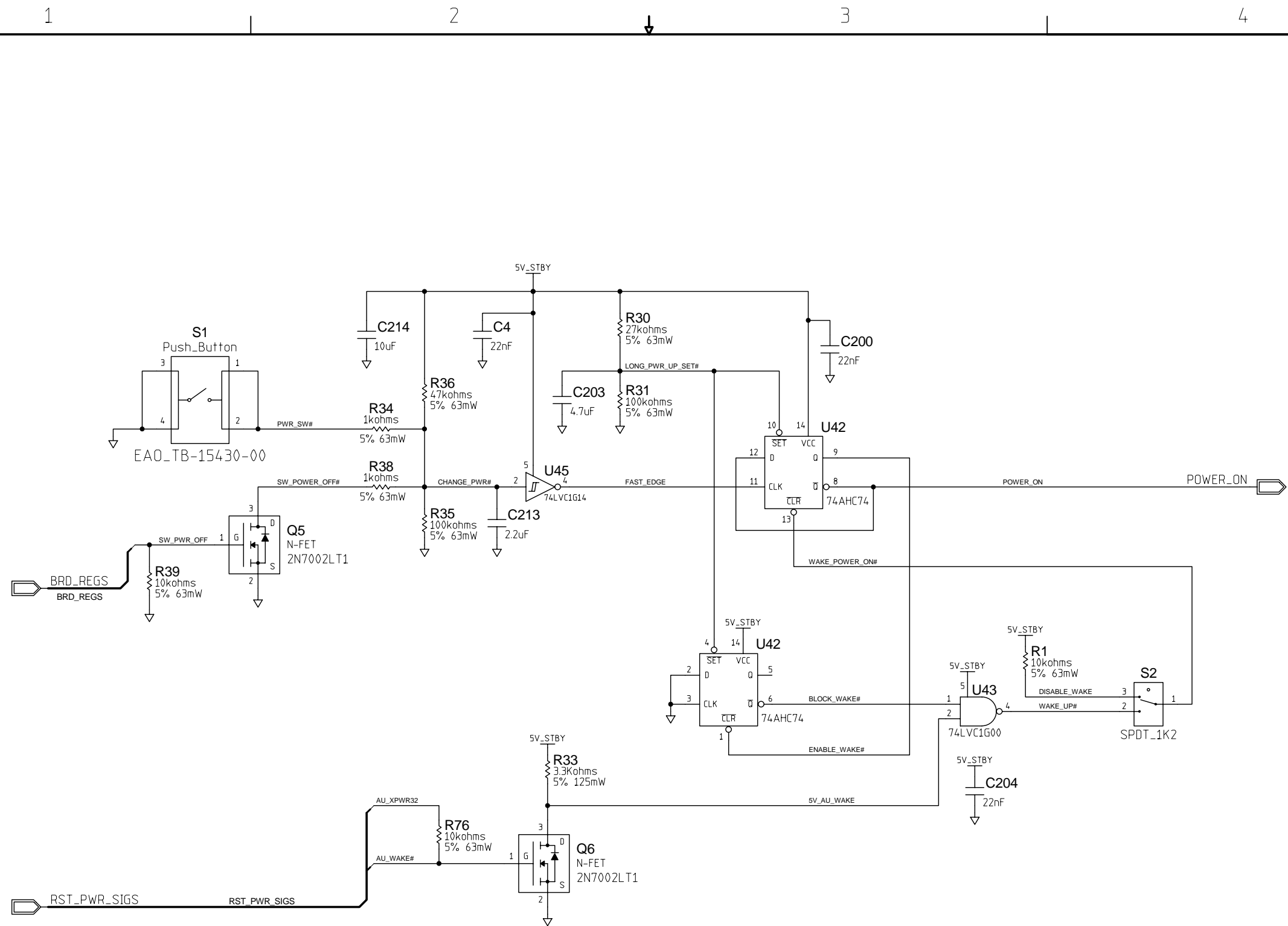
DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 42
Project: DBAu1200	Schematic: clks_test	REV 1





DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein Sheet 43
Project: DBAu1200	Schematic: power REV 1



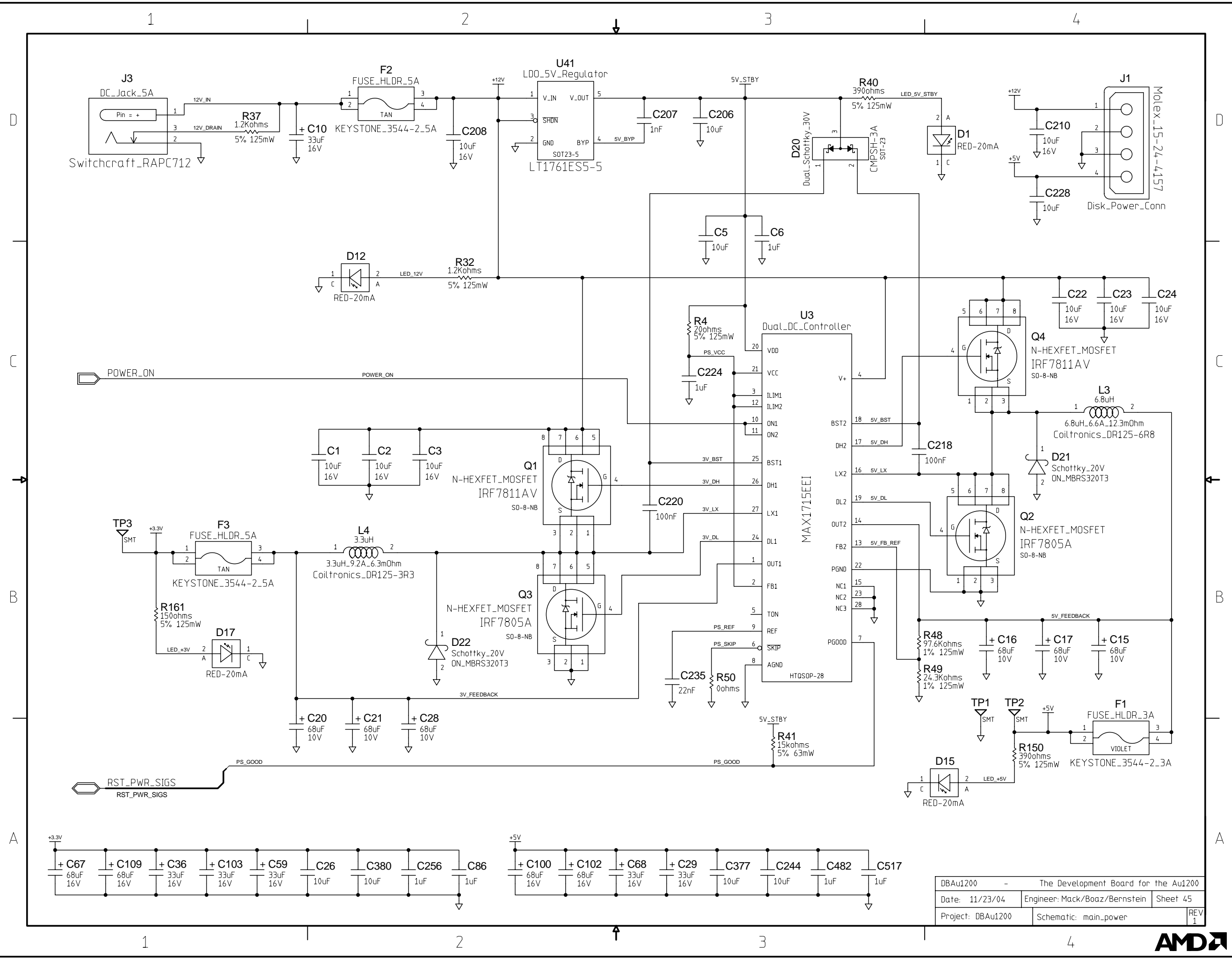


AU_WAKE# is blocked from being able to turn the system on, until it has been manually turned on at least once.

AU_WAKE# can only turn the system back on. It can never turn the system off.

DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: power_on_cntl
Sheet 44	REV 1

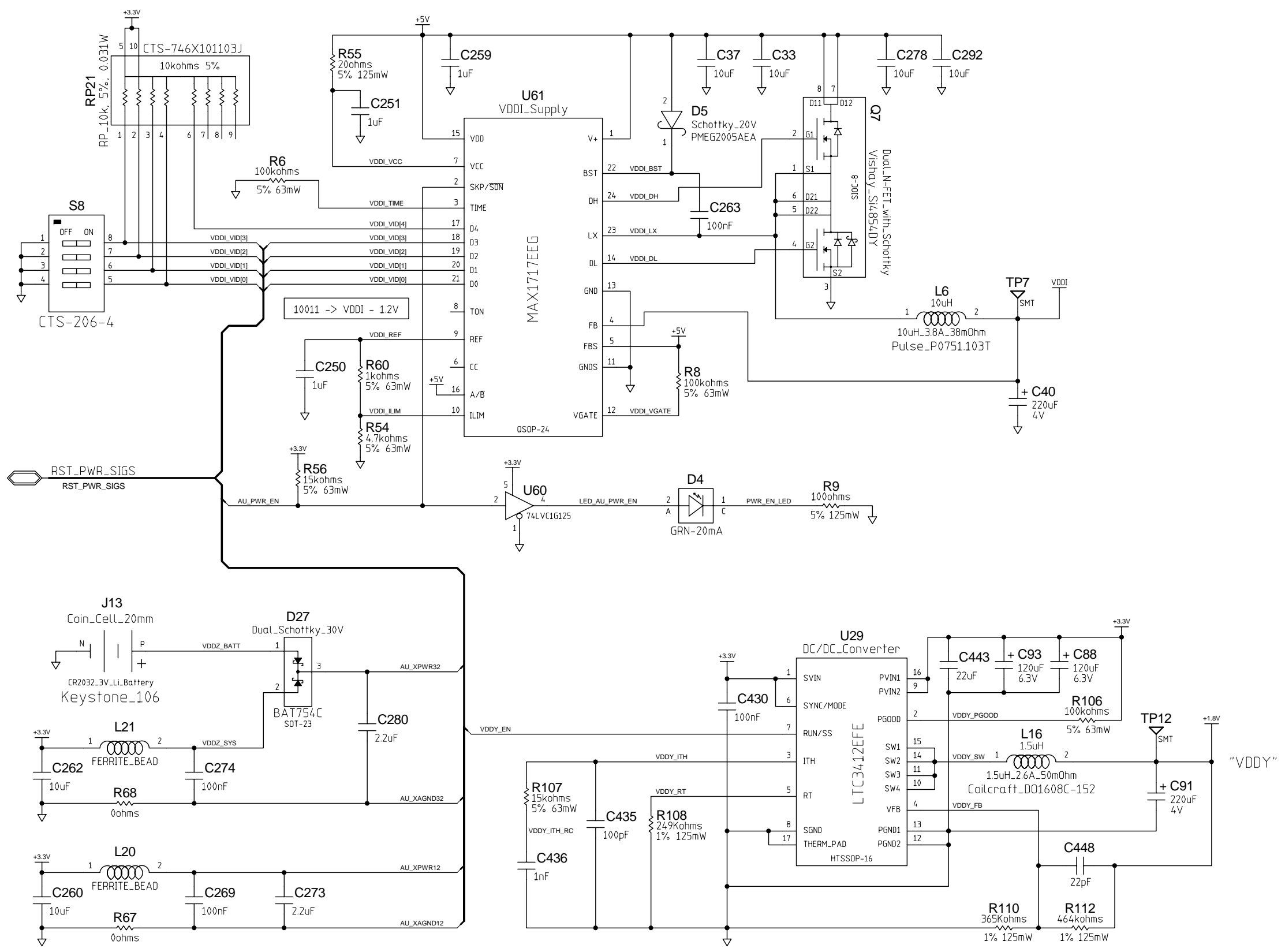




DBAu1200 - The Development Board for the Au1200	
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein
Project: DBAu1200	Schematic: main.power
Sheet 45	REV 1



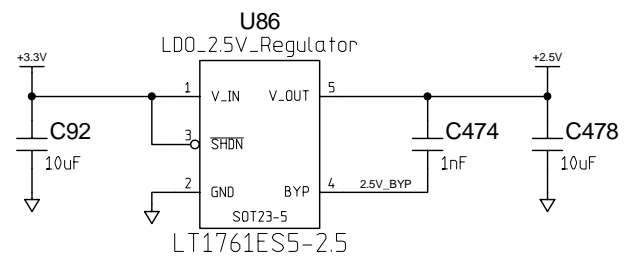
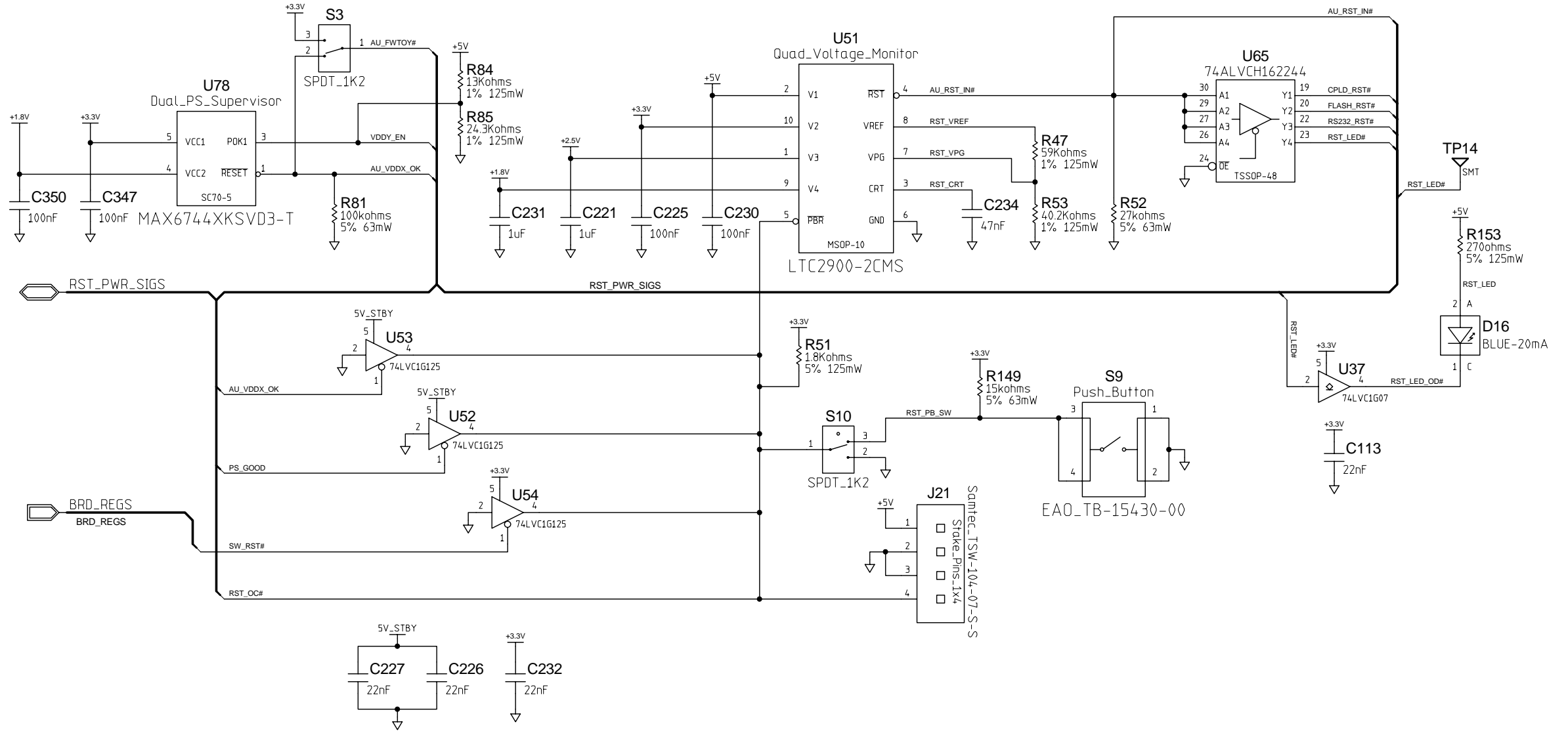
1 2 3 4



DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 46
Project: DBAu1200	Schematic: processor_power	REV 1



1 2 3 4



Provides +2.5V
for Wolfson WM8731
I2S Audio CODEC

DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 47
Project: DBAu1200	Schematic: resets_i2s_power	REV 1



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D

C

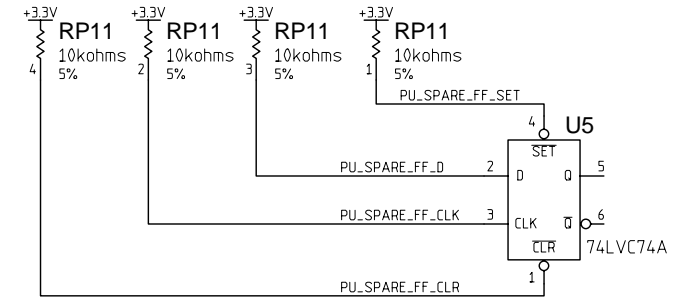
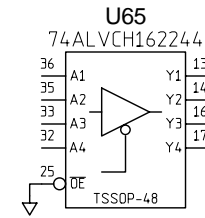
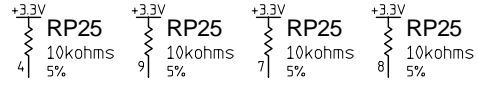
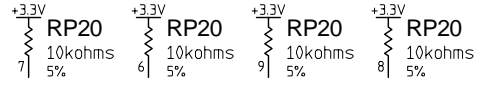
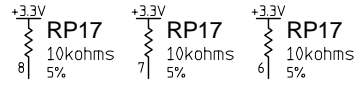
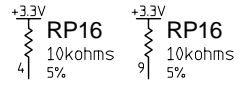
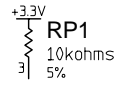
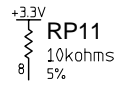
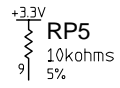
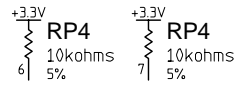
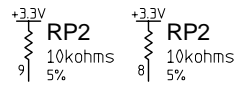
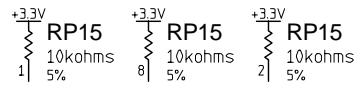
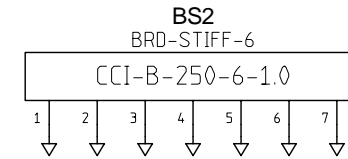
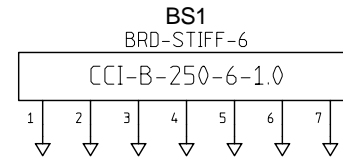
C

B

B

A

A



Pull-up Unused IC Inputs

DBAu1200 - The Development Board for the Au1200		
Date: 11/23/04	Engineer: Mack/Boaz/Bernstein	Sheet 48
Project: DBAu1200	Schematic: spares	REV 1

