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Purpose

The EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements manual provides the requirements for procedures and test equipment used for testing the analogue interface PCDs. These requirements are in accordance with the EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification Version 2.5, March 2015.

Audience

This manual is provided to:

- Testing Laboratories that perform PCD testing activities on behalf of EMVCo.
- Test Tools Vendors that produce EMVCo-compliant PCD Test Tools.

Overview

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<td>6 Preparation of the EMV Test Equipment</td>
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Using this Manual

Chapter Description

7 PCD Analogue Test Plan Describes the preparations and procedures for efficient and complete testing of PCDs supplied by a vendor. This includes descriptions of Type A and Type B transactions, how to set up the EMV – TEST PCD and EMV – TEST PICC for actual Test Bench operations and how to carry out the individual test cases for efficient and complete testing of PCDs supplied by a vendor.

A PCD Acceptance Criteria This appendix contains the values for acceptance criteria used during testing of a PCD.

B Set-up Values for EMV Test Equipment This appendix contains the test conditions used during testing of a PCD.

C PICC Emulation: Frame Trail This appendix contains details on frame trails used during testing of a PCD. Frame trails show the sequence of command events from a PCD and related PICC responses for testing the PCD receptivity.

D Reference Implementation This appendix contains details on a specific Test Bench implementation using the peak sampling method.

E Recommendations for Frame Delay Time Measurements This appendix contains important recommendations to maintain consistency across all laboratories in Frame Delay Time measurements.

Reference Documents

Specification and Standards Documents

- EMV Contactless Symbol Reproduction Requirements, Version 5, 20 April 2015
- EMVCo Type Approval Accreditation Requirements for EMVCo Terminal Type Approval Laboratories.
Laboratory Test Documents

The test documents to be applied by EMVCo accredited laboratories when performing an EMV Contactless Terminal Type Approval Level 1 session are listed in the following document:

**EMVCo Type Approval
Contactless Terminal Level 1
Laboratories Documentation**

Check the last version of this document for any update of the test documents.

Acronyms and Abbreviations

The following acronyms and abbreviations are used in this manual:

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<td>Analogue to Digital</td>
</tr>
<tr>
<td>AC CLn</td>
<td>Anticollision Cascade Level n, Type A</td>
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<td>ASK</td>
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<td>Clock</td>
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<td>CMR</td>
<td>Common Mode Rejection</td>
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<td>DIV</td>
<td>Division</td>
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<tr>
<td>DSO</td>
<td>Digital Sampling Oscilloscope</td>
</tr>
<tr>
<td>DTE</td>
<td>Device Test Environment</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic Compatibility</td>
</tr>
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<td>EMI</td>
<td>Electromagnetic Interference</td>
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<td>EoF</td>
<td>End of Frame</td>
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<td>End of Sequence</td>
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<td>End of Test</td>
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<tr>
<td>etu</td>
<td>Elementary time unit</td>
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<td>Subcarrier Frequency</td>
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<td>Halt Command, Type B</td>
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<td>Inter Integrated Circuit</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
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<td>ICS</td>
<td>Implementation Conformance Statement</td>
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<tr>
<td>IEC</td>
<td>International Electrotechnical Commission</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronic Engineers</td>
</tr>
<tr>
<td>MSa/s</td>
<td>Mega Samples / Second</td>
</tr>
<tr>
<td>PAN</td>
<td>Primary Account Number</td>
</tr>
<tr>
<td>PCD</td>
<td>Proximity Coupling Device</td>
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<tr>
<td>TTA</td>
<td>Terminal Type Approval</td>
</tr>
<tr>
<td>TTL</td>
<td>Transistor-Transistor Logic</td>
</tr>
<tr>
<td>UID</td>
<td>Unique Identifier, Type A</td>
</tr>
<tr>
<td>Vpp</td>
<td>Peak to Peak Amplitude Voltage</td>
</tr>
<tr>
<td>VSWR</td>
<td>Voltage Standing Wave Ratio</td>
</tr>
<tr>
<td>WUPA</td>
<td>Wake UP command, Type A</td>
</tr>
<tr>
<td>WUPB</td>
<td>Wake UP command, Type B</td>
</tr>
</tbody>
</table>
Units

All units in this document follow the International System of Units (SI) standard.

Notational Conventions

The following notational conventions apply:

<table>
<thead>
<tr>
<th>Notation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( z, r, \varphi, \theta )</td>
<td>These four coordinates define the position of the PICC in the Operating Volume. The coordinates ( z, r, ) and ( \varphi ) are the coordinates of the center of the Presentation Plane. The coordinate ( \theta ) is the angle between the ( \varphi=0 ) axis of the PCD, and the ( \varphi_c=0 ) axis of the PICC.</td>
</tr>
<tr>
<td>((zrf))</td>
<td>Position label indicating the values for coordinates ( z, r, \varphi ).</td>
</tr>
<tr>
<td>( xx )</td>
<td>Value.</td>
</tr>
</tbody>
</table>

Definitions

The following definitions are used in this manual:

<table>
<thead>
<tr>
<th>Definition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Mode Rejection (CMR) circuit board</td>
<td>A hardware device which conditions and switches signals between its inputs and outputs.</td>
</tr>
<tr>
<td>EMV – TEST CMR</td>
<td>A hardware device qualified as reference equipment which is used with other EMV Test Equipment. Its purpose is to condition and switch signals between its inputs and outputs.</td>
</tr>
<tr>
<td>EMV – TEST PCD</td>
<td>A hardware device qualified as reference equipment which is used with other EMV Test Equipment. Its purpose is to simulate a PCD.</td>
</tr>
<tr>
<td>EMV – TEST PICC</td>
<td>A hardware device qualified as reference equipment which is used with other EMV Test Equipment. Its purpose is to simulate a PICC.</td>
</tr>
<tr>
<td>Envelope</td>
<td>Waveform connecting positive or negative peaks of oscillating signal.</td>
</tr>
<tr>
<td>Landing Plane</td>
<td>The designated surface area of a PCD where a user should place a PICC to obtain a successful transaction.</td>
</tr>
<tr>
<td>Loopback mode</td>
<td>Loopback involves cycling back information in a channel. Any data transmitted through such a channel is immediately received by the same channel. A device is in loopback mode after such a mode has been activated.</td>
</tr>
<tr>
<td>Definition</td>
<td>Description</td>
</tr>
<tr>
<td>----------------------------------</td>
<td>------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Modulation Index</td>
<td>The modulation Index of an amplitude modulated signal is defined as $m_i = (</td>
</tr>
<tr>
<td>Operating Volume</td>
<td>The 3-dimensional space in which the EMV – TEST PCD shall reliably communicate with an EMV – TEST PICC by means of a magnetic field.</td>
</tr>
<tr>
<td>Polling</td>
<td>Sequence during which the PCD sends alternatively WUPA and WUPB commands until a response is received.</td>
</tr>
<tr>
<td>Presentation Plane</td>
<td>The plane on the EMV – TEST PICC that faces the EMV – TEST PCD.</td>
</tr>
<tr>
<td>Proximity Coupling Device (PCD)</td>
<td>A hardware device that uses inductive coupling to provide power to the PICC and exchange data with the PICC.</td>
</tr>
<tr>
<td>Proximity Integrated Circuit Card (PICC)</td>
<td>A hardware device containing an integrated circuit and capable of inductive coupling in the proximity of a coupling device.</td>
</tr>
<tr>
<td>Sample</td>
<td>A physical implementation of a PICC or a PCD delivered to the Testing Laboratory for testing.</td>
</tr>
<tr>
<td>Set-up</td>
<td>Procedure to follow to prepare EMV Test Equipment before starting a test.</td>
</tr>
<tr>
<td>Terminal</td>
<td>Any device used to interact with a PICC and which operates to the requirements of the <em>EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification</em>. This includes the PCD and may also include other components and interfaces.</td>
</tr>
<tr>
<td>Test Bench</td>
<td>A specific test bench as described in the in the EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements manual.</td>
</tr>
<tr>
<td>Test Case</td>
<td>Test to verify a requirement at a specific position in the Operating Volume.</td>
</tr>
<tr>
<td>Test Code</td>
<td>Code to identify a Test Case.</td>
</tr>
<tr>
<td>Testing Laboratory</td>
<td>A facility accredited by EMVCo for performing EMV Contactless testing of the analogue interface for PICCs and PCDs.</td>
</tr>
<tr>
<td>Transaction</td>
<td>A sequence of logic interactions that the PICC and the Terminal shall execute as foreseen by the EMV Contactless application. The transaction starts with the first logic message from the PCD to the PICC.</td>
</tr>
</tbody>
</table>
Word Usage

The following words are used often in this manual and have a specific meaning:

- **Shall** - Defines a capability which is mandatory.
- **May or Should** - Defines a capability which is optional or a statement which is informative only.

Support

For support regarding EMV Contactless analogue testing, refer to [www.emvco.com](http://www.emvco.com).
Requirements for Testing Laboratories

This chapter describes general requirements for Testing Laboratories.

1.1 Overview and Requirements

1.2 Accreditation Requirements

1.2.1 Using EMV Test Equipment

1.2.2 Creation of the Test Bench

1.2.3 Approval of the Test Bench

1.2.4 Test Bench Organization

1.2.5 Accreditation by EMVCo

1.2.6 Official Compliance to ISO 17025

1.3 Controlled Test Conditions

1.3.1 Power Supply Conditions

1.3.2 Temperature and Humidity

1.3.3 RF Environment

1.3.3.1 Interference Issues

1.3.3.2 Managing the RF Environment
1.1 Overview and Requirements

The EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements manual provides the Test Cases for testing of the analogue interface of terminals.

Analogue interface testing is one of the phases related to EMVCo Terminal Type Approval (TTA).

1.2 Accreditation Requirements

This section describes the requirements for passing full accreditation. Replacing the test equipment by any other devices voids accreditation for testing of the analogue interface for EMV Contactless products.

1.2.1 Using EMV Test Equipment

The EMV Test Equipment comprises the following:

1.2.1.1 EMV TEST Proximity Integrated Circuit Card

The EMV – TEST Proximity Integrated Circuit Card (PICC) emulates the radio frequency (RF) interface of an EMV Contactless card.

1.2.1.2 EMV TEST Proximity Coupling Device

The EMV – TEST Proximity Coupling Device (PCD) emulates the RF interface of a EMV Contactless terminal.

1.2.1.3 EMV TEST Common Mode Rejection Circuit Board

The EMV – TEST Common Mode Rejection (CMR) circuit board aims at conditioning signals and switching them between its inputs and outputs for Test Bench set-ups.

1.2.2 Creation of the Test Bench

Each Testing Laboratory shall create its own proprietary test bench connected to three test devices:

- The EMV – TEST PICC
- The EMV – TEST PCD
- The EMV – TEST CMR

1.2.3 Approval of the Test Bench

The complete test bench shall be approved by EMVCo before the Testing Laboratory is allowed to provide official type approval testing services to PCD vendors.
1.2.4 Test Bench Organization

The Test Bench shall be governed by standard operating procedures. These procedures shall include:

- Calibration
- Operator training
- Test bench operation
- Test bench maintenance

1.2.4.1 Calibration

Each item of measurement equipment shall be calibrated according to its calibration guidelines once a year.

In any case, calibration shall be performed and documented in compliance with ISO / IEC 17025:2005 - General Requirements for the Competence of Calibration and Testing Laboratories.

1.2.4.2 Operator Training

The Testing Laboratory shall ensure operator training to establish the required level of skills and expertise prior to any testing operations.

To ensure the quality of testing, it is recommended that additional training be provided to personnel at least once per year and that close attention be paid to customer requirements.

1.2.4.3 Test Bench Operation

The Testing Laboratory shall prepare and maintain documentation covering all relevant aspects of the design, implementation and operation of its proprietary Test Bench and its interaction with EMV Test Equipment that are necessary for correct operation.

The Testing Laboratory shall operate the Test Bench in accordance with this documentation.

1.2.4.4 Test Bench Maintenance

Each piece of measuring equipment shall undergo regular preventive maintenance, as required by its operating specifications. Written records of such maintenance operations shall be kept by the Testing Laboratory.

In case of test bench failure, corrective maintenance shall take place to repair the test bench. The repaired test bench instruments and accessories shall be restored to their original Testing Laboratory approved standard performance levels. Written records of maintenance operations shall also be kept by the Testing Laboratory.
1.2.5 Accreditation by EMVCo

Only Testing Laboratories that are accredited by EMVCo are authorized to perform EMV analogue interface testing.

1.2.6 Official Compliance to ISO 17025

The Testing Laboratory shall prove to EMVCo that they operate their test bench in compliance with ISO/IEC 17025:2005 - General Requirements for the Competence of Calibration and Testing Laboratories.

Also refer to the EMVCo Type Approval Accreditation Requirements for EMVCo Terminal Type Approval Laboratories document for additional accreditation requirements.

1.3 Controlled Test Conditions

Analogue Interface testing shall be carried out under controlled test conditions. Refer to ISO/IEC 17025, section 5.3 and 5.4 for details.

1.3.1 Power Supply Conditions

At the beginning of a test session, the Testing Laboratory shall ensure that all electrical power supplies are within the range required for their purpose.

Power Supply voltage shall be measured with calibrated measurement equipment while the Power Supply is connected to the load.

1.3.2 Temperature and Humidity

The normal temperature and humidity conditions for analogue tests should be any convenient combination of temperature and humidity within the following ranges:

- Temperature: 23°C ± 3°C
- Relative humidity: 40 % to 60 %

When it is impossible to perform tests under these conditions, a note to this effect, stating the ambient temperature and relative humidity during the tests, shall be added to the test report.

1.3.3 RF Environment

1.3.3.1 Interference Issues

Electromagnetic Interference (EMI) appears in many different forms. The most prominent in Testing Laboratories are the intentional radiators, such as other PCDs under test and other communication devices in the 1 to 100 MHz range of the RF
spectrum. In addition, cordless telephones and mobile telephones can be significant interferers in Testing Laboratories.

Another form of interference is EMI radiated from incidental sources: devices and/or systems that are not designed to transmit intentionally. Such interference is also known as broadband emission or “noise,” and may be generated by any electronic or electrical device and/or system. This interference may lead to incorrect measurements.

Extraneous noise may radiate from many sources. These are so numerous that it is virtually impossible for all of these suspected devices to be completely managed or controlled. However, efforts must be made to restrict the level of interference signals coming from these sources. The laboratory shall have ISO/IEC 17025 compliant procedures in place to monitor and control the RF environment to ensure that it does not adversely affect the quality of the measurements covered in this document.

1.3.3.2 Managing the RF Environment

The RF spectrum (from 1 to 100 MHz) should be managed by documenting all frequencies as follows:

- Using a spectrum analyzer for initial benchmarking of the level, nature, and impact of conducted and radiated RF signals that may affect the reliability of measurements.
- Recording critical frequencies of other Testing Laboratory devices and/or systems.
- Preventing the intrusion of interfering sources into vulnerable test frequencies (always scan for noise as well as intentional transmitters).
- Managing this information and knowing which frequencies are in use in the environment.
- Scanning the Testing Laboratory environment regularly for possible broadband emissions, especially in areas where PCDs are in use or under test.

**Note**

Equipment such as computers and power supplies should be selected to be as quiet as possible in terms of electro-magnetic disturbances towards the Test bench.

**Note**

Cables connected to Test Bench equipment shall be as short as possible, ideally less than 50 cm. However, cables connected to computers and power supplies may have a length of up to 100 cm. This allows physical separation of the equipment to minimize coupling of electromagnetic disturbances to sensitive components of the Test Bench.
Positioning Conventions and Requirements

This chapter introduces the conventions for describing the position of the EMV – TEST PICC relative to the EMV – TEST PCD during the setup. It also presents the positioning of EMV Test Equipment relative to the samples used in testing operations. These positioning conventions and requirements are essential for accurate and consistent test results.

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  2.2.2 Positioning Characteristics for the EMV TEST PICC........................................... 2-2
  2.2.3 Relative Positioning of the EMV TEST PICC and EMV TEST PCD............... 2-3
    2.2.3.1 Definition of φ Angle Coordinate............................................................... 2-5
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2.5 Positioning Accuracy ........................................................................................................ 2-10
2.1 Importance of Positioning

The correct positioning of PICCs and PCDs during testing is of critical importance with EMV Contactless technology, due to the fact that:

- PCDs come in many forms, such as a standard terminal in a retail location, a card reader in front of a public transport turnstile, a wireless hand-held device, etc.
- The cardholder can either tap the PICC onto the PCD or simply wave it in front of the PCD.

It is very important to understand the positioning characteristics applied to PICCs and PCDs and the relationship of these positioning characteristics to the Operating Volume. This ensures successful and repeatable testing of the various PICCs and PCDs available on the market.

2.2 Conventions Regarding Positioning

For best accuracy and consistency in testing PCDs, the position of the device must be precisely set. This section explains this using the EMV – TEST PCD and the EMV – TEST PICC during the set-up. The same conventions apply to testing of PCDs in general.

2.2.1 Positioning Characteristics for the EMV TEST PCD

The EMV – TEST PCD clearly identifies where a user should position a PICC to obtain a successful transaction. The designated surface area of a EMV – TEST PCD near which a PICC user should position a PICC to obtain a successful transaction is referred to as the Landing Plane.
Figure 2.1 shows the EMV – TEST PCD positioning characteristics:

The conventions used in this chapter relate to Appendix C of the *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification*.

The Z axis of the EMV – TEST PCD is the axis which passes through the center of the Landing Plane. The Z axis is orthogonal to the Landing Plane and points outwards from the EMV – TEST PCD Landing Plane top surface.

The $\varphi=0$ axis is an axis defined on the Landing Plane to support the indication of the orientation of the EMV – TEST PICC versus the EMV – TEST PCD. In theory, the $\varphi=0$ axis is the writing direction of the EMV – TEST PCD.

For testing, the PCD under test shall have markings for the center of the Landing Plane (Contactless symbol) and the direction of the $\varphi=0$ axis.

### 2.2.2 Positioning Characteristics for the EMV TEST PICC

When the EMV – TEST PICC is presented over the Landing Plane of the EMV – TEST PCD, the plane on the EMV – TEST PICC that faces the EMV – TEST PCD is called the Presentation Plane.
Figure 2.2 shows the EMV – TEST PICC positioning characteristics:

![EMV - TEST PICC Positioning Characteristics](image)

The Presentation Plane is on the bottom surface of the PICC (dotted lines).

The $Z_c$ axis of the EMV – TEST PICC is an axis which passes through the center of the Presentation Plane. This axis is also orthogonal to the Presentation Plane and points outwards from the EMV – TEST PICC Presentation Plane’s bottom surface.

The point on the Presentation Plane where the $Z_c$ axis begins is called the center of the Presentation Plane.

The $\phi_c=0$ axis is the axis defined on the Presentation Plane to identify the orientation of the EMV – TEST PICC versus the EMV – TEST PCD.

### 2.2.3 Relative Positioning of the EMV TEST PICC and EMV TEST PCD

When an EMV – TEST PICC is placed directly above an EMV- TEST PCD, communication is ideally obtained when both the Landing Plane of the PCD and Presentation Plane of the EMV – TEST PICC are perfectly parallel and aligned. This means that the $Z$ axis of the EMV – TEST PCD passes through the center of the Presentation Plane of the EMV – TEST PICC and that the $Z_c$ axis of the EMV – TEST PICC passes through the center of the Landing Plane of the EMV – TEST PCD.
Figure 2.3 shows the relative positioning of an EMV – TEST PICC and EMV – TEST PCD when both are perfectly aligned and parallel:

The position of the EMV – TEST PICC relative to the EMV – TEST PCD is defined with four coordinates (z, r, φ and θ), as shown in Table 2.1:

<table>
<thead>
<tr>
<th>Coordinate</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>z</td>
<td>Coordinate starting at the center of the Presentation Plane:</td>
<td>mm</td>
</tr>
<tr>
<td></td>
<td>a point along the Z axis.</td>
<td></td>
</tr>
<tr>
<td>r</td>
<td>Coordinate starting at the center of the Presentation Plane:</td>
<td>mm</td>
</tr>
<tr>
<td></td>
<td>a point along the radius defined from the center of the Presentation Plane</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(for example 25 mm).</td>
<td></td>
</tr>
<tr>
<td>φ</td>
<td>Coordinate starting at the center of the Presentation Plane:</td>
<td>Radians</td>
</tr>
<tr>
<td></td>
<td>this coordinate is explained in section 2.2.3.1</td>
<td></td>
</tr>
<tr>
<td>θ</td>
<td>Angle defining the orientation of the EMV – TEST PICC with respect to the</td>
<td>Radians</td>
</tr>
<tr>
<td></td>
<td>EMV – TEST PCD. This coordinate is explained in section 2.2.3.2</td>
<td></td>
</tr>
</tbody>
</table>

Table 2.1—Positioning Coordinate Definitions
2.2.3.1 Definition of $\phi$ Angle Coordinate

Figure 2.4 shows four possible positions of an EMV – TEST PICC:

- The $z$ coordinate is a fixed value for all four positions of the EMV – TEST PICC.
- The $r$ coordinate is 25 mm for all four positions of the EMV – TEST PICC.
- The $\phi$ coordinate varies for all four positions of the EMV – TEST PICC.
- The $\theta$ angle is 0 radians for all four positions of the EMV – TEST PICC. As a result, the EMV – TEST PICC is perfectly parallel to the EMV – TEST PCD in any of the four positions.

In this example, to clearly indicate the effect of the $\phi$ coordinate, all other coordinates have fixed values. Only the position of the center point of the coordinate changes. The $r$ and $\phi$ coordinates identify the center of the EMV – TEST PICC that is horizontal to the Landing Plane of the EMV – TEST PCD. When the values for the $r$ and $\phi$ coordinates vary over their complete range, the entire surface of the EMV – TEST PCD can be swept by the EMV – TEST PICC.
2.2.3.2 Definition of the $\theta$ Angle Coordinate

When an EMV – TEST PICC is placed directly above an EMV – TEST PCD, valid communication is also required when the Landing Plane of the EMV – TEST PCD and the Presentation Plane of the EMV – TEST PICC do not perfectly match but are rotated with respect to each other.

This means that an angle $\theta$ is created between the $\phi=0$ axis of the EMV – TEST PCD and the $\phi_c=0$ axis of the EMV – TEST PICC.

Figure 2.5 shows what happens when the relationship between the $\phi=0$ axis of the EMV – TEST PCD and the $\phi_c=0$ axis of the EMV – TEST PICC changes:

![Figure 2.5—Change of the Relationship between the $\phi=0$ Axis of the EMV – TEST PCD and the $\phi_c=0$ Axis of the EMV – TEST PICC](image)

The angle $\theta$ expresses the difference between the two axes.

To completely define all acceptable positions for the EMV – TEST PICC, the position of the center point of its Presentation Plane shall be within a defined Operating Volume above the EMV – TEST PCD Landing Plane. The origin of the Operating Volume is the point in the center of the contactless symbol of the EMV – TEST PCD. The Operating Volume is explained in the next section.
2.3 Operating Volume

The Operating Volume defines all the positions for valid testing measurements. The Operating Volume for an EMV – TEST PICC and EMV – TEST PCD is the 3-dimensional space in which the EMV – TEST PCD can reliably communicate with an EMV – TEST PICC by means of a magnetic field. Figure 2.6 shows the Operating Volume:

![Operating Volume Diagram]

The Operating Volume is measured from the center of the Landing Plane, along an axis perpendicular to the Landing Plane (the Z axis).

The requirements relating to the Operating Volume assume that the EMV – TEST PCD is stationary (fixed Landing Plane) and that the EMV – TEST PICC moves through the Operating Volume.

For further information, see section 2.4 of *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification*.

Note: The Operating Volume for an EMV – TEST PICC and EMV – TEST PCD also applies to all PCDs under test.
2.4 Positioning During Actual Setups and Tests

From here on in this chapter, the term EMV – TEST PICC refers to the EMV Test Equipment only while the term PCD refers to generic devices including devices used in tests.

The exact position of any EMV – TEST PICC or PCD during setup and testing is defined by two basic aspects:

- The position of these devices, as explained in section 2.2
- The Operating Volume, as explained in section 2.3

In actual PCD testing, two additional factors shall be taken into account:

- The EMV – TEST PICC is not rotated with respect to the PCD.
- Target Position Conventions are used for the location points on the positioning tool. This simplifies position labeling.

2.4.1 Target Position Conventions

While four coordinates fully define the exact position of any EMV – TEST PICC, the $\theta$ angle is not necessary as it is a fixed value used for all testing operations ($\theta=0$).

The Presentation Plane $(z, r, \phi)$ coordinates are the only ones needed.

To further simplify the labels corresponding to the coordinates, the position of any PICC is described with the coordinates of the Presentation Plane $(z, r, \phi)$ converted to a position label $(z, r, f)$ using simple identifiers.

Table 2.2, Table 2.3 and Table 2.4 show the equivalences between the values for the $z$, $r$ and $\phi$ coordinates and the identifiers used for labels:

<table>
<thead>
<tr>
<th>Value of Coordinate $z$</th>
<th>Value of $z$ Identifiers for Label Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 mm</td>
<td>0</td>
</tr>
<tr>
<td>10 mm</td>
<td>1</td>
</tr>
<tr>
<td>20 mm</td>
<td>2</td>
</tr>
<tr>
<td>30 mm</td>
<td>3</td>
</tr>
<tr>
<td>40 mm</td>
<td>4</td>
</tr>
</tbody>
</table>

The identifier $z$ is a code for the distance $z$.

Table 2.2—$z$ Values and Associated $z$ Identifiers
The identifier \( r \) is a code for the distance \( r \).

**Table 2.3—\( r \) Values and Associated \( r \) Identifiers**

<table>
<thead>
<tr>
<th>Value of Coordinate ( r )</th>
<th>Value of ( r ) Identifiers for Label Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 mm</td>
<td>0</td>
</tr>
<tr>
<td>15 mm</td>
<td>1</td>
</tr>
<tr>
<td>25 mm</td>
<td>2</td>
</tr>
</tbody>
</table>

The identifier \( f \) is a code for the angle \( \phi \).

**Table 2.4—\( \phi \) Values and Associated \( f \) Identifiers**

<table>
<thead>
<tr>
<th>Value of Coordinate ( \phi )</th>
<th>Value of ( f ) Identifiers for Label Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( \pi /2 )</td>
<td>3</td>
</tr>
<tr>
<td>( \pi )</td>
<td>6</td>
</tr>
<tr>
<td>( 3\pi /2 )</td>
<td>9</td>
</tr>
</tbody>
</table>

For example, Figure 2.7 shows nine identifiers corresponding to the label points in a plane of the target position for a given value of \( z \) with respect to the Landing Plane of the PCD:

![Figure 2.7—Label Points in a Plane of the Target Position](image)
Table 2.5 shows how the various points defined by a label point identifier match the previously described EMV – TEST PICC positions:

<table>
<thead>
<tr>
<th>Label Point Identifier</th>
<th>$\phi$ Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$z00$</td>
<td>—</td>
</tr>
<tr>
<td>$z10, z20$</td>
<td>0</td>
</tr>
<tr>
<td>$z13, z23$</td>
<td>$\pi/2$</td>
</tr>
<tr>
<td>$z16, z26$</td>
<td>$\pi$</td>
</tr>
<tr>
<td>$z19, z29$</td>
<td>$3\pi/2$</td>
</tr>
</tbody>
</table>

Table 2.5—Label Point Identifiers and Associated $\phi$ Value

2.4.2 Summary

For the purpose of the tests described in this manual, the PCDs under test shall be used with these recommendations:

- The Presentation Plane of an EMV – TEST PICC shall always be parallel to the Landing Plane of the PCD.
- The EMV – TEST PICC is not rotated with respect to the PCD.

2.5 Positioning Accuracy

The accuracy of the positioning during the test session shall be as follows:

- Accuracy on $z$ and $r = \pm 1$ mm
- Accuracy on $\phi$ and $\theta = \pm 0.1$ radian

A non-metallic positioning tool shall be used to avoid influencing electro-magnetic fields.
EMV Test Equipment

This chapter describes the EMV Test Equipment.

There are three types of EMV Test Equipment:

- The EMV – TEST PICC: used to test PCD capability.
- The EMV – TEST PCD: used to test PICC capability.
- The EMV – TEST CMR: used to condition and switch signals between its inputs and outputs.

Test equipment ensures the accuracy of all future PICC and PCD testing operations.

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  3.1.1 Description.............................................................................................................. 3-1
  3.1.2 Electrical Connectivity......................................................................................... 3-1
  3.1.3 Positioning Characteristics................................................................................. 3-3
  3.1.4 On-board Adjustment.......................................................................................... 3-3

3.2 EMV TEST PCD................................................................................................................ 3-5
  3.2.1 Description.............................................................................................................. 3-5
  3.2.2 Electrical Connectivity......................................................................................... 3-6
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3.1 EMV TEST PICC

3.1.1 Description

Figure 3.1 shows the EMV – TEST PICC, Version 2.1:

![Figure 3.1—EMV – TEST PICC, Version 2.1](image)

The EMV – TEST PICC comprises the PICC pickup coil (based on a design by the LETI laboratory) and the EMV – TEST PICC antenna.

The EMV – TEST PICC antenna has a circuit that tunes the antenna, rectifies the RF signal, provides a series of load circuits and allows load modulation of the RF field.

On the underside of the EMV – TEST PICC, a C-shaped PICC pickup coil allows signal acquisition through a 50 Ω SMA socket connector (J9). Section 3.1.2 explains the underside of the EMV – TEST PICC.

All signal connections are made using a set of 50 Ω SMA socket connectors at the end farthest away from the coils.

Note: EMVCo currently does not allow the replacement of a qualified EMV Test PCD or EMV Test PICC unit by a spare unit.

3.1.2 Electrical Connectivity

The EMV – TEST PICC features 8 connectors: two inputs, two outputs, and four additional output connectors. Of the four additional output connectors, only one is used for calibration purpose; the others are not currently used.
The features and functions of the input connectors are shown in Table 3.1:

<table>
<thead>
<tr>
<th>Input Connectors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>Allows sending PICC emulated data to the PCD being tested.</td>
</tr>
<tr>
<td>J3</td>
<td>Not used with the EMV – TEST PICC. Do not connect anything to it.</td>
</tr>
</tbody>
</table>

Table 3.1—EMV – TEST PICC Input Connectors

All inputs are internally terminated with 50 Ω loads.

The features and functions of the output connectors are shown in Table 3.2:

<table>
<thead>
<tr>
<th>Output Connectors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Allows measurement of the field strength of a PCD. This field strength is measured into a high impedance load with a passive or active probe.</td>
</tr>
<tr>
<td>J9</td>
<td>Allows sensing the PCD signal through the PICC pickup coil. It shall be connected to 50 Ω input impedance equipment. Specifically, if a test does not require connecting J9 to J8 of the EMV – TEST CMR (providing a 50 Ω load), J9 must be connected to a 50 Ω load. The voltage on J9 will vary with PCD power and EMV – TEST PICC position. A voltage of 1 V peak to peak represents a typical level.</td>
</tr>
</tbody>
</table>

Table 3.2—EMV – TEST PICC Output Connectors

The features and functions of the additional connectors are shown in Table 3.3:

<table>
<thead>
<tr>
<th>Output Connectors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J6</td>
<td>Allows calibration and calibration verification of the EMV – TEST PICC. The method for calibration verification is described later in this document as well as in the \textit{EMV – TEST PICC} manual.</td>
</tr>
<tr>
<td>J3, J5, J5B</td>
<td>Not currently used.</td>
</tr>
</tbody>
</table>

Table 3.3—EMV – TEST PICC Additional Connectors

Note: Do not make any connection to J6 during testing as its ground is not connected to local ground.
3.1.3 Positioning Characteristics

Figure 3.2 shows the underside of the EMV – TEST PICC, Version 2.1:

![C-shaped Pickup Coil](image)

**Figure 3.2—Underside of the EMV – TEST PICC, Version 2.1.**

The C-shaped PICC pickup coil forms the presentation plane. The central point of the presentation plane is the geometric center of the C-shaped PICC pickup coil of the EMV – TEST PICC.

The orientation of the $Z_c$ axis is indicated in Figure 3.1.

The $\phi_c=0$ axis is the direction from the center of the presentation plane towards the edge with the connectors.

3.1.4 On-board Adjustment

*Note* Tuning the VC1 capacitor changes the calibration status of the EMV – TEST PICC. It shall only be done if allowed by EMVCo.

On the EMV – TEST PICC, three parameters are adjustable:

1. Variable capacitor (VC1) is used to adjust the EMV – TEST PICC resonant frequency.
2. Jumper set J7 is used to adjust the EMV – TEST PICC load. The jumper positions determine how many pairs of diodes are placed in series with the stepped load:

<table>
<thead>
<tr>
<th>Jumpers</th>
<th>Provides</th>
</tr>
</thead>
<tbody>
<tr>
<td>Removed</td>
<td>4 diode pairs are in series with the load.</td>
</tr>
<tr>
<td>1 – 2</td>
<td>3 diode pairs are in series with the load.</td>
</tr>
<tr>
<td>1 – 3 (default setting)</td>
<td>2 diode pairs are in series with the load.</td>
</tr>
<tr>
<td>1 – 4</td>
<td>1 diode pair is in series with the load.</td>
</tr>
<tr>
<td>1 – 5</td>
<td>No diode pairs are in series with load.</td>
</tr>
</tbody>
</table>

Table 3.4—Jumper Set J7 Settings

3. Jumper set J8 is used to adjust the EMV – TEST PICC load type:

<table>
<thead>
<tr>
<th>Jumpers</th>
<th>Provides</th>
</tr>
</thead>
<tbody>
<tr>
<td>Removed</td>
<td>No load</td>
</tr>
<tr>
<td>1 – 2</td>
<td>Fixed load 330 Ω</td>
</tr>
<tr>
<td>1 – 3</td>
<td>Alternate fixed load – not used in the current version</td>
</tr>
<tr>
<td>1 – 4 (default setting)</td>
<td>Non-linear load</td>
</tr>
</tbody>
</table>

Table 3.5—Jumper Set J8 Settings

>Note

Unless otherwise specified, jumper set J7 shall be used to select 2 diode pairs in series with the load. Jumper set J8 shall be used to enable the non-linear load.
3.2 EMV TEST PCD

3.2.1 Description

Figure 3.3 shows the EMV - PCD, Version 1.2:

The EMV – TEST PCD comprises a PCB and a stand.

The PCB forms the antenna and has two 50 Ω SMA sockets for connecting to test equipment.

The stand elevates the PCB above the bench, which provides a defined separation for the Landing Plane and incorporates a set of location points for accurate positioning of the EMV – TEST PICC or PICC under test.

**Note**

To ensure the best spatial repartition of the RF field, the EMV Test PCD board shall be mounted under its Perspex® stand with components side downwards, as shown on the above picture.
EMVCo currently does not allow the replacement of a qualified EMV Test PCD or EMV Test PICC unit by a spare unit.

3.2.2 Electrical Connectivity

The EMV – TEST PCD features two connectors:

<table>
<thead>
<tr>
<th>Connectors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Allows reception of the PCD carrier. When the EMV -Test PCD is calibrated, the input impedance at J1 is $50 , \Omega$ at 13.56 MHz when no PICC is in the field of the PCD.</td>
</tr>
<tr>
<td>J2</td>
<td>Allows signal acquisition by sending out a $1 , \Omega$ source impedance output signal. J2 shall be connected to equipment featuring $50 , \Omega$ input impedance.</td>
</tr>
</tbody>
</table>

Table 3.6—EMV – TEST PCD Connectors

3.2.3 Positioning Characteristics

Positioning characteristics are defined with respect to the landing plane:

- The landing plane is the circle on the Perspex® stand above the EMV – TEST PCD antenna.
- The central point of the landing plane is the geometric center of the circle drawn on the Perspex.
- The $Z$ axis of the EMV – TEST PCD is the axis through the central point of the landing plane and pointing from the antenna PCB up through the face of the Perspex cover.
- The $\varphi=0$ axis of the EMV – TEST PCD is the axis through the central point of the landing plane, parallel to the line formed by connectors J1 and J2, and oriented in the direction of J1.

3.2.4 On-board Adjustment

The two variable capacitors (VC1 and VC2) on the EMV – TEST PCD set the input impedance and the resonant frequency. The PCB is always mounted as shown in Figure 3.3. Capacitors VC1 and VC2 are mounted on the component side of the PCB.

Note: Tuning the VC1 and VC2 capacitors changes the calibration status of the EMV – TEST PCD. It shall only be done if allowed by EMVCo.
3.3 EMV TEST Common Mode Rejection Circuit Board

3.3.1 Description

The EMV – TEST CMR is used to condition and switch signals between its inputs and outputs. This allows added flexibility in the Test Bench.

Figure 3.4 shows the EMV – TEST Common Mode Rejection circuit board, Version 2.1:

![EMV TEST CMR Circuit Board, Version 2.1](image)

**Figure 3.4—EMV – TEST CMR Circuit Board, Version 2.1**

The EMV – TEST CMR circuit board is the interface between EMV – TEST PCD output or the EMV – TEST PICC pickup coil output and the test equipment.

**Note**

The EMV – TEST CMR should be switched on five minutes before using it and should be left powered up during a test session.
Laboratories are allowed to use a spare EMV Test CMR device for Type Approval testing, provided that the three conditions below are met:

1. The spare unit has a valid calibration certificate, issued by an authorized entity less than one year before;
2. The spare unit is used for the whole test session, from the initial verifications to the final test;
3. The specific gain of the spare unit is used during all relevant tests, in place of the gain from the replaced unit.

**Note**

EMVCo currently does not allow the replacement of a qualified EMV Test PCD or EMV Test PICC unit by a spare unit.

### 3.3.2 Electrical Connectivity

**Connectors**

The EMV – TEST CMR circuit board features three input connectors and four output connectors.

All signal connectors on the EMV – TEST CMR circuit board are 50 Ω SMA socket connectors.

The features and functions of the input connectors are shown in Table 3.7:

<table>
<thead>
<tr>
<th>Input Connectors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Receives an external clock signal which is neither J2 nor J8. This input presents a 50 Ω load to the source regardless of which input is selected via the relays. For normal operation, this input signal should be up to ± 2 V for normal operation and shall not exceed ± 3 V.</td>
</tr>
<tr>
<td>J2</td>
<td>Receives the signal coming from the EMV – TEST PCD antenna. This input presents a 50 Ω load to the source regardless of which input is selected via the relays. For normal operation, this input signal should be up to ± 2 V for normal operation and shall not exceed ± 3 V.</td>
</tr>
<tr>
<td>J8</td>
<td>Receives the signal coming from the EMV – TEST PICC pickup coil. This input presents a 50 Ω load to the source regardless of which input is select via the relays. For normal operation, this input signal should be up to ± 2 V for normal operation and shall not exceed ± 3 V.</td>
</tr>
</tbody>
</table>

**Table 3.7—EMV – TEST CMR Input Connectors**
All these inputs are internally connected to 50 Ω loads.

The features and functions of the output connectors are shown in Table 3.8:

<table>
<thead>
<tr>
<th>Output Connectors</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3</td>
<td>Recovers the clock signal from a signal coming from either J1, J2 or J8. The recovered clock will be delayed as required by the delay lines. This is explained in section 3.3.3.</td>
</tr>
<tr>
<td>J4</td>
<td>Recovers a copy of an input signal with almost unity gain. In normal use, the output will be up to 1.5 V peak to peak without using the clipper block. Note: the input signal can also be amplified using the clipper block, but this option is not used in the current version of the document.</td>
</tr>
<tr>
<td>J5</td>
<td>Samples and holds an input signal. Note: Do not use this connector for PCD or PICC capability testing.</td>
</tr>
<tr>
<td>J9</td>
<td>Sends a clock signal for the sample and hold feature. Note: Do not use this connector for PCD or PICC capability testing.</td>
</tr>
</tbody>
</table>

Table 3.8—EMV – TEST CMR Output Connectors

All CMR board outputs shall be connected to equipment which features 50 Ω input impedance.

When not used, J4 shall be connected to a 50 Ω load.
Relays

The EMV – TEST CMR circuit board features three relays.

The features and functions of the relays are shown in Table 3.9:

<table>
<thead>
<tr>
<th>Relays</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relay 1</td>
<td>Selects the EMV – TEST CMR input between J2 (signal coming from EMV – TEST PCD output J2) and J8 (signal coming from the EMV – TEST PICC output J9).</td>
</tr>
<tr>
<td>Relay 2</td>
<td>Selects which input signal will be used to derive the clock signal that is sent to the Acquisition Device (either the chosen input or the signal coming from the signal generator producing the carrier frequency).</td>
</tr>
<tr>
<td>Relay 3</td>
<td>Selects if the EMV – TEST CMR input is sent via a buffer amplifier or if the signal has been processed via the clipper amplifier. Note: Do not use the clipper amplifier in the current version of the document.</td>
</tr>
</tbody>
</table>

Table 3.9—EMV – TEST CMR Relay Features

Delay lines

The delay lines consist of four delay chips in series. The four delay lines are organized in two pairs of two chips referred to as DL1+DL2 and DL3+DL4. Note that the output from DL3+DL4 includes any delay introduced by DL1+DL2. Each pair of delay lines provides a programmable delay of between 4.4 ns and 24.4 ns.

3.3.3 Other Common Mode Rejection Circuit Board Connections

In addition, two more connection groups are available:

- Four power terminals (12 V, 5 V, 0 V and -12 V) requiring an external regulated Power Supply.
- An Inter Integrated Circuit (IIC), also known as I2C connector which can receive control data from an external source.
### 3.3.4 Common Mode Rejection Circuit Board Control

The EMV – TEST CMR circuit board shall be controlled through the I2C connector. The controls affect three relays and four delay lines. Table 3.10 shows the EMV – TEST CMR functions and associated controls:

<table>
<thead>
<tr>
<th>Function</th>
<th>Settings</th>
<th>Description</th>
<th>Controlled by</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>J2, J8</td>
<td>Input signals into the EMV – TEST CMR.</td>
<td>Relay</td>
</tr>
<tr>
<td>Output</td>
<td>J4</td>
<td>Output signals from the EMV – TEST CMR.</td>
<td>Uncontrolled (permanently available)</td>
</tr>
<tr>
<td>Clock</td>
<td>J1, J2, J8</td>
<td>J1: A clock signal based on an external clock signal.</td>
<td>Relay</td>
</tr>
<tr>
<td></td>
<td></td>
<td>J2, J8: A clock signal based on a recovered clock signal depending on the input signal.</td>
<td></td>
</tr>
<tr>
<td>Main clock selection</td>
<td>DL1 + DL2</td>
<td>Sets the delay of the main clock.</td>
<td>Delay lines and Multiplexers</td>
</tr>
<tr>
<td></td>
<td>DL3 + DL4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DL1 + DL2 (180 degrees)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DL3 + DL4 (180 degrees)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S/H clock selection</td>
<td>DL1 + DL2</td>
<td>DL1 + DL2 + DL3 + DL4 sets the delay of the sample and hold clock.</td>
<td>Delay lines and Multiplexers</td>
</tr>
<tr>
<td></td>
<td>DL3 + DL4</td>
<td>DL1 + DL2 (180 degrees)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DL3 + DL4 (180 degrees)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

As the sample and hold clock is not used in the tests described in this document, the delay lines shall always be set to DL1 + DL2.

Table 3.10—EMV – TEST CMR Functions and Associated Controls
Requirements for the Test Bench

This chapter describes the requirements for test functions and test equipment used in EMV Contactless PCD Analogue Interface Testing. It also presents Test Bench support equipment.

4.1 Overview

4.1.1 Test Bench Functions for Set-up

4.1.1.1 PICC Emulation

4.1.1.2 Signal Acquisition and Measurement on EMV TEST PICC

4.1.1.3 EMV TEST CMR Control

4.1.1.4 PCD Emulation

4.1.1.5 Signal Acquisition and Measurement on the EMV TEST PCD

4.1.2 Test Bench Functions for Testing

4.2 Test Bench Functions

4.2.1 PICC Emulation

4.2.1.1 Purpose

4.2.1.2 Requirements

4.2.1.3 PICC Emulation Implementation

4.2.2 Signal Acquisition and Measurement on the EMV TEST PICC

4.2.2.1 Purpose

4.2.2.2 Requirements

4.2.2.3 Signal Acquisition and Measurement on the EMV TEST PICC Implementation

4.2.3 EMV TEST CMR Control

4.2.3.1 Purpose

4.2.3.2 Requirements

4.2.3.3 EMV TEST CMR Control Implementation

4.2.4 PCD Emulation

4.2.4.1 Purpose

4.2.4.2 General Requirements

4.2.4.3 PCD Emulation Implementation

4.2.5 Signal Acquisition and Measurement on EMV TEST PCD

4.2.5.1 Purpose

4.2.5.2 Requirements

4.2.5.3 Signal Acquisition and Measurement on EMV TEST PCD Implementation

4.3 Test Bench Environment

4.3.1 Purpose
4.3.2 Requirements ........................................................................................................... 4-17

4.4 Summary of Signals Names and Parameters ................................................................. 4-18
  4.4.1 Signal Names ........................................................................................................... 4-18
  4.4.2 Parameters ................................................................................................................ 4-20
4.1 Overview

The proprietary Test Bench is connected to the EMV Test Equipment provided by EMVCo. Figure 4.1 shows a block diagram of the Test Bench:

![Block Diagram of the Test Bench](image)

**Note**

The term proprietary refers to a Test Bench assembled using equipment chosen by the Testing Laboratory as meeting all requirements described in this chapter.

There are two steps in using the Test Bench:

- Set-up of the EMV Test Equipment.
- Test PCDs from a vendor.
4.1.1 Test Bench Functions for Set-up

Figure 4.2 shows the test functions of the EMV Analogue Test Bench used during the setup of the EMV Test Equipment:

![Diagram showing test functions of the EMV Analogue Test Bench]

**4.1.1.1 PICC Emulation**

Emulation of the PICC consists in a simulation of the answer of an EMV Contactless compliant PICC. Emulation should be representative of a real PICC therefore different load modulation amplitudes are generated to provide representative emulation.

**4.1.1.2 Signal Acquisition and Measurement on EMV TEST PICC**

The Test Bench, using the EMV – TEST PICC, measures PCD parameters such as magnetic field strength, waveform characteristics and carrier frequency.

**4.1.1.3 EMV TEST CMR Control**

For tests using the EMV – TEST CMR, the Test Bench controls the various configuration settings of the EMV – TEST CMR using the EMV – TEST CMR control software.

**4.1.1.4 PCD Emulation**

The Test Bench, used with the EMV – TEST PCD, emulates a real PCD. Various characteristics of the emulated PCD such as magnetic field strength and carrier frequency can be adjusted.
4.1.1.5 Signal Acquisition and Measurement on the EMV TEST PCD

The Test Bench used with the EMV – TEST PCD measures PICC parameters such as load modulation.

Note: Signal Acquisition and Measurement on EMV – TEST PCD is only used during set-up.

4.1.2 Test Bench Functions for Testing

When testing PCDs from a vendor, a PCD under test replaces the EMV – TEST PCD. Figure 4.3 shows a block diagram for PCD testing:

[Diagram of PCD Testing Block Diagram]

Figure 4.3—Block Diagram for PCD Testing
4.2 Test Bench Functions

This section describes the test functions of the Test Bench. Each test function description comprises its purpose (including any necessary parameters and signal names), the requirements to meet the purpose and a description of the functionalities used to meet the requirements.

While the test bench functions are individually described, the Testing Laboratory does not have to implement each function as an individual entity. The Testing Laboratory may integrate functions provided that the overall test bench meets the performance requirements.

4.2.1 PICC Emulation

The PICC emulation function sends an emulated PICC answer to the PCD under test. The EMV – TEST PICC uses this signal to modify the load it presents to the electromagnetic field generated by the PCD. Using with various load modulation amplitudes, PCD receptivity can be evaluated.

4.2.1.1 Purpose

The PICC emulation function delivers an electrical signal to input J2 of the EMV – TEST PICC. This signal is called the PICC Analogue Transmission signal. Adjusting the voltage level of the PICC Analogue Transmission signal changes the load modulation amplitude.

4.2.1.2 Requirements

The PICC emulation function shall feature the following quality characteristics for the PICC Analogue Transmission signal:

- The logic content and the timing of the Analogue Transmission Signal (implementing the PICC emulation function) shall be compliant to the one defined in Appendix C.
- The amplitude shall be adjustable from 0.5 to 5 V.
- The overshots shall not exceed 5% of the amplitude.
- The rise and fall times shall not exceed 30 ns.
- When measured on the connector J2 of the EMV – TEST PCD, load modulation shall be adjustable with a resolution ≤ ± 1 mV.
- The output impedance shall be nominally 50 Ω to match the 50 Ω input impedance on input J2 of the EMV – TEST PICC.
- The PICC answer shall be sent with a delay adjustable by steps of 20 ns or better.
- The emulated PICC responses shall be synchronized with the PCD commands to provide the required timing interval according to Appendix C. The accuracy shall be ± 1/fC or better.
- The PICC emulation function shall deliver a trigger to the Acquisition Device (not shown in Figure 4.4).
4.2.1.3 PICC Emulation Implementation

Figure 4.4 shows the conceptualized block diagram for PICC emulation:

![Block Diagram for PICC Emulation](image)

The PICC emulation function comprises two functional blocks, these are:

- PICC Signal Generation
- PICC Synchronization System

**PICC Signal Generation**

The PICC Signal Generation system sends PICC coding to the PCD under test. It comprises:

- PICC Coding Generator
- Load Modulation Adjustment

**PICC Coding Generator**

The PICC Coding Generator produces a digital signal that carries the information for the bit-level coded answer of the PICC. One logic state encodes an absence of the load while the other logic state encodes the presence of the load. This signal is called the PICC Digital Transmission signal.

The basic performance criteria of the PICC Coding Generator shall be the following:

- Timing resolution: 20 ns or better
- Overall accuracy of \( f_c/16 \) subcarrier < 10 ppm
- Low jitter \( \leq 1 \text{ ns} \)
Load Modulation Adjustment

The Load Modulation Adjustment system varies the signal voltage coming from the output of the PICC Coding Generator to set the load modulation amplitude at the level required by the test. The output signal is called the PICC Analogue Transmission signal.

The basic performance criteria of the Load Modulation Adjustment shall be the following:

- The voltage output shall be adjustable from 0.5 to 5 V.

Note

The PICC Signal Generation function may be implemented by a single device that combines PICC Coding Generation and a Load Modulation Adjustment. The presentation of these two functionalities as separate is only used for the sake of clarity in the requirements.

PICC Synchronization System

The PICC Synchronization System provides a trigger to the PICC Coding Generator at the end of the PCD under test command. This signal is called the PCD Synchronization signal.

The basic performance criteria of the PICC Synchronization System shall be the following:

- The synchronization system shall be capable of detecting all the PCD commands and shall deliver a trigger signal in a format suited to the PICC Coding Generator and synchronized to the end of sequence (EoS) of the PCD frame.
- The trigger signal shall be provided to the PICC Coding Generator in sufficient time for the PICC Coding Generator to emulate PICC responses within the timing requirements of Appendix C.
- At the end of a PCD command, the PICC answer following the trigger pulse shall be sent with a delay adjustable by steps of 20 ns or better.
- The synchronization system shall not affect measurements.
- The synchronization device antenna shall be placed at the farthest convenient position that maintains consistent readings and does not influence the measurement. This position must be identical throughout testing with the standard positioning tool.

Table 4.1 shows a summary of the signal name and its characteristics:

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Measured at</th>
<th>Built From</th>
</tr>
</thead>
</table>
| PICC Analogue Transmission   | Provides a signal that the EMV – TEST PICC uses to modify the load on the PCD electromagnetic field | Input J2 of the EMV – TEST PICC.             | • PCD Synchronization
|                              |                                                                              |                                              | • PICC Digital Transmission             |
4.2.2 Signal Acquisition and Measurement on the EMV TEST PICC

The signal acquisition and measurement on the EMV – TEST PICC uses the signals available on the J9 and J1 connectors of the EMV – TEST PICC.

4.2.2.1 Purpose

This acquisition and measurement system serves the following purposes:

- Measure the field strength generated by the PCD under test.
- Measure the critical parameters of the waveform generated by the PCD under test.

4.2.2.2 Requirements

This acquisition and measurement system shall feature the following characteristics:

- The equipment shall be able to provide a graphic display of the digitally formatted signal for visual analysis. The signal capture shall be over at least 20 ms.
- The equipment shall be able to display all small envelope variations (greater than 5 mV) that allow the evaluation of monotonicity.
- The equipment should self-trigger on Type A and Type B commands. If the equipment is not capable of self-triggering on Type A and Type B commands, the Testing Laboratory shall ensure that the external triggering (with a DSO or other equipment) does not affect the measurements.
- The equipment shall be able to measure the following:
  - The mean amplitude of a signal ranging from 0 to 10 V, averaged over not less than 10 μs, with DC and AC components, within a 30 MHz bandwidth and with an accuracy of ± 2 % or better.
  - The nominal frequency of 13.56 MHz ± 7 kHz with an accuracy of ± 100 Hz or better.
  - A timing resolution on the waveform signal of at least one cycle of the carrier frequency.
  - The modulation index of a Type B PCD signal with an accuracy of ± 0.5 % (absolute precision).
- The equipment shall convert the analogue signal to a digital format as early as possible in the process. Conversion may be peak detection or asynchronous sampling.

Note

If a complete transaction needs to be observed, the acquisition device capture period (memory length) shall be at least 300 ms.

Note

The equipment may decode the digital bit string sent by the PCD, but the Device Test Environment (DTE) provided with the sample to check PCD receptivity can be used.
Note

The use of a low-pass filter fitted between the PICC and the EMV – TEST CMR is highly recommended. The filter shall feature less than 1 dB attenuation at 20 MHz and more than 40 dB attenuation at 40 MHz.

4.2.2.3 Signal Acquisition and Measurement on the EMV TEST PICC Implementation

The signal acquisition and measurement on EMV – TEST PICC comprises two functional blocks:

- Power Parameter Acquisition and Measurement device
- AC Parameters Acquisition and Measurement device

Figure 4.5 shows the functional blocks for signal acquisition/measurement on the EMV – TEST PICC:

![Block Diagram for Signal Acquisition/Measurement on the EMV – TEST PICC](image)

Note

The EMV – TEST CMR control is explained in section 4.2.3, and the EMV – TEST CMR is described in Chapter 3.

Power Parameter Acquisition and Measurement

The power parameter acquisition and measurement device determines the DC voltage at the output of the J1 connector of the EMV – TEST PICC. This signal is called the PICC Analogue Power Sensing signal.

The basic performance criteria of the power parameter acquisition and measurement device shall be the following:
• The input impedance of the acquisition system shall present a high impedance (≥1 MΩ and less than 15 pF for a frequency between 0 and 30 MHz) to the EMV – TEST PICC output J1.

• At least 10 mV resolution in the range 0 - 10 V

• Minimum sampling rate: 100 MSa/s

• Automated calculation of the mean value of all samples

• Sampling shall be carried out during the absence of PCD modulation.

**AC Parameters Acquisition and Measurement**

The AC parameters acquisition and measurement device senses the PCD parameters of the waveform at the J4 connector of the EMV – TEST CMR (which provides a flexible interface) from the source waveform appearing at the J9 connector of the EMV – TEST PICC. The signal at J9 is called the Unprocessed PICC Analogue Sensing signal.

• The input impedance of the acquisition system shall present a 50 Ω load to EMV – TEST CMR output J4.

• The equipment shall be able to measure a nominal frequency of 13.56 MHz ± 7 kHz with an accuracy of ± 100 Hz or better.

If this device uses the peak sampling method, it shall have the following characteristics:

• The test equipment shall feature at least 14-bit resolution.

If this measurement is carried out using the asynchronous sampling method, it shall have the following characteristics:

• The test equipment shall feature at least 14-bit resolution.

• Minimum sampling rate: 100 MSa/s. However, note that this sampling rate is only acceptable if appropriate digital post-processing is used.

Table 4.2 shows a summary of the signal names and their characteristics:

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Measured at</th>
<th>Built from</th>
</tr>
</thead>
<tbody>
<tr>
<td>PICC Analogue Power Sensing</td>
<td>PCD carrier power evaluation</td>
<td>Output J1 of the EMV – TEST PICC</td>
<td>None, this is a basic signal from the EMV – TEST PICC</td>
</tr>
<tr>
<td>Unprocessed PICC Analogue Sensing</td>
<td>PCD waveform evaluation</td>
<td>While the source waveform appears at the J9 connector of the EMV – TEST PICC, it is measured at output J4 of the EMV – TEST CMR</td>
<td>None, this is a basic signal from the EMV – TEST PICC provided through the EMV – TEST CMR</td>
</tr>
</tbody>
</table>

**Table 4.2—Summary of the Signal Names and their Characteristics**
Several parameters are measured when evaluating the signals in the previous table. Table 4.3 shows a summary of the parameters and the associated signal names:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Description</th>
<th>Measured at</th>
<th>Associated Signal Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCD field strength</td>
<td>$V_{OV}$</td>
<td>The field strength of a PCD is measured at the EMV – TEST PICC</td>
<td>Output J1 of the EMV – TEST PICC</td>
<td>PICC Analogue Power Sensing</td>
</tr>
<tr>
<td>PCD field strength during a reset</td>
<td>$V_{OV,RESET}$</td>
<td>The field strength of a PCD during a reset is measured at the EMV – TEST PICC</td>
<td>Output J9 of the EMV – TEST PICC</td>
<td>Unprocessed PICC Analogue Sensing</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>$f_c$</td>
<td>PCD frequency measured at the Unprocessed PICC Analogue Sensing signal</td>
<td>Output J9 of the EMV – TEST PICC</td>
<td>Unprocessed PICC Analogue Sensing</td>
</tr>
<tr>
<td>PCD signal timing</td>
<td>$t_x$</td>
<td>Time between two defined levels of the Unprocessed PICC Analogue Sensing signal</td>
<td>Output J9 of the EMV – TEST PICC</td>
<td>Unprocessed PICC Analogue Sensing</td>
</tr>
<tr>
<td>Type B modulation index</td>
<td>$m_i$</td>
<td>PCD Type B modulation index calculated between two defined levels of the Unprocessed PICC Analogue Sensing signal</td>
<td>Output J9 of the EMV – TEST PICC</td>
<td>Unprocessed PICC Analogue Sensing</td>
</tr>
</tbody>
</table>

Table 4.3—Summary of the Parameters and the Associated Signal Names

4.2.3 EMV TEST CMR Control

The EMV – TEST CMR contains relays and delay lines that switch its inputs and set internal signal conditioning features. An external device sends the control signals for switching and setting through the I2C connector.

4.2.3.1 Purpose

For the purposes of the tests in this document, the EMV – TEST CMR control aims to define the CMR input and the clock recovery. The EMV – TEST CMR control writes data to the I2C bus but for the tests described in this manual, does not need to read data.

4.2.3.2 Requirements

The EMV – TEST CMR control shall feature the following characteristics:

- Control of the relays selecting inputs J2 or J8 (mutually exclusive).
- Control of the relay selecting the clipper amplifier or the buffer amplifier (mutually exclusive).
- Control of main clock selection and S/H clock selection.
• No data transmission from the PC to the EMV – TEST CMR shall occur during measurements.
• Data sent to the I2C connector shall meet the I2C specification.
• If synchronous sampling is used, the clock sampling shall be adjustable with a resolution of 10 ps with a range from zero to one carrier cycle.

4.2.3.3 EMV TEST CMR Control Implementation

Figure 4.6 shows the functional blocks for the EMV – TEST CMR control:

![Figure 4.6—Functional Blocks for the EMV – TEST CMR Control](image)

EMV – TEST CMR control software accompanies the EMV – TEST CMR circuit board. This software is adapted to the peak sampling method.

If the acquisition device connected to the EMV – TEST CMR uses the peak sampling method, the CMR control shall be able to adjust the delay lines and clock sources of the EMV – TEST CMR.

If the Acquisition Device connected to the EMV – TEST CMR uses the asynchronous sampling method, it shall have control software that meets the requirements described in section 4.2.3.2.

For more information on how to control the EMV – TEST CMR, see the EMV – TEST CMR manual.
4.2.4 PCD Emulation

PCD emulation shall be used in the set-up phase of testing operations. Once the EMV Test Equipment is properly set up, the PCD from a vendor shall be used in testing.

4.2.4.1 Purpose

This test function produces an amplified modulated carrier for the EMV – TEST PCD at connector J1. This signal is called the PCD Power Output signal.

It is a source signal used in EMV – TEST PICC set-up.

Note

Modulation is not necessary for tests performed in this document.

4.2.4.2 General Requirements

The PCD emulation function shall feature the following quality characteristics:

- The generated frequency shall be 13.56 MHz with an accuracy of ± 100 Hz or better.
- When connected to the EMV – TEST PCD Antenna, the voltage at connector J1 shall be adjustable up to a maximum of 20 V peak to peak. This maximum shall not be exceeded. In the free air condition, the voltage shall be stable within ± 1 % over the period when it is being used for set-up.
- When measured on connector J1 of the EMV – TEST PICC, the PCD emulation voltage shall be adjustable to achieve the desired signal level with an accuracy of ± 2 % including measurement uncertainty.
- The output impedance shall be nominally 50 Ω to match the input impedance at input J1 of the EMV – TEST PCD Antenna (50 Ω at 13.56 MHz).

4.2.4.3 PCD Emulation Implementation

The PCD emulation is composed of two functional blocks:

- Signal Generation
- RF Amplification
Figure 4.7 shows the functional blocks for a PCD emulator:

**Signal Generation**

The Waveform Generator sends a low-power analogue electrical signal with a waveform corresponding to the waveform of the electromagnetic field that needs to be generated. This signal is called the PCD Analogue Transmission signal.

The basic performance criteria of the Waveform Generator shall be the following:

- Frequency range 13.5 to 13.6 MHz
- Frequency resolution and accuracy of 100 Hz or better
- Spurious distortion less than -60 dBc in the vicinity of the carrier or its sidebands; the sum of all distortions shall be less than -50 dB so as not to swamp card modulation measurements.

**RF Amplification**

In this second functional block, one component amplifies the signal received from the signal generation block.

The RF Power Amplifier converts the low-power PCD Analogue Transmission signal into a higher power signal that is fed to the J1 input of the EMV – TEST PCD. This signal is called the PCD Power Output signal.

The basic performance criteria of the RF Amplifier after any additional attenuation shall be the following:

- Power output at 1dB compression point : 1W minimum
- Low harmonic distortion (better than -50 dBc)
- Suitable bandwidth (13.56 MHz ± 2 MHz)
- For EMV Contactless testing, the power output of the RF Amplifier shall be from 0.5 W to 1 W into an impedance of 50 Ω.
- VSWR < 1.2:1
The RF power amplifier must be able to operate with a high VSWR without damage, as VSWR will increase when the EMV – TEST PICC under test is placed close to the EMV – TEST PCD.

Table 4.4 shows a summary of the signal name and its characteristics:

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Measured at</th>
<th>Built From</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCD Power Output</td>
<td>Amplified carrier signal</td>
<td>Input J1 of the EMV – TEST PCD</td>
<td>PCD Analogue</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Transmission signal</td>
</tr>
</tbody>
</table>

Table 4.4—Summary of the Signal Name and its Characteristics

4.2.5 Signal Acquisition and Measurement on EMV TEST PCD

During load modulation measurement of the EMV – TEST PICC set-up, signal acquisition and measurement on the EMV – TEST PCD plays an important role and its parameters shall be evaluated.

4.2.5.1 Purpose

This function acquires and measures PICC load modulation to be used in PCD receptivity testing.

4.2.5.2 Requirements

The signal acquisition shall feature the following general characteristics:

- The equipment shall be able to acquire a signal with an amplitude up to 2 V peak to peak.
- The equipment shall provide a graphic display of the digitally formatted signal for visual analysis. The signal shall be measured for at least 1 ms and shall be displayed with a load modulation amplitude accuracy of 10 % with a minimum of 1 mV or better.
- The input impedance of the acquisition equipment shall present a 50 Ω load to the EMV – TEST CMR output.
- The equipment shall convert the analogue signal to a digital format as early as possible in the process (conversion may be peak detection or asynchronous sampling).
- The equipment shall be able to make automated measurements of the load modulation and shall measure down to 3 mV of load modulation coming from the EMV – TEST PICC.

Over at least seven successive subcarrier cycles of the same phase state, the automated measurement shall calculate the difference between the average value of all the positive peaks and the average value of all the negative peaks that correspond to the positive and negative peaks of the subcarrier cycles.
4.2.5.3 Signal Acquisition and Measurement on EMV TEST PCD Implementation

Figure 4.8 shows the block diagram for signal acquisition and measurement on the EMV – TEST PCD:

Figure 4.8—Block Diagram for Signal Acquisition and Measurement on the EMV – TEST PCD

EMV TEST PCD

The EMV – TEST PCD sends a signal to the EMV – TEST CMR. This signal is called the Unprocessed PCD Analogue Sensing signal.

Acquisition Device

The Acquisition Device achieves the test function requirements by signal acquisition and measurement on output J4 of the EMV – TEST CMR (Relay 1 of the EMV – TEST CMR is set to enable signal flow from J2 to J4). This signal is called the Processed PCD Analogue Sensing signal.

If this device uses the peak sampling method, it shall have the following characteristics:

- The equipment shall feature at least 14-bit resolution.

If this measurement is carried out using the asynchronous sampling method, it shall have the following characteristics:

- The equipment shall feature at least 14-bit resolution.
- The minimum sampling rate shall be 100 MSa/s.

Note

The minimum sampling rate of 100 MSa/s is only acceptable if suitable digital post processing is performed.
Table 4.5 shows a summary of the signal name and its characteristics.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Measured at</th>
<th>Built From</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processed PCD Analogue</td>
<td>Signal used for PICC load modulation measurement</td>
<td>Output J4 of the EMV – TEST CMR</td>
<td>Unprocessed PCD Analogue Sensing</td>
</tr>
</tbody>
</table>

Table 4.6—Summary of the Signal Name and its Characteristics

Table 4.6 shows a summary of the parameter and its characteristics:

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Measured at</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load Modulation</td>
<td>$V_{pp}$</td>
<td>Difference (over at least seven successive subcarrier cycles of the same phase state) between the average of the high peak values and the average of the low peak values of the subcarrier visible in the Processed PCD Analogue Sensing signal</td>
<td>Output J4 of the EMV – TEST CMR</td>
</tr>
</tbody>
</table>

Table 4.6—Summary of the Parameter and its Characteristics
4.3 Test Bench Environment

The Test Bench requires additional hardware to be functionally complete, operate efficiently and facilitate operator duties.

4.3.1 Purpose

The Test Bench shall be supplied with appropriate electrical power, environmental monitoring tools and data storing/reporting devices for simple and efficient operation.

4.3.2 Requirements

The Test Bench shall feature the following characteristics:

**Test Bench Powering**

The PCD under test shall use the Power Supply required by the vendor of the PCDs to be tested. In the case where the Power Supply required by the vendor is specified as one provided by the Testing Laboratory (a stabilized Power Supply), monitoring of voltages shall be performed during the test sessions.

**Environmental Monitoring**

- AC voltage monitoring in the following range 0 to 250 V AC, with an absolute total error of less than ± 500 mV.
- DC voltage monitoring in the following range 0 to 50 V DC, with an absolute total error of less than ± 100 mV.
- Temperature monitoring in the following range 20°C to 26°C, with an absolute total error of less than ± 1.0°C.
- Humidity monitoring in the following range 40% to 60%, with an absolute total error of less than ± 3 % RH.

**Data Storing**

- Data Storage
4.4 Summary of Signals Names and Parameters

This section presents the signal names and parameters, along with their definitions, which are used in analogue testing operations.

4.4.1 Signal Names

Each test function corresponds to a signal of interest that is measured or used in testing. A signal of interest is created with Test Bench equipment that produce component signals directly related to the nature of the signal of interest.

Table 4.7 shows the signals and their components in the PCD EMV Contactless Test Bench:

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Measured at</th>
<th>Built from</th>
</tr>
</thead>
<tbody>
<tr>
<td>PICC Analogue Transmission</td>
<td>Signal used by the EMV – TEST PICC to modify the load on the PCD electromagnetic field</td>
<td>Input J2 of the EMV – TEST PICC</td>
<td>• PCD Synchronization</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• PICC Digital Transmission</td>
</tr>
<tr>
<td>PICC Analogue Power Sensing</td>
<td>PCD carrier power evaluation</td>
<td>Output J1 of the EMV – TEST PICC</td>
<td>None, this is a basic signal from the EMV – TEST PICC</td>
</tr>
<tr>
<td>Unprocessed PICC Analogue Sensing</td>
<td>PCD waveform evaluation</td>
<td>Output J9 (pickup coil) of the EMV – TEST PICC</td>
<td>None, this is a basic signal from the EMV – TEST PICC</td>
</tr>
<tr>
<td>PCD Power Output</td>
<td>Amplified carrier signal</td>
<td>Input J1 of the EMV – TEST PCD</td>
<td>PCD Analogue Transmission</td>
</tr>
<tr>
<td>Processed PCD Analogue Power Sensing</td>
<td>Signal used for PICC output Load Modulation Measurement</td>
<td>Output J4 of the EMV – TEST CMR</td>
<td>Unprocessed PCD Analogue Sensing</td>
</tr>
</tbody>
</table>

Table 4.7—Summary of the Signals and their Components in the PCD EMV Contactless Test Bench
Table 4.8 shows the component signals from which test function signals of the PCD EMV Contactless Test Bench are made:

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Description</th>
<th>Available at</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCD Synchronization</td>
<td>Trigger signal for PICC coding generation</td>
<td>Output of the synchronization circuit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input trigger of the PICC Coding Generator</td>
</tr>
<tr>
<td>PICC Digital Transmission</td>
<td>Digital code stream signal at the output of the PICC Coding Generator used to implement the PICC emulation function.</td>
<td>Output of the PICC Coding Generator</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input of Load Modulation Adjustment</td>
</tr>
<tr>
<td>PCD Analogue Transmission</td>
<td>Un-amplified carrier</td>
<td>Output of the Waveform Generator</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input of the RF Amplifier</td>
</tr>
<tr>
<td>Unprocessed PCD Analogue Sensing</td>
<td>PICC load modulation before passing through the EMV – TEST CMR</td>
<td>Output J2 of the EMV – TEST PCD</td>
</tr>
</tbody>
</table>

Table 4.8—Summary of Component Signals in the PCD EMV Contactless Test Bench

While the component signals are not measured in the tests found in this document, their familiarity allows accurate description of a Test Bench implementation.

Note

### 4.4.2 Parameters

Table 4.9 shows a summary of the parameters applicable to the PCD EMV Contactless Test Bench:

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCD field strength</td>
<td>$V_{OV}$</td>
<td>The field strength of a PCD measured at the J1 connector of the EMV – TEST PICC. This is an average voltage over 10 $\mu$s to 200 $\mu$s of the PICC Analogue Power Sensing signal</td>
</tr>
<tr>
<td>PCD field strength during a reset</td>
<td>$V_{OV,RE SET}$</td>
<td>The field strength of a PCD during a reset is measured at the J9 connector of the EMV – TEST PICC</td>
</tr>
<tr>
<td>Load modulation</td>
<td>$V_{PP}$</td>
<td>Difference (over at least seven successive subcarrier cycles of the same phase state) between the average of the high peak values and the average of the low peak values of the subcarrier visible in the Processed PCD Analogue Sensing signal</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>$f_c$</td>
<td>PCD frequency measured at the Unprocessed PICC Analogue Sensing signal</td>
</tr>
<tr>
<td>PCD signal timing</td>
<td>$t_x$</td>
<td>Time between two defined levels of the Unprocessed PICC Analogue Sensing signal</td>
</tr>
<tr>
<td>Type B modulation index</td>
<td>$m_i$</td>
<td>PCD Type B modulation index calculated between two defined levels of the Unprocessed PICC Analogue Sensing signal</td>
</tr>
</tbody>
</table>

Table 4.9—Parameters Applicable to the PCD EMV Contactless Test Bench
5

Executing an EMV Analogue Interface Test Session

Several steps are necessary to ensure accurate and repeatable EMV analogue interface sample testing. Test samples shall be representative and properly prepared for testing. The results of the various tests shall then be properly reported including deviations from the standard procedures.

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  5.2.2 Recommendations for a PCD without a perfectly flat Landing Plane .......... 5-5

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5.8 Tasks after Completing a Test Campaign .................................... 5-8
5.1 Preparation for Testing

Before starting any testing campaign or receiving test samples, several important requirements shall be verified:

- The Testing Laboratory shall implement a Test Bench with all test functions described in Chapter 4.
- The personnel operating the Test Bench shall be appropriately trained and qualified.
- The Testing Laboratory shall write standard operating procedures providing detailed methods on the EMV Analogue PCD tests and how results are recorded.
- The testing laboratory shall calculate and maintain records of measurement uncertainty estimates prepared using internationally accepted methodology for all Test Cases.

5.2 Verifying Appropriateness

This section contains verifications and requirements to ensure that a PCD test sample is appropriate for testing. It also contains recommendations that shall be followed for dealing with a PCD without a perfectly flat landing plane.

5.2.1 General Requirements

The first step in testing the EMV analogue interface shall be to verify that the sample submission is complete and appropriate.

When samples arrive from the vendor, the Testing Laboratory shall compare the items and their markings with the delivery documentation to ensure that they match. Any discrepancy shall be resolved with the vendor before beginning any testing.

If the submission is not complete, the Testing Laboratory shall also contact the vendor and request completion. Carefully note the reasons for discrepancies, delays and incompleteness in sample delivery to the Testing Laboratory.

Before starting PCD testing, the qualified operator shall carry out the following actions:

1. Select one PCD sample according to the sampling rules of the Testing Laboratory.
2. Verify that the sample is properly identified and labeled (manufacturer, type, serial number, revision).
3. Verify that the PCD features a correct EMV Contactless symbol as defined in the specifications. All the following items shall be verified:

   a. The symbol drawing shows the contactless indicator (four circular arc lines from smallest to largest in size, left to right) at the center of the symbol, the hand holding a generic contactless form factor device and an oval key line that wraps the indicator and the hand.

   b. The drawing is in white reversed line drawing against any medium to dark background, or in black line drawing against a white or light-colored background.

   c. The background is a solid color. It does not feature any graphic pattern.

   d. No additional nor modified item is present.

   e. The minimum size of the symbol is 13 mm height by 22 mm width.
f. The size of the symbol features a height/width ratio of 0.59 ± 0.05.

![Correct symbol example]

![Incorrect symbol example]

h. The symbol is neither rotated nor flipped. The hand is present on the right side of the symbol.

![Correct symbol example]

![Incorrect symbol example]

i. There is no text message with the symbol.

The appropriate section of the test report must be filled with the result of this verification.

4. Verify that the positioning characteristics have been defined properly.

5. Verify that the PCD sample has been subjected to the pre-validation test. Refer to the EMVCo Contactless Type Approval: PCD Pre-validation Prior to Level 1 testing manual for details. Two cases are possible depending on the pre-validation test results:

   - If the results are pass, the laboratory continues the analogue tests of the Contactless Terminal Type Approval Level 1 testing process as described in
Chapter 7 of the EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements manual.

- If some results are fail, the laboratory informs the vendor and waits for the decision of the vendor to either continue the Contactless Terminal Type Approval Level 1 testing or stop the process unless the vendor already requested to continue testing regardless of the results.

In the situation where the vendor decides to stop, the test report shall be made available for the Vendor.

6. Verify the presence of a vendor-provided Device Test Environment (DTE) meeting the requirements described in the EMVCo Device Testing Environment document. For further information on this DTE, see Appendix A of the EMVCo Type Approval Contactless Terminal Level 1/ Device Test Environment document.

7. Verify the presence of vendor-provided Device Testing Environment (DTE) documentation:
   - That is identified in the ICS (make sure that you have received everything that you are supposed to receive)
   - That is complete thereby allowing the performance of all necessary tests.

8. Verify that the vendor-provided DTE is understood by the operator.

9. Verify the presence of supplementary documentation with respect to:
   - Documentation of the electrical interface between the sample and the terminal, when these two units are separate hardware items.
   - Documentation of the setup information describing the normal operating conditions of the PCD under test and the conditions for powering and activating the PCD sample.
   - Documentation of any operator-defined settings influencing analogue behavior.
   - A troubleshooting manual, describing common abnormalities and their remedies.

10. Take a photograph of the side of the sample with the positioning characteristics.
For testing purposes, the $\phi=0$ axis is oriented as shown in Figure 5.1:

![PCD Surface with Logo](image)

Figure 5.1— $\phi=0$ Axis Orientation

### 5.2.2 Recommendations for a PCD without a perfectly flat Landing Plane

PCDs with ridges or uneven landing planes shall be handled and tested using special precautions to ensure consistent test results. The recommendations are:

- In all cases, the plane of the EMV – TEST PICC shall remain perpendicular to the z axis at all times.

- If the EMV – TEST PICC can be placed against the landing plane at test positions within the area defined by a ridged, concave or concave-like PCD test area, the actual level $z=0$ cm (specifically, the surface at the center of the landing plane) is used.

- If the EMV – TEST PICC is larger than this area and therefore sits on a ridge or one of its edges touches a concave PCD surface, the space between the elevated EMV – TEST PICC plane and the actual level $z=0$ cm surface is treated as follows:
  - All points between the actual level $z=0$ cm and the point where the EMV – TEST PICC sits on the ridge will be reported as “Not tested because of terminal shape”. In these cases, the Test Cases are performed using all the usually required higher positions in the Test Position tables and additionally at the closest achievable level to $z=0$ cm.

**Note**  
If you cannot reach below 5 mm, contact EMVCo to obtain help in determining new test positions to be performed.
5.3 Identifying the Sample

The configuration of the sample shall be identified unambiguously. Any modification to the sample (mechanical, electrical, functional) during the test session shall require complete re-testing of the modified sample, regardless of the nature of the modified part.

5.4 Powering the Sample

Where the sample needs a power source to operate, it shall be tested according to the conditions provided by the vendor. Where the sample can be powered using either external or internal power sources, it shall be tested using the internal power source as specified by the vendor.

The power source used and the supply voltage provided during the test session shall be recorded in the test report.

5.4.1 PCD Tests with External Power Source provided by the Vendor

During tests, the external power source provided with the equipment shall be used. The Testing Laboratory shall be capable of producing high AC voltage as required by the vendor.

During tests, the test power source voltages shall remain within the vendor tolerance.

5.4.2 PCD Tests with External Power Source provided by the Testing Laboratory

During tests, the external power source provided with the equipment shall be replaced by an external test power source provided by the Testing Laboratory and capable of producing normal test operating voltages as specified by the vendor. The internal impedance of the external test power source shall be low enough for its effect on the test results to be negligible. For the purpose of analogue tests, the voltage of the external test power source shall be measured at the input connections of the PCD. The external test power source shall be suitably decoupled so as to be located as far away from the PCD as possible. All external power leads shall be arranged so as not to affect measurements.
During tests the test power source voltages shall remain within the vendor tolerance.

5.4.3 PCD Test with Internal Power Source

For radiated (RF or electromagnetic) measurements on portable equipment, fully charged internal batteries shall be used. The batteries used shall be as supplied or recommended by the PCD vendor. If internal batteries are used, the test power source voltages shall remain within the vendor tolerance.

The power source voltage at the beginning and at the end of the tests shall be recorded in the test report.

5.4.4 Other Power Sources

For operation from other power sources or types of battery, the normal test voltage shall be that declared by the PCD vendor and agreed by the accredited Testing Laboratory. Such values should be recorded in the test report when possible.

5.5 Preparing the EMV Test Equipment

Before starting the test on a sample, the operator shall perform a preparatory verification of the EMV Test Equipment for the test according to the procedures described in this manual.

The only critical verification that shall be performed periodically is the EMV – TEST PCD and EMV – TEST PICC cross verification. See Chapter 6 for more information.

The Testing Laboratory can also use the required monitoring equipment to confirm that the Test Bench is properly powered and stable. See the section Test Bench Support Functions in Chapter 4.

5.6 Sample Testing

5.6.1 Sequence of Execution

The execution of an EMV analogue test involves performing all Test Cases under different test conditions, as specified in this document.

The PCD under test shall be challenged using the Test Bench equipment and according to external conditions. The challenge shall be conducted in a non-destructive fashion, which primarily means that the Test Bench shall not exceed the sample PCD limits.

After verifying appropriateness, a specific order of Test Cases or conditions is not required during EMV analogue testing with the exception of measuring the carrier frequency, as long as all Test Cases are performed for all specified test conditions on the sample. Any deviation shall be properly recorded in the test report.
5.6.2 Test Results

The test results shall be recorded as an ordered collection of pass/fail values, related to the PCDs under test and the test conditions. This is called detailed report data.

The Testing Laboratory shall also provide screenshots and traces resulting from test failures or intermittent results.

5.6.3 Failed Procedures

If one or more of the following situations appears:

- A specified test condition cannot be attained during test execution.
- A test procedure cannot be executed exactly as indicated.
- A test procedure cannot be completed.

Two cases are possible depending on test bench automation:

- If the test bench is automated, the test bench shall report a failed procedure. Operator action is necessary to correct the situation.
- If the test bench is not automated, then the operator shall report a failed procedure situation and shall, for example, repeat the Test Case.

5.7 Generating a Report

The results of all individual Test Cases that were carried out shall be gathered into a single detailed report.

If it was not possible for any reason to carry out all the Test Cases then this shall be clearly documented.

A summary report based on detailed report data shall then be prepared and shall fulfill all the requirements of the EMV PCD report template.

5.8 Tasks after Completing a Test Campaign

The Testing Laboratory shall store all forms and reports to ensure security and confidentiality in accordance to client requirements.

Onsite report and documentation storage shall comply with ISO/IEC 17025:2005 standards.

Test samples shall be safely stored on premises to facilitate future testing or unexpected requirements.
Preparation of the EMV Test Equipment

This chapter introduces the procedures necessary to establish that all the EMV Test Equipment is functioning correctly and is suitable for testing operations.

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   6.5.1 Cross Verifying the EMV TEST PCD and the EMV TEST PICC 6-14
6.1 General Requirements

The operator shall use the procedures described in this chapter to determine and document the correct functionality of the EMV Test Equipment used for all tests.

These procedures shall be carried out before starting tests on PICCs or PCDs. The data obtained from these procedures shall be included in the test report for the product.

In the event of EMV – TEST PICC or EMV – TEST PCD preparation failure, the test equipment shall be re-calibrated.

**Note**

Do not perform any EMV Analogue Interface test until the test equipment has been calibrated by a Tool Vendor or Laboratory authorized by EMVCo to specifically perform calibration of these devices.

**Note**

The following preparation procedures allow verification of the test equipment calibration with a Vector Network Analyzer (VNA). Testing Laboratories may use other procedures described in the section Verification Procedure of the documents EMV – TEST PCD manual, EMV – TEST CMR manual and EMV – TEST PICC manual.
6.2 Preparing the EMV TEST PICC

The procedure for EMV – TEST PICC verification shall take place in an environment where the temperature is 23°C ± 3°C and the relative humidity is 50%RH ± 10%RH.

**Note**
The verification of the EMV – TEST PICC shall be performed using a suitable Calibration Kit.

**Note**
For all connections, the standard cable is a high quality coaxial cable, such as RG-316, terminated by SMA connectors. The cable ends are then fitted with appropriate adaptors for the connections to be made.

6.2.1 Verifying the EMV TEST PICC

Follow this procedure for EMV – TEST PICC verification:

1. Refer to the diagram in Figure 6.1:

   ![Diagram for EMV – TEST PICC](image)

   **Figure 6.1—Diagram for EMV – TEST PICC**

2. Connect a cable to Port 1 of the VNA but do not yet connect the other end of this cable to the EMV – TEST PICC at J6.

3. Set the frequency range of the VNA from 10 MHz to 20 MHz with at least 1000 points in the sweep and the power sweep generator at an output corresponding to 0 dBm/50 Ω.

   **Note**
   If it is not possible for the sweep to comprise at least 1000 points, the sweep must be reduced until the VNA step size is at most 10 kHz.

4. Perform an Open/Short/Load (OSL) calibration of the VNA and its built-in bridge at the unconnected end of the cable. This establishes the reference plane for Port 1.

5. Connect the unconnected end of the cable to the EMV – TEST PICC at J6.
6. Set the VNA to the S\text{11} measurement mode and the impedance format. The screen shown in Figure 6.2 appears on the VNA display:

![Figure 6.2—EMV – TEST PICC Resonant Frequency](image)

At the resonant frequency of the EMV – TEST PICC antenna, note the presence of a peak of the impedance and zero degrees phase shift.

7. Measure the resonant frequency.

**Acceptance Criteria**

Verification is successful if the resonant frequency is 16.100 MHz ± 100 kHz.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

**Failure Action**

A fail message requires the following actions:

- Request calibration of the EMV – TEST PICC.
- Report failure to EMVCo and request advice.
- Wait until EMVCo gives feedback before starting any such test.
6.3 Preparing the EMV TEST PCD Antenna

The procedure for EMV – TEST PCD verification shall take place in an environment where the temperature is 23°C ± 3°C and the relative humidity is 50%RH ± 10%RH.

Note

The verification of the EMV – TEST PCD antenna shall be performed using a suitable Calibration Kit.

6.3.1 Verifying the EMV TEST PCD Antenna

Follow this procedure for verification of a previously calibrated EMV – TEST PCD using a VNA:

1. Refer to the diagram in Figure 6.3 :

![Diagram](image)

Figure 6.3—Connectivity for EMV – TEST PCD

2. Connect a 50 Ω load to the EMV – TEST PCD at J2.
3. Connect a cable to Port 1 of the VNA but do not yet connect the other end of this cable to the EMV – TEST PCD at J1.
4. Set the frequency range of the VNA from 13 MHz to 14 MHz with at least 1000 points in the sweep and the power level set to 0 dBm/50 Ω.
5. Perform an Open/Short/Load (OSL) calibration of the VNA and its built-in bridge at the unconnected end of the cable coming from Port 1. This establishes the reference plane for Port 1.
6. Connect the unconnected end of the cable coming from Port 1 of the VNA to the EMV – TEST PCD at J1.
7. Set the VNA to S11 measurement mode at Port 1.
8. Set the VNA in Smith Chart format (R+jX). Figure 6.4 shows measurements executed on the VNA at 13.56 MHz:

![Smith Chart Graph](image)

**Figure 6.4—EMV – TEST PCD Verification**

**Note**

The impedance magnitude may be computed using the formula

\[ z = \sqrt{R^2 + X^2} \]

**Note**

The impedance phase may be computed using the formula

\[ \varphi_z = \text{degrees} \left( \arctan \left( \frac{X}{R} \right) \right) \]

**Acceptance Criteria**

Verification is successful if the resonant frequency is 13.560 MHz ± 7 kHz (the frequency with maximum return loss) and the impedance at 13.560 MHz has a magnitude of 50 Ω ± 5 Ω with a phase of 0° ± 10°.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
Failure Action

A fail message requires the following actions:

- Request calibration of the EMV – TEST PCD.
- Report failure to EMVCo and request advice.
- Wait until EMVCo gives feedback before starting any such test.
6.4 Preparing the EMV TEST CMR

The procedure for EMV – TEST CMR verification shall take place in an environment where the temperature is 23°C ± 3°C and the relative humidity is 50%RH ± 10%RH.

6.4.1 Verifying the EMV TEST CMR

The EMV – TEST CMR does not require any calibration, but instead requires that the gain obtained from the input to the output is measured and recorded during the verification procedure.

The EMV – TEST CMR shall successfully pass three tests to verify that it has suitable signal transmission, delay line and gain. Perform all three verification procedures in this section for EMV – TEST CMR preparation.

6.4.1.1 J2 to J4 Signal Transmission Verification

Follow this procedure for the signal transmission verification:

1. Refer to the diagram in Figure 6.5:

   ![Diagram for the EMV – TEST CMR Signal Transmission Verification](image)

   **Figure 6.5—Diagram for the EMV – TEST CMR Signal Transmission Verification**

   Connect appropriate devices so as to implement the functionalities shown.

2. Connect the power supplies to the appropriate voltage connection points, switch on the power supplies and check that the current drawn is within the limits shown in Table 6.1:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>+12 V</td>
<td>150 mA</td>
</tr>
<tr>
<td>-12 V</td>
<td>350 mA</td>
</tr>
<tr>
<td>+5 V</td>
<td>1300 mA</td>
</tr>
</tbody>
</table>

   **Table 6.1—Power Supply Parameters**
3. Set up the EMV – TEST CMR relays as shown in Table 6.2:

<table>
<thead>
<tr>
<th>Relay</th>
<th>Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>Clock</td>
</tr>
<tr>
<td>Internal recovery</td>
<td>Amplifier</td>
</tr>
</tbody>
</table>

Table 6.2—EMV – TEST CMR settings

4. Set the Waveform Generator to 13.56 MHz with an amplitude of 300 mV peak to peak into 50 Ω.

5. Measure the amplitude on CH0 of the DSO.

6. Measure the amplitude and frequency of the signal on CH1 of the DSO.

Acceptance Criteria

The amplitude on CH0 of the DSO is between 285 and 300 mV peak to peak.

A square wave on CH1 of the DSO has an amplitude of approximately 2 V peak to peak.

The signal frequency on CH1 of the DSO is 13.560 MHz ± 7 kHz.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- Report failure to EMVCo and request advice.
- Wait until EMVCo gives feedback before starting any such test.
6.4.1.2 Delay Line Verification

Follow this procedure for delay line verification:

1. Refer to the diagram in Figure 6.6:

   ![Figure 6.6—Diagram for the EMV – TEST CMR Delay Line Verification](image)

   Connect appropriate devices so as to implement the functionalities shown.

2. Connect the power supplies to the appropriate voltage connection points, switch on the power supplies and check that the current drawn is within the limits shown in Table 6.3:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>+12 V</td>
<td>150 mA</td>
</tr>
<tr>
<td>-12 V</td>
<td>350 mA</td>
</tr>
<tr>
<td>+5 V</td>
<td>1300 mA</td>
</tr>
</tbody>
</table>

   **Table 6.3—Power Supply Parameters**

3. Set up the EMV – TEST CMR relays as shown in Table 6.4:

<table>
<thead>
<tr>
<th>Relay</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>J2</td>
</tr>
<tr>
<td>Clock</td>
<td>Internal recovery</td>
</tr>
<tr>
<td>Amplifier</td>
<td>Buffer</td>
</tr>
</tbody>
</table>

   **Table 6.4—Test CMR Settings**

4. Set the Waveform Generator to 13.56 MHz with an amplitude of 300 mV peak to peak.

5. Using the I2C interface, adjust the delay settings for DL1 and DL2.
Acceptance Criteria

The phase of the main clock signal on CH1 of the DSO shall be modified by steps according to the adjustment made to the delay lines.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- Report failure to EMVCo and request advice.
- Wait until EMVCo gives feedback before starting any such test.

6.4.1.3 Main Clock Verification

1. Refer to the diagram in Figure 6.7:

   ![Diagram](image)

   **Figure 6.7—Diagram for the EMV – TEST CMR Main Clock Verification**

   Connect appropriate devices so as to implement the functionalities shown.

2. Connect the power supplies to the appropriate voltage connection points, switch on the power supplies and check that the current drawn is within the limits shown in Table 6.5:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>+12 V</td>
<td>150 mA</td>
</tr>
<tr>
<td>-12 V</td>
<td>350 mA</td>
</tr>
<tr>
<td>+5 V</td>
<td>1300 mA</td>
</tr>
</tbody>
</table>

   **Table 6.5—Power Supply Parameters**
3. Set up the EMV – TEST CMR relays as shown in Table 6.6:

<table>
<thead>
<tr>
<th>Relay</th>
<th>Input</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>J2</td>
</tr>
<tr>
<td>Clock</td>
<td>External recovery (input J1)</td>
</tr>
<tr>
<td>Amplifier</td>
<td>Buffer</td>
</tr>
</tbody>
</table>

Table 6.6—EMV – TEST CMR Settings

4. Set the Waveform Generator to 13.56 MHz with an amplitude of 300 mV peak to peak.

5. Observe the signal on CH1 of the DSO.

Acceptance Criteria

If the signal on CH1 of the DSO is a square wave with an amplitude of approximately 2 V peak to peak, the verification is successful.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- Report failure to EMVCo and request advice.
- Wait until EMVCo gives feedback before starting any such test.
6.4.2 EMV TEST CMR Gain Measurement

Follow this procedure for the EMV – TEST CMR gain measurement:

1. Refer to the diagram in Figure 6.8:

   Connect appropriate devices so as to implement the functionalities shown.

   The connection between the DSO and the Waveform Generator is made with two SMA cables of 50 cm or less, interconnected by an I-SMA adaptor which is a female to female SMA adaptor.

2. Set the Waveform Generator to 13.56 MHz with an amplitude of 1 V peak to peak into 50 Ω.

3. Measure the peak to peak amplitude on CH0 of the DSO.

4. Refer to the diagram in Figure 6.9:

   Using the same cables used in previous steps, remove the I-SMA adaptor and substitute the CMR in its place, using input J2 and output J4, to implement the functionalities shown.

   The accuracy of the gain measurement strongly depends on using the same cables in the same positions.
6. Switch on the power supplies and check that the current drawn is within the limits shown in Table 6.7.

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>+12 V</td>
<td>150 mA</td>
</tr>
<tr>
<td>-12 V</td>
<td>350 mA</td>
</tr>
<tr>
<td>+5 V</td>
<td>1300 mA</td>
</tr>
</tbody>
</table>

Table 6.7—Power Supply Parameters

7. Wait 5 minutes for the EMV – TEST CMR to reach operating temperature.
8. Set up the EMV – TEST CMR relays as shown in Table 6.8:

<table>
<thead>
<tr>
<th>Relay</th>
<th>Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>Clock</td>
</tr>
<tr>
<td>Internal recovery</td>
<td>Amplifier Buffer</td>
</tr>
</tbody>
</table>

Table 6.8—EMV – TEST CMR settings

9. Make sure that the Waveform Generator is still set to generate a 13.56 MHz sine wave with an amplitude of 1 V peak to peak into 50 Ω.
10. Measure the peak to peak amplitude on CH0 of the DSO.
11. Calculate the gain by dividing the voltage measured in step 10 by the voltage measured in step 3.

Acceptance Criteria

The EMV – TEST CMR gain shall be within 1% of the value specified in the EMV – TEST CMR verification report provided by the EMV – TEST CMR supplier.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- Report failure to EMVCo and request advice.
- Wait until EMVCo gives feedback before starting any such test.
6.5 EMV TEST PCD and EMV TEST PICC Cross Verification

The following procedure shall take place in an environment where the temperature is 23°C ± 3°C and the relative humidity is 50%RH ± 10%RH.

**Note**

To avoid the possibility of damaging the DSO used in this procedure, make sure that the voltage provided by the signal generator and entering DSO does not exceed the power handling limits of the DSO.

6.5.1 Cross Verifying the EMV TEST PCD and the EMV TEST PICC

Follow this procedure for the cross verification:

1. Refer to the diagram in Figure 6.10:

   ![Diagram for the EMV TEST PCD and EMV TEST PICC Cross Verification](image)

   **Figure 6.10—Diagram for the EMV – TEST PCD and EMV – TEST PCD Cross Verification**

2. Connect appropriate devices so as to implement the functionalities shown.
3. Set the Waveform Generator frequency to 13.56 MHz.
4. Set the signal generator to obtain 15.5 Vpp on CH0 of the DSO.
5. Switch the amplifier off and disconnect the cable to CH0 of the DSO.
6. Refer to the diagram in Figure 6.11:

![Diagram](image.png)

Note 1: Probe can be passive or active, >1MΩ, <15 pF.

**Figure 6.11—Diagram for the EMV – TEST PCD and EMV – TEST PCD Cross Verification**

7. Connect appropriate devices so as to implement the functionalities shown.
8. Place the EMV – TEST PICC at position (2, 0, 0) above the EMV – TEST PCD.
9. Measure the voltage at J1 of the EMV – TEST PICC.
10. Repeat steps 1 to 9 five times and calculate the average value of the five voltage measurements obtained.

**Acceptance Criteria**

Verification is successful if the voltage measured at input J1 of the EMV – TEST PICC is 5.53 ± 0.10 V DC.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

**Failure Action**

A fail message requires the following actions:

- Request another verification of the EMV – TEST PCD.
- Request another verification of the EMV – TEST PICC.
7

PCD Analogue Test Plan

This chapter describes the preparations and procedures for efficient and complete testing of PCDs supplied by a vendor.

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7.1 Prerequisites

Before proceeding with the PCD analogue test plan and its Test Cases, the Testing Laboratory shall use the knowledge acquired in previous chapters to construct a test environment.

Before performing Test Cases for PCDs, make sure that Test Laboratory staff:

- Is familiar with the positioning conventions and requirements (see Chapter 2).
- Is familiar with the EMV Test Equipment (see Chapter 3).
- Is familiar with the recommendations for Frame Delay Time Measurements (see Appendix E).
- Has built a Test Bench for PCD testing that conforms to specifications (see Chapter 4).
- Has verified the EMV Test Equipment (see Chapter 6).
- Has established and maintains measurement uncertainty calculations as described in the ISO/IEC 17025 standard.

Note

If necessary, refer to Appendix D for a detailed description of a specific Test Bench implementation.
7.2 Understanding the Two Types of Modulation

Before performing the Test Cases and set up the EMV Test Equipment, the Testing Laboratory shall become familiar with the two types of load modulation used in the tests found in this manual.

The “Dogs” software has been used to produce the signal displays in the following sections.

Alternative acquisition and processing solutions for load modulation not involving the “Dogs” software are also acceptable.

7.2.1 Type A Load Modulation

Figure 7.1 shows the Type A load modulation envelope signal:

An Acquisition Device acquires the Type A load modulation signal at the output J4 of the EMV – TEST CMR.

The crenellations in Figure 7.1 are not included in the calculations.
Figure 7.2 shows a close-up of the 7 cycles subject to calculation by the automated measurement:

![Figure 7.2—Type A Load Modulation](image)

Over at least seven successive subcarrier cycles of the same phase state, the automated measurement shall calculate the difference between the average value of all the positive peaks (upper carrier levels) and the average value of all the negative peaks (lower carrier levels).

### 7.2.2 Type B Load Modulation

Figure 7.3 shows the Type B load modulation signal after synchronous peak sampling:

![Figure 7.3—Type B Load Modulation Signal](image)

An Acquisition Device acquires the Type B load modulation signal at the output J4 of the EMV – TEST CMR.
See Figure 7.4 for a close-up of the 8 cycles subject to calculation by the automated measurement for Type B load modulation.

**Note**

Peaks due to phase transitions shall not be taken into account for the load modulation measurement.

**Figure 7.4—Type B Load Modulation**

Over at least seven successive subcarrier cycles of the same phase state, the automated measurement shall calculate the difference between the average value of all the positive peaks (upper carrier levels) and the average value of all the negative peaks (lower carrier levels).
7.3 Preliminary Set-ups

Before performing the Test Cases, it is necessary to set up the EMV Test Equipment.

Note

The EMV – TEST CMR does not require any set-up.

The set-up of the EMV Test Equipment for PCD testing comprises two steps:

• Setting up the EMV – TEST PCD
• Setting up the EMV – TEST PICC

The EMV – TEST PCD field strength shall be a known value to allow subsequent set-up of the EMV – TEST PICC. These two steps shall be performed sequentially as described and as a single pass procedure as they are dependent.

Note

Unless specified otherwise in the test case description, a positive load modulation shall be used.

Note

Even when a specific DTE mode is mentioned in a Test Case procedure, the “loopback” mode may be used during all Type Approval test cases, provided that the software of the Test Bench is capable of correctly setting the required test conditions and of correctly measuring the requested signal(s) at the appropriate moment.

7.3.1 Setting up the EMV TEST PCD Power/EMV TEST PICC Positive Load Modulation Intensity

This set-up involves two steps:

• Setting up the power of the EMV – TEST PCD
• Setting up the EMV – TEST PICC positive load modulation intensity

A PCD emulation provides a carrier signal to the EMV – TEST PCD. A Power Sensing Device connected to J1 on the EMV – TEST PICC measures the power sent by the PCD emulation through the EMV – TEST PCD.

Note

When setting up the EMV – TEST PCD, the power sent by the RF Amplifier output shall never exceed 1 W. For example, when connecting the RF Amplifier output to a DSO channel set to 50 Ω, the output shall never measure more than 20 V peak to peak.
Follow this procedure for the EMV – TEST PCD power set-up and EMV – TEST PICC positive load modulation intensity set-up:

1. Refer to Figure 7.5:

- Refer to Figure 7.5:

**Figure 7.5—Block Diagram for the EMV – TEST PCD Power Set-up and EMV-Test PICC Positive Load Modulation Intensity Set-up**

In this set-up procedure, if the PICC Emulation Device needs an external trigger to generate PICC answers, this signal is not issued by the Synchronization Device but by a Waveform Generator. Such a component shall generate a trigger signal with a delay between triggers equal to or greater than 100 ms and with a format matching the specification of the PICC emulation trigger input.

2. Connect appropriate Test Bench devices so as to implement the functionalities shown in Figure 7.5 except the connection to J2 of the EMV – TEST PICC.

3. Set up the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Place the EMV – TEST PICC at position \((z=2, r=0, \varphi=0)\) on the EMV – TEST PCD.

5. Adjust the PCD Emulation Device to send a 13.56 MHz sine wave.

6. Set the Power Sensing Device time scale to allow averaging over 10 \(\mu\)s to 200 \(\mu\)s and the voltage scale to an appropriate level and offset to give best accuracy.

7. Measure the average voltage \(V_{OV}\) at output connector J1 of the EMV – TEST PICC.

8. If the measured \(V_{OV}\) is the value \(V_{N,OV}\) defined in Table B.1 of Appendix B, go to step 9. If it is not, adjust the waveform amplitude of the PCD Emulation Device and repeat steps 6 and 7.

9. Remove the EMV – TEST PICC from the Operating Volume of the EMV – TEST PCD.

10. Connect the end of the cable installed in step 2 to J2 of the EMV – TEST PICC.

11. Set the EMV – TEST CMR with the control software as shown in Table 7-1:

<table>
<thead>
<tr>
<th>Function</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>J2</td>
</tr>
<tr>
<td>Clock</td>
<td>CLK IN (internal recovery)</td>
</tr>
<tr>
<td>Amplifier</td>
<td>Buffer</td>
</tr>
</tbody>
</table>

**Table 7-1—CMR Parameter Settings**

12. Place the EMV – TEST PICC in the appropriate position on the EMV – TEST PCD. The exact position depends on the test being performed:

   a. For the \(V_{s1,pp}\) test, the position is \((z=0, r=0, \varphi=0)\).
   
   b. For the \(V_{s2,pp}\) test, the position is \((z=2, r=0, \varphi=0)\).

13. Set the PICC Emulation device to generate positive load modulation.

14. Send a correct Type A or Type B PICC answer with a content equivalent to a Response to Select PPSE Command as defined in Appendix C.

15. Set the EMV – TEST CMR delay lines DL1+DL2 until the maximum amplitude is observed on the Acquisition Device.

16. In case of minimum load modulation setup, set the Acquisition Device x-axis to capture the first 7 contiguous subcarrier cycles of the PICC response to Select PPSE command.

   In case of nominal or maximum load modulation setup, set the Acquisition Device x-axis to capture the last 7 contiguous subcarrier cycles without phase change of the PICC response to Select PPSE command.

17. Set the Acquisition Device vertical scale to maximum.
The automated test bench set-up measures the load modulation as the difference between the average value of upper subcarrier peaks and the average value of subsequent lower subcarrier peaks at the output J4 of the EMV – TEST CMR.

18. If the measured load modulation level is not the one required for the test, set the amplitude of the signal on input J2 of the EMV – TEST PICC.

19. Repeat step 17 and 18 until the required value for load modulation is reached.

20. Remove the EMV – TEST PICC from the Operating Volume of the EMV – TEST PCD.

The PICC Emulation device works properly if the output J2 of the EMV – TEST PCD shows an increasing voltage above the unmodulated carrier when the subcarrier is switched on, as shown in Figure 7.6. Unless specified in the Test Cases, the envelope of the output J2 of the EMV – TEST PCD shows an increasing voltage above the unmodulated carrier when the subcarrier is switched on, as shown in Figure 7.6. In some test cases, inverted load modulation is applied as shown in Figure 7.8.

![Figure 7.6—Positive load modulation](image)
7.3.2 Setting up the EMV TEST PCD Power/EMV TEST PICC Negative Load Modulation Intensity

This set-up involves two steps:

- Setting up the power of the EMV – TEST PCD
- Setting up the EMV – TEST PICC negative load modulation intensity

A PCD emulation provides a carrier signal to the EMV – TEST PCD. A Power Sensing Device connected to J1 on the EMV – TEST PICC measures the power sent by the PCD emulation through the EMV – TEST PCD.

Note

When setting up the EMV – TEST PCD, the power sent by the RF Amplifier output shall never exceed 1 W. For example, when connecting the RF Amplifier output to a DSO channel set to 50 Ω, the output shall never measure more than 20 V peak to peak.
Follow this procedure for the EMV – TEST PCD power set-up and EMV – TEST PICC negative load modulation intensity set-up:

1. Refer to Figure 7.7:

![Block Diagram for the EMV – TEST PCD Power Set-up and EMV-Test PICC Negative Load Modulation Intensity Set-up](image)

Note 1: Probe can be passive or active, >1MΩ, <15 pF. The Power Sensing Device input impedance shall match the probe impedance.

Note 2: J9 must be terminated by a 50 Ω load at all times.

2. Connect appropriate Test Bench devices so as to implement the functionalities shown in Figure 7.7 except the connection to J2 of the EMV – TEST PICC.

3. Set up the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Place the EMV – TEST PICC at position (z=2, r=0, φ=0) on the EMV – TEST PCD.

5. Adjust the PCD Emulation Device to send a 13.56 MHz sine wave.

6. Set the Power Sensing Device time scale to allow averaging over 10 µs to 200 µs and the voltage scale to an appropriate level and offset to give best accuracy.

7. Measure the average voltage $V_{OV}$ at output connector J1 of the EMV – TEST PICC.

8. If the measured $V_{OV}$ is the value $V_{N,OV}$ defined in Table B.1 of Appendix B, go to step 9. If it is not, adjust the waveform amplitude of the PCD Emulation Device and repeat steps 6 and 7.

9. Remove the EMV – TEST PICC from the Operating Volume of the EMV – TEST PCD.

10. Connect the end of the cable installed in step 2 to J2 of the EMV – TEST PICC.

11. Set the EMV – TEST CMR with the control software as shown in Table 7-2:

<table>
<thead>
<tr>
<th>Function</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>J2</td>
</tr>
<tr>
<td>Clock</td>
<td>CLK IN (internal recovery)</td>
</tr>
<tr>
<td>Amplifier</td>
<td>Buffer</td>
</tr>
</tbody>
</table>

Table 7-2—CMR Parameter Settings

12. Place the EMV – TEST PICC in the appropriate position on the EMV – TEST PCD. The exact position depends on the test being performed:
   a. For the $V_{s1,pp}$ test, the position is (z=0, r=0, φ=0).
   b. For the $V_{s2,pp}$ test, the position is (z=2, r=0, φ=0).

13. Set the PICC Emulation device to generate negative load modulation.

14. Send a correct Type A or Type B PICC answer with a content equivalent to a Response to Select PPSE Command as defined in Appendix C.

15. Set the EMV – TEST CMR delay lines DL1+DL2 until the maximum amplitude is observed on the Acquisition Device.

16. In case of minimum load modulation setup, set the Acquisition Device x-axis to capture the last 7 contiguous subcarrier cycles without phase change of the PICC response to Select PPSE command.
   In case of nominal or maximum load modulation setup, set the Acquisition Device x-axis to capture the first 7 contiguous subcarrier cycles of the PICC response to Select PPSE command.

17. Set the Acquisition Device vertical scale to maximum.
The automated test bench set-up measures the load modulation as the difference between the average value of upper subcarrier peaks and the average value of subsequent lower subcarrier peaks at the output J4 of the EMV – TEST CMR.

18. If the measured load modulation level is not the one required for the test, set the amplitude of the signal on input J2 of the EMV – TEST PICC.

19. Repeat step 17 and 18 until the required value for load modulation is reached.

20. Remove the EMV – TEST PICC from the Operating Volume of the EMV – TEST PCD.

The PICC Emulation device works properly if the output J2 of the EMV – TEST PCD shows a decreasing voltage below the unmodulated carrier when the subcarrier is switched on, as shown in Figure 7.8.

Figure 7.8—Negative load modulation
7.4 Set-up of the PCD Sample

By default, all PCD functions shall be considered deactivated and the polling for technologies (different from Type A and Type B transactions) disabled. The PCD set-up required for each Test Case is described in the test procedures.

Before any PCD test, the PCD Sample shall be set up with one of the different control possibilities described below:

- Continuous sending of the carrier with no polling (CARRIER mode).
- The PCD polls (POLLING mode) in two ways:
  - The PCD polls as described in section 9.2 of the EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification, if the polling for other technologies is enabled.
  - The PCD polls between Type A and Type B, sending WUPA and WUPB commands only if the polling for other technologies is disabled.
- The PCD generates a RESET (RESET Mode).
- The PCD sends a WUPA command (WUPA mode).
- The PCD sends a WUPB command (WUPB mode).
- The PCD sends the commands of the Collision Detection procedure as described in section 9.3.3 of the EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification and the commands of the activation procedure described in section 9.4.2 of the EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification (ATTRIB Mode).
- The PCD activates the Loopback application (LOOPBACK mode).

Otherwise unless specified in the Test Cases, other technologies shall be disabled.

For further information on this DTE, see Appendix A of the EMVCo Type Approval Contactless Terminal Level 1/ Device Test Environment document.

When Type A or Type B transactions are used, the following factors must be taken into account:

- Polling for other technologies is disabled.
- The WUPA, WUPB, RATS and ATTRIB modes all require that a carrier be active prior to the polling activity.
7.5 Identifying PCD Test Cases

To facilitate future referencing, all PCD Test Cases shall be identified by a unique label according to the following format:

ZLCN. zrf

Where:

- Z is the PCD data transmission type:
  - TAB = both PCD data transmission Type A and Type B
  - TA = PCD data transmission Type A
  - TB = PCD data transmission Type B
- L is the level of the test (level 1 Type Approval Tests described).
- C is the test category:
  - 1 = Radio frequency power tests
  - 2 = Signal interface PCD to PICC tests
  - 3 = Signal interface PICC to PCD tests
  - 4 = Sequence, Frame bit coding and synchronization tests
- N is the number of the test in the specified category.

z, r and f are identifiers for label points, as defined in Chapter 2, section 2.4.1 Target Position Conventions.
7.6 Measurement Uncertainty

Testing Laboratories shall have and shall apply procedures for estimating uncertainty of measurement. The ISO/IEC 17025, ISO 5725 and the Guide to the expression of Uncertainty of Measurement requirements allow the Testing Laboratory to evaluate the accuracy, repeatability and reproducibility of its own test results and to properly determine and quantify sources of error.

These procedures are essential feedback mechanisms enabling the Test Laboratory to improve the quality of its measurements. This is done by minimizing the identified sources of error through optimization of methods and procedures.

For each test method, according to the present document, the Testing Laboratory shall calculate measurement uncertainty figures. These shall correspond to an expansion factor (coverage factor) of $k = 1.96$ (which provides a confidence level of 95% in the case where the distributions characterizing the actual measurement uncertainties are normal (Gaussians). Table 7-3, Table 7-4 and Table 7-5 are based on such expansion factors.

The estimation of measurement uncertainties shall be done according to recognized international methods. When estimating the uncertainty of measurement, all uncertainty components which are relevant and significant in the given situation shall be taken into account using appropriate methods of analysis.

Sources contributing to uncertainty include, but are not limited to:

- Reference standards
- Methods and equipment
- Environmental conditions
- Effects of positional accuracy
- Mismatches
- Cable losses
- Sampling rates and timing factor
- Operator skills
- Properties and condition of the tested samples

### Table 7-3—Parameter and Signal Generation Uncertainty Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Uncertainty</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{SOV}$</td>
<td>± 2 %</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>± 100 Hz</td>
</tr>
<tr>
<td>Load modulation ($V_{S1}$, $V_{S2}$)</td>
<td>± 1 mV</td>
</tr>
<tr>
<td>Bit rate (PICC Load Modulation)</td>
<td>± 0.2 %</td>
</tr>
<tr>
<td>Type B PICC bit coding set-up ($t_{PICC,S1}$, $t_{PICC,S2}$, $t_{PICC,E}$, EGT$_{PICC}$)</td>
<td>± 2/fc</td>
</tr>
<tr>
<td>Type B PICC TR0, TR1, t$_{FSOFF}$</td>
<td>± 2/fc</td>
</tr>
<tr>
<td>FDT$_{A,PICC}$</td>
<td>± 1/fc</td>
</tr>
</tbody>
</table>

### Table 7-4—Parameter and Environmental Condition Uncertainty Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Uncertainty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positioning ($z$, $r$)</td>
<td>± 1 mm</td>
</tr>
<tr>
<td>Positioning ($\phi$, $\theta$)</td>
<td>± 0.1 rad</td>
</tr>
<tr>
<td>Temperature</td>
<td>± 1°C</td>
</tr>
<tr>
<td>Humidity</td>
<td>± 3 %</td>
</tr>
</tbody>
</table>

### Table 7-5—Parameter and Measurement Uncertainty Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Uncertainty</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OV}$</td>
<td>± 2 %</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>± 100 Hz</td>
</tr>
<tr>
<td>Load modulation ($V_{PP}$)</td>
<td>± 10% with a minimum of 1 mV</td>
</tr>
<tr>
<td>Type A timing ($t_1$, $t_2$, $t_3$, $t_4$, $t_5$)</td>
<td>± 2/fc</td>
</tr>
<tr>
<td>Type A ringing level</td>
<td>± 0.5 % of $V_1$</td>
</tr>
<tr>
<td>Type A overshoots</td>
<td>± 0.5 % of $V_1$</td>
</tr>
<tr>
<td>Bit rate (PCD Type A / Type B modulation)</td>
<td>± 0.5 %</td>
</tr>
<tr>
<td>Type B modulation index</td>
<td>± 0.5 %</td>
</tr>
<tr>
<td>Type B rise and fall times</td>
<td>± 2/fc</td>
</tr>
<tr>
<td>Type B overshoots and undershoots</td>
<td>± 1 % of ($V_1$-$V_2$)</td>
</tr>
<tr>
<td>Type B bit coding ($t_{PCD,S1}$, $t_{PCD,S2}$, $t_{PCD,E}$, EGT$_{PCD}$)</td>
<td>± 2/fc</td>
</tr>
</tbody>
</table>
Note
The previous tables include the mismatch effects and the effects on measurements in the near field due to positional accuracy.

Note
For the peak sampling method using the EMV–TEST CMR, the delay line shall be adjusted until the maximum amplitude is reached on the Acquisition Device.

Note
When establishing measurement points with a cursor (or its equivalent), unless otherwise stated in the test procedure, always use the reference points as specified in Appendix E. Do this consistently to maintain measurement accuracy.
7.7 Interpretation of the Measurement Results

The interpretation of the results recorded in a test report for the measurements described in the present document shall be as follows:

- The value of the measurement uncertainty for the measurement of each parameter shall be included in the test report.
- The recorded value of the measurement uncertainty shall be, for each measurement, equal to or lower than the values in Table 7-3, Table 7-4 and Table 7-5.
- The shared risk approach shall be applied for the interpretation of measurement results.

Note

The shared risk approach is an agreement on limits between the vendor and the regulator.
7.8 Performing PCD Test Cases

When Test Cases are performed, results are normally a PASS or a FAIL verdict.

The following procedure applies to each test case from TA131 up to and including TA138 for Type A and from TB131 up to and including TB138 for Type B (i.e. for each position and each test subcase):

- It is allowed to run each test subcase a maximum of six times.
- When three consecutive runs of the same test subcase succeed, record a PASS message and proceed to the next test subcase.
- After performing the sixth test run of the same test subcase without three consecutive successes, record a FAIL message and proceed to the next test subcase.

It is not allowed to run any test subcase from TA131 up to and including TA138 for Type A and from TB131 up to and including TB138 for Type B more than six times during one Type Approval session.

For all other Test Cases, the following procedure applies (i.e. for each position and each test subcase):

- It is allowed to run each test subcase a maximum of three times.
- When one run of the same test subcase succeed, record a PASS message and proceed to the next test subcase.
- After performing the third test run of the same test subcase without success, record a FAIL message and proceed to the next test subcase.

It is not allowed to run any of these test subcases more than three times during one Type Approval session.

In the above text, the counting of test times is incremented by one unit each time that the test bench at least starts answering a WUP command from the PCD under test, sent with the modulation type that is concerned by the test case performed.

- When the PCD under test polls using a modulation type that is not concerned by the test case run, the number of test times shall not be incremented. For example, when running the test TB132, all occurrences of WUPA commands shall be discarded.
- When the PCD under test polls using the modulation type that is concerned by the test case but the test bench does not answer, the number of test times shall not be incremented. For example, a WUPA command that is not answered by the test bench running test TA124 shall be discarded.
- Each time that the test bench starts answering a WUP command sent by the PCD under test using the modulation type concerned by the test case performed, the number of test times shall be incremented by one unit.
If the Test PCD has a concave surface to place against the EMV – TEST PICC, you shall follow the recommendations in the "Recommendations for a PCD without a perfectly flat Landing Plane" section in Chapter 5.

The following sections present all the PCD Test Cases. They are presented in the sequence defined in the specifications. Test Cases may be performed in any order unless otherwise specified in a Test Case.

To perform the Test Cases, a Test Bench implementing essential functionalities shall be constructed. Figure 7.9 shows the necessary functionalities:

Note 1: Probe can be passive or active, >1MΩ, <15 pF.
Note 2: The EMV - TEST CMR is specified for the Load Modulation Adjustment set-up.
Note 3: A Frequency Counter is used for some tests.
A Frequency Counter function in another test instrument may also be used.

Figure 7.9—Block Diagram of the Test Bench to Perform the Test Cases

Note
Make sure that you carry out any special connections as described in individual Test Cases.

Note
All Test Cases shall be completed without regard to individual test failure.

Note
The use of a low-pass filter fitted between the PICC and the EMV – TEST CMR is highly recommended. The filter shall feature less than 1 dB attenuation at 20 MHz and more than 40 dB attenuation at 40 MHz.
7.8.1 Radio Frequency Power

These tests determine the quality of the radio frequency fields of the PCD under test.

7.8.1.1 TAB111.zrf Verifying the PCD to PICC Power Transfer

This test verifies the power transmission from the PCD to the PICC.

Test Code

TAB111.zrf

Reference

This test refers to requirement 3.2.1.1.

Test Positions

Use Table 7-6 for the test positions during verification of the power transmission from the PCD to the PICC:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
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<td>3</td>
</tr>
<tr>
<td>1</td>
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<td>3</td>
<td>2</td>
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<tr>
<td>3</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>6</td>
</tr>
</tbody>
</table>
Table 7-6—Test Positions of Test TAB111.zrf

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>2</td>
<td>9</td>
</tr>
<tr>
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<tr>
<td>4</td>
<td>1</td>
<td>9</td>
</tr>
</tbody>
</table>

Procedure

Follow this procedure to verify the power transmission from the PCD to the PICC:

1. Connect the Power Sensing Device to output J1 of the EMV – TEST PICC.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1 - 3 and J8 1- 4).
5. Make sure that the CARRIER is switched on.
6. Place the EMV – TEST PICC in the first position of Table 7-6.
7. Set the Power Sensing Device to capture 10 μs of the full level unmodulated signal.
8. Optimize the Power Sensing Device settings for the accurate measurement of amplitude.
9. Launch the acquisition.
10. Determine the true mean value of voltage $V_{OV}$ at output J1 of the EMV – TEST PICC.
11. Repeat steps 8 to 10 for all other positions of Table 7-6.

Acceptance Criteria

Within the Operating Volume, the PCD shall generate a DC voltage $V_{OV}$ at J1 of the EMV – TEST PICC. Refer to Table A.1 in Appendix A for the applicable range of $V_{OV}$ mean values.

When testing PCDs without a perfectly flat landing plane, refer to section 5.2.2. above and adjust the acceptance criteria according to the actual $z$ distance used during testing. The distance is taken from the center of the EMV – Test PICC.
Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.1.2 TAB112.200 Verifying the PCD Carrier Frequency

This test verifies the carrier frequency emitted by the PCD under test.

**Note**
This test requires the use of a Frequency Counter or its functional equivalent in an instrument such as a DSO.

**Test Code**
TAB112.200

**Reference**
This test refers to requirement 3.2.4.1.

**Procedure**
Follow this procedure to verify the carrier frequency emitted by the PCD under test:

1. Connect the Frequency Counter to output J9 of the EMV – TEST PICC.

   **Note**
   Alternatively, the laboratory may use the following connection scheme:
   Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
   Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
   Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a non-linear load (jumper setting J7 1-3 and J8 1-4).
5. Make sure that the CARRIER is switched on.
6. Place the EMV – TEST PICC at position (z=2, r=0, φ=0).
7. Optimize the Acquisition Device settings for the accurate measurement of frequency.
8. Launch the acquisition.
9. Determine the mean value during the acquisition period of the carrier frequency on connector J9 of the EMV – TEST PICC.

**Acceptance Criteria**
The frequency of the Operating Field (carrier frequency) provided by the PCD shall be 13.560 MHz ± 7 kHz.

**Expected Results**
Results are recorded with one of two statements:
• Pass message
• Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.1.3 TAB113.z00 Verifying the PCD Operating Field Resetting

This test verifies how the PCD resets the Operating Field.

Test Code

TAB113.z00

Reference

This test refers to requirement 3.2.6.1.

Test Positions

Use Table 7-7 for the test positions during verification of the power transmission from the PCD to the PICC:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
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</tr>
</tbody>
</table>

Table 7-7—Test Positions of Test TAB113.z00

Procedure

Follow this procedure for verification of the PCD Operating Field reset:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
5. Place the EMV – TEST PICC in the first position of Table 7-7.
6. Make sure that the CARRIER is switched on.
7. Set the Acquisition Device to capture more than 20 ms of signal from the start of the PCD reset of the Operating Field.
8. Optimize the Acquisition Device settings for the accurate measurement of amplitude.
9. Launch the acquisition.
10. Make the PCD under test reset the PCD Operating Field.
11. Measure the RMS voltage of a 20 MHz band limited signal at the output of the EMV – TEST CMR during the reset of the PCD.

12. Measure the time of the reset $t_{\text{RESET}}$ from the point at which the voltage of the envelope first falls below $V_{\text{OV, RESET, MAX}} \times \sqrt{2}$ until it last rises above $V_{\text{OV, RESET, MAX}} \times \sqrt{2}$ at the end of the reset period. The appropriate value of $V_{\text{OV, RESET, MAX}}$ is shown in the maximum column of $V_{\text{OV, RESET}}$ in Table A.1 in Appendix A.

13. Repeat steps 8 to 12 for all other positions of Table 7-7.

Acceptance Criteria

When the PCD resets the Operating Field, then within the Operating Volume, the PCD shall generate for a time $t_{\text{RESET}}$ a voltage less than or equal to the RMS value of $V_{\text{OV, RESET}}$ at the output of the pickup coil of the EMV – TEST PICC. The time interval $t_{\text{RESET}}$ shall conform to the values shown in Table A.5 in Appendix A and the value of $V_{\text{OV, RESET}}$ shall conform to the values shown in Table A.1 in Appendix A.

Note

As a low pass filter is used, the measurement of the signal shall be corrected according to its insertion loss at 13.56 MHz.

Note

The measurement should take into account any DC offset introduced by the EMV TEST CMR. This can be achieved for example by measuring the CMR J4 output voltage when no signal is generated, and using a compensated threshold voltage formula: threshold = $\text{CMR}_{\text{offset}} + (V_{\text{OV, RESET, MAX}} \times \sqrt{2})$.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.1.4 TAB114.200 Verifying the PCD Power-Off of the Operating Field

This test verifies how the PCD performs a power-off of the Operating Field.

Test Code

TAB114.200

Reference

This test refers to requirement 3.2.9.1.

Procedure

Follow this procedure for verification of the PCD power-off of the Operating Field:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.

2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a nominal positive load modulation V_{S1pp}. See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of V_{S1pp}. In this test case, the EOT Command must be set to “Power-Off procedure”.

5. Place the EMV – TEST PICC at position (z=2, r=0, \phi=0).

6. Set the DTE in LOOPBACK mode.

7. Set the Acquisition Device to capture more than 20 ms of signal from the start of the PCD power-off of the Operating Field at the end of the transaction.

When using the Dogs software, capturing the whole transaction in asynchronous high-speed mode is not possible. You may want to delay appropriately the start of the acquisition by using the “Trigger delay” function of the “Config CMR/ADC” tab.

8. Optimize the Acquisition Device settings for the accurate measurement of amplitude.

9. Launch the acquisition.

10. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests. The second byte of the EOT Command shall be equal to ‘72’.

11. Place an X-cursor or its equivalent to identify the time when the voltage of the envelope first falls below V_{OV,POWEROFF,MAX} \times \sqrt{2}. This cursor shall be referenced as X_1.
12. Place an X-cursor or its equivalent to identify the time \( (X_1 + t_{POWEROFF,MIN}) \) after the \( X_1 \) start cursor. This cursor shall be referenced as \( X_2 \).

13. Place an Y-cursor or its equivalent to identify the voltage \( V_{OV,POWEROFF,MAX} \). This cursor shall be referenced as \( Y_1 \).

14. Measure the RMS voltage of a 20 MHz band limited signal at the output of the EMV – TEST CMR during the power-off of the Operating Field, i.e. between the cursors \( X_1 \) and \( X_2 \).

Acceptance Criteria

When the PCD performs a power-off of the Operating Field, the PCD shall, during a time \( t_{POWEROFF,MIN} \), generate a RMS voltage less than or equal to \( V_{OV,POWEROFF,MAX} \) at the output of the pickup coil of the EMV – TEST PICC. The value of \( V_{OV,POWEROFF,MAX} \) shall conform to the values shown in Table A.1 in Appendix A.

\[ \text{Expected Results} \]

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

\[ \text{Note} \]

As a low pass filter is used, the measurement of the signal shall be corrected according to its insertion loss at 13.56 MHz.

\[ \text{Note} \]

The measurement should take into consideration any DC offset introduced by the EMV TEST CMR. This can be achieved for example by measuring the CMR J4 output voltage when no signal is generated, and using a compensated threshold voltage formula: \( \text{threshold} = \text{CMR}_{\text{offset}} + (V_{OV,POWEROFF,MAX} \times \sqrt{2}) \).
7.8.1.5 TAB115.200 Polling sequence when supporting other technologies

This test verifies if a PCD is polling correctly when other technologies than Type A and Type B are supported.

This test case is applicable only if the PCD supports other technologies.

Test Code

TAB115.200

Reference

This test refers to requirements 9.2.1.1, 9.2.1.3, 9.2.1.4 and 9.2.1.7.

Procedure

Follow this procedure to verify a PCD is polling correctly when other technologies than Type A and Type B are supported:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

3. Place the EMV – TEST PICC at position (200).

4. Set the DTE in LOOPBACK mode with other technologies activated.

5. Set the Acquisition Device to capture 60 ms of signal starting 21 ms before the beginning of the WUPA of the polling loop.

6. Record the viewable trace on EMV Test PICC J9 output.

7. Observe the PCD polling sequence and verify that:
   a. The polling loop is ending with a reset, and measure its duration.
   b. This reset is followed by the WUPA command of the polling sequence.
   c. There is no ASK modulation between reset and WUPA.
   d. This WUPA command is followed by the WUPB command of the polling sequence.
   e. There is no ASK modulation between WUPA and WUPB.
   f. There is no ASK modulation after WUPB for at least FWT_{ATQB}.

Note

We consider that there is no ASK modulation when the signal does not decrease below V_{1} \times 95\% during more than 1 \mu s and does not increase over V_{1} \times 105\% during more than 1 \mu s, with V_{1} being the level of the upper signal envelope between two PCD commands.
Acceptance Criteria

When the PCD supports other technologies:

- The PCD shall reset the Operating Field during a time $t_{\text{RESET}}$ before restarting the polling loop. Refer to Table A.5 in Appendix A.1 for the minimum and maximum $t_{\text{RESET}}$ values.
- The PCD shall wait a time $FWT_{ATQB}$ with unmodulated carrier before sending any proprietary command. Refer to Table A.4 in Appendix A.1 for the minimum $FWT_{ATQB}$ value.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
### 7.8.2 PCD to PICC Signal Interface for Type A Communications

PCD to PICC Type A communication uses the modulation principle of 100% ASK. The carrier is switched on and off, creating the lower level when switched off. In practice, it results in a modulation index of 90% or higher.

Figure 7.10 shows the lower level for Type A communications:

In this section, V (voltage) represents the envelope of the signal measured at the output of the pickup coil of the EMV – TEST PICC within the Operating Volume of the PCD. The envelope (V) is obtained by applying a moving average with a period of 1/fC on the magnitude of the complex Hilbert transform of the signal.

V1 is the initial value measured immediately before any modulation is applied by the PCD. V2, V3 and V4 are defined as follows:

- V2 = 0.05 × V1
- V3 = 0.6 × V1
- V4 = 0.9 × V1
It is strongly recommended to perform these test cases using the same acquisitions to avoid any random behavior of the PCD under test.

7.8.2.1 TA121.z00 Verifying the t₁ Timing

This test verifies the time between V₄ of the falling edge to V₂ of the rising edge within a given time t₁.

Test Code

TA121.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 7-8 for the test positions during verification of the time t₁ between V₄ of the falling edge to V₂ of the rising edge.

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<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
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Table 7-8—Test Positions of Test TA121.z00

Procedure

Follow this procedure to verify the time t₁ between V₄ of the falling edge to V₂ of the rising edge.

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

5. Place the EMV – TEST PICC in the first position defined in Table 7-8.

6. Make sure that the CARRIER is switched on and set the PCD under test in mode.
7. Set the Acquisition Device to capture 10 μs of the PCD signal centered upon one
   pause within the WU PA command sent by the PCD.

8. Optimize the Acquisition Device settings for accurate measurement of waveform
   level and timing.

9. Launch the acquisition.

10. Identify the signal positive peak amplitude V1.

11. Calculate V4 as equal to 0.9 × V1 and place a Y-cursor (or its equivalent) to
determine the corresponding level.

12. Measure V2 as equal to 0.05 × V1 and place a Y-cursor (or its equivalent) to
determine the corresponding level.

13. Place an X-cursor (or its equivalent) to determine the time where the PCD carrier
envelope crosses V4 for the first time as the carrier envelope decays.

14. Place an X-cursor (or its equivalent) to determine the time where the PCD carrier
crosses cursor V2 for the first time as the carrier envelope increases (excluding any
temporary increase above V2 due to ringing).

15. Determine the timing t1, when V decreases through V4 to when V increases through
V2, as the difference between the times identified by the two X-cursors.

16. Repeat steps 8 to 15 for all positions defined in Table 7-8.

Acceptance Criteria

V shall decrease from V4 to less than V2 and subsequently increase to greater than V2 in
time interval t1. The time interval t1 shall conform to the values shown in Table A.2 in
Appendix A.

Expected Results

Results are recorded with one of two statements:

• Pass message

• Fail message including a list of all failed conditions and reference details of the
  acceptance criterion not met.
7.8.2.2 TA122.z00 Verifying the Monotonic Decrease from V4 to V2

This test verifies the monotonic decrease of V from V4 to less than V2.

Test Code

TA122.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 7-9 for the test positions during verification that the monotonic decrease of V is from V4 to less than V2:

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<th>Value for z</th>
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Table 7-9—Test Positions of Test TA122.z00

Procedure

Follow this procedure to verify that the monotonic decrease of V is from V4 to less than V2:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

5. Place the EMV – TEST PICC in the first position defined in Table 7-9.

6. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.

7. Set the Acquisition Device to capture 10 μs of the PCD signal centered upon one pause within the WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.

Figure 7.11 shows a typical waveform envelope display:

![Figure 7.11—Non Monotonic Decrease](image)

10. Identify the signal positive peak amplitude V₁.

11. Calculate V₄ as equal to 0.9 × V₁ and place a Y-cursor (or its equivalent) to determine the corresponding level.

12. Calculate V₂ as equal to 0.05 × V₁ and place a Y-cursor (or its equivalent) to determine the corresponding level.

13. Determine when the PCD carrier envelope decreases through V₄ on the first falling edge.

14. Determine when the PCD carrier envelope decreases through V₂ on the first falling edge.

15. Observe V decreasing from V₄ to less than V₂ on the first falling edge on the PCD carrier envelope. If the carrier envelope decreases continuously between V₄ and V₂, go to step 17. Otherwise go to step 16.

16. Measure (using cursors or their equivalents) the time elapsed between a local maximum value and the previous time that this value was reached. This elapsed time shall be identified as t₅. This shall only apply if the local maximum is greater than V₂. See Figure 7.11 for details.

17. Repeat steps 8 to 16 for all positions defined in Table 7-9.
Acceptance Criteria

If \( V \) does not decrease monotonically, the time \( t_5 \) between a local maximum and the time of passing the same value before the local maximum shall conform to appropriate values shown in Table A.2 in Appendix A.

When multiple \( t_5 \) times happen within one signal decrease period, each individual \( t_5 \) time shall conform to appropriate values shown in Table A.2 in Appendix A.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.2.3 TA123.z00 Verifying the Ringing

This test verifies the ringing following the falling edge, where the falling edge is the part of the envelope V, where V decreases from V₄ to V₂.

Test Code

TA123.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 7-10 for the test positions during verification of the ringing following the falling edge:

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<th>Value for f</th>
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</table>

Table 7-10—Test Positions of Test TA123.z00

Procedure

Follow this procedure to verify the ringing following the falling edge:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC in the first position defined in Table 7-10.
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.
7. Set the Acquisition Device to capture 10 μs of the PCD signal centered upon one pause within the WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.

Figure 7.12 shows the acquired signal:

10. Identify the signal positive peak amplitude $V_1$.

11. Calculate $V_2$ as equal to $0.05 \times V_1$ and place a Y-cursor (or its equivalent) to determine the corresponding level.

12. If there is no signal peak over the level $V_2$, occurring after the carrier envelope has initially reached this level, then go to step 13. Otherwise, the maximum amplitude due to ringing of any peaks above level $V_2$ and occurring after the carrier envelope has initially reached this level shall be measured (using cursors or their equivalents).

13. Repeat steps 8 to 12 for all positions defined in Table 7-10.

**Acceptance Criteria**

When no ringing is observed, the result shall be “Pass”. When ringing is observed, the signal amplitude following the falling edge shall remain below $V_{\text{OUA}} \times V_1$. The falling edge is that part of the envelope $V$ where $V$ decreases from $V_4$ to $V_2$. See Table A.2 in Appendix A for the appropriate values of $V_{\text{OUA}}$.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.2.4 TA124.z00 Verifying the t2 Timing

This test verifies lower level timing during a Type A modulation.

**Test Code**

TA124.z00

**Reference**

This test refers to requirement 3.3.2.1.

**Test Positions**

Use Table 7-11 for the test positions during verification of the t2 timing:

<table>
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**Table 7-11—Test Positions of Test TA124.z00**

**Procedure**

Follow this procedure to verify the t2 timing:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 7-11.
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.
7. Set the Acquisition Device to capture 10 μs of the PCD signal centered upon one pause within the WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Identify the signal positive peak amplitude \( V_1 \).

11. Calculate \( V_2 \) as equal to \( 0.05 \times V_1 \) and place a Y-cursor (or its equivalent) to identify the corresponding level.

12. Place an X-cursor (or its equivalent) to identify the time where the PCD carrier envelope crosses \( V_2 \) for the last time preceding the first rising edge or after ringing if ringing occurs.

13. Place an X-cursor (or its equivalent) to identify the time where the PCD carrier envelope crosses \( V_2 \) for the first time as the carrier envelope increases.

14. Determine the timing \( t_2 \) when \( V \) decreases through \( V_2 \) to when \( V \) increases through \( V_2 \) as the difference between the times identified by the two X-cursors.

15. Repeat steps 8 to 14 for all points defined in Table 7-11.

**Acceptance Criteria**

\( V \) shall remain less than \( V_2 \) for a time \( t_2 \). The time interval \( t_2 \) shall conform to appropriate values shown in Table A.2 in Appendix A.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.2.5 TA125.z00 Verifying the \( t_3 \) and \( t_4 \) Timings

This test verifies the increase of \( V \) from \( V_2 \) to \( V_4 \) within a given time \( t_3 \) and from \( V_2 \) to \( V_3 \) within a given time \( t_4 \).

**Test Code**

TA125.z00

**Reference**

This test refers to requirement 3.3.2.1.

**Test Positions**

Use Table 7-12 for the test positions during verification of the increase of \( V \) from \( V_2 \) to \( V_3 \) within a given time \( t_4 \):

<table>
<thead>
<tr>
<th>Value for ( z )</th>
<th>Value for ( r )</th>
<th>Value for ( f )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

*Table 7-12—Test Positions of Test TA125.z00*

**Procedure**

Follow this procedure to verify the increase of \( V \) from \( V_2 \) to \( V_4 \) within a given time \( t_3 \) and the increase of \( V \) from \( V_2 \) to \( V_3 \) within a given time \( t_4 \):

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 7-12.
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.
7. Set the Acquisition Device to capture 10 μs of the PCD signal centered upon one pause within the WUPA command sent by the PCD.

8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.

10. Identify the signal positive peak amplitude \( V_1 \).

11. Calculate \( V_2 \) as equal to \( 0.05 \times V_1 \) and place a Y-cursor \( Y_1 \) at the corresponding level.

12. Calculate \( V_3 \) as equal to \( 0.6 \times V_1 \) and place a Y-cursor \( Y_2 \) at the corresponding level.

13. Calculate \( V_4 \) as equal to \( 0.9 \times V_1 \) and place a Y-cursor \( Y_3 \) at the corresponding level.

14. Place an X-cursor \( X_1 \) (or its equivalent) to identify the time where the PCD carrier envelope increases through \( V_2 \).

15. Place an X-cursor \( X_2 \) (or its equivalent) to identify the time where the PCD carrier envelope increases through \( V_3 \).

16. Place an X-cursor \( X_3 \) (or its equivalent) to identify the time where the PCD carrier envelope increases through \( V_4 \).

17. Determine the timing \( t_4 \) as the difference between the times identified by the \( X_1 \) and \( X_2 \) cursors.

18. Determine the timing \( t_3 \) as the difference between the times identified by the \( X_1 \) and \( X_3 \) cursors.

19. Repeat steps 8 to 18 for all points defined in Table 7-12.

**Acceptance Criteria**

\( V \) shall increase from \( V_2 \) to \( V_4 \) within a given time \( t_3 \). \( V \) shall increase from \( V_2 \) to \( V_3 \) within a given time \( t_4 \). The time intervals \( t_3 \) and \( t_4 \) shall conform to appropriate values shown in Table A.2 in Appendix A.

**Expected Results**

Results are recorded with one of two statements:

- Pass message

- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.2.6 TA127.z00 Verifying the Monotonic Increase from V2 to V4

This test verifies the monotonic increase of V from V2 to V4.

**Test Code**

TA127.z00

**Reference**

This test refers to requirement 3.3.2.1.

**Test Positions**

Use Table 7-13 for the test positions during verification of the monotonic increase of V from V2 to V4:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
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<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Table 7-13—Test Positions of Test TA127.z00**

**Procedure**

Follow this procedure to verify the monotonic increase of V from V2 to V4:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 7-13.
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.
7. Set the Acquisition Device to capture 10 μs of the signal the PCD signal centered upon one pause within the WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Identify the signal positive peak amplitude $V_1$.

11. Calculate $V_2$ as equal to $0.05 \times V_1$ and place a Y-cursor $Y_1$ at the corresponding level.

12. Calculate $V_4$ as equal to $0.9 \times V_1$ and place a Y-cursor $Y_2$ at the corresponding level.

13. Identify when the PCD carrier envelope increases through $V_2$.

14. Identify when the PCD carrier envelope increases through $V_4$.

15. Observe $V$ increasing from $V_2$ to $V_4$ on the PCD carrier envelope. If the carrier envelope increases continuously between $V_2$ and $V_4$, the increase is monotonic.

16. Repeat steps 8 to 15 for all points defined in Table 7-13.

**Acceptance Criteria**

$V$ shall increase monotonically from $V_2$ to $V_4$.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.2.7 TA128.z00 Verifying the Overshoot

This test verifies the overshoot immediately following the rising edge, which is that part of the envelope $V$, where $V$ increases from $V_2$ to $V_4$.

Test Code

TA128.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 7-14 for the test positions during verification of the overshoot immediately following the rising edge:

<table>
<thead>
<tr>
<th>Value for $z$</th>
<th>Value for $r$</th>
<th>Value for $f$</th>
</tr>
</thead>
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<tr>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 7-14—Test Positions of Test TA128.z00

Procedure

Follow this procedure to verify the overshoot immediately following the rising edge:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 7-14.
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.
7. Set the Acquisition Device to capture 10 μs of the signal the PCD signal centered upon one pause within the WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.

10. Identify the signal positive peak amplitude $V_1$.

11. Calculate $V_4$ as equal to $0.9 \times V_1$ and place a Y-cursor (or its equivalent) to identify the corresponding level.

12. Observe $V$ after that the envelope has increased through $V_4$.

13. Identify and measure (using cursors or their equivalent) the maximum and the minimum peak following the rising edge from $V_2$ to $V_4$.

14. Repeat steps 8 to 13 for all points defined in Table 7-14.

**Acceptance Criteria**

Overshoots immediately following the rising edge shall remain within $(1 \pm V_{OU,A}) \times V_1$. See Table A.2 in Appendix A for the value of $V_{OU,A}$.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.3 PICC to PCD Signal Interface for Type A Communications

This section presents the verifications applicable for Type A communications.

**Note**

The tests in this section should have their timings adjusted for the actual carrier frequency of the PCD under test.

7.8.3.1 TA131.zrf Verifying the Load Modulation $V_{S1,pp}$ at Minimum Positive Modulation

This test verifies if a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

**Test Code**

TA131.zrf

**Reference**

This test refers to requirement 3.4.5.1.

**Test Positions**

Use Table 7-15 for the test positions during verification that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

<table>
<thead>
<tr>
<th>Value for $z$</th>
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<td>2</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>9</td>
</tr>
</tbody>
</table>

**Table 7-15—Test Positions of Test TA131.zrf**
Procedure

Follow this procedure to verify that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum positive load modulation $V_{S1,pp}$. See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-15.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-15.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC applies minimum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.3.2 TA132.zrf Verifying the Load Modulation $V_{S2,pp}$ at Minimum Positive Modulation

This test verifies whether a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool.

Test Code

TA132.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 7-16 for the verification that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool:

<table>
<thead>
<tr>
<th>Value for $z$</th>
<th>Value for $r$</th>
<th>Value for $f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
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</tr>
<tr>
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<tr>
<td>3</td>
<td>2</td>
<td>9</td>
</tr>
<tr>
<td>4</td>
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<td>0</td>
</tr>
<tr>
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<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
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<td>4</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 7-16—Test Positions of Test TA132.zrf

Procedure

Follow this procedure to verify that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum positive load modulation \(V_{S2,pp}\). See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of \(V_{S2,pp}\).

5. Place the EMV – TEST PICC at the first position defined in Table 7-16.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-16.

**Acceptance Criteria**

The PCD shall function correctly when the EMV – TEST PICC, placed in a position \(z\) which is \(\geq 3\) cm in height in the positioning tool, applies minimum positive load modulation characteristics. All responses shall be observed.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.3.3 TA133.zrf Verifying the Load Modulation $V_{S1,pp}$ at Maximum Positive Modulation

This test verifies if a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

Test Code

TA133.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 7-17 for the test positions during verification that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool:

<table>
<thead>
<tr>
<th>Value for $z$</th>
<th>Value for $r$</th>
<th>Value for $f$</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
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<td>0</td>
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</tr>
<tr>
<td>0</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
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<td>0</td>
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<tr>
<td>2</td>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 7-17—Test Positions of Test TA133.zrf

Procedure

Follow this procedure to verify that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
2. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
3. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the
Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum positive load modulation $V_{S1,pp}$. See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-17.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with the each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-17.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool, applies maximum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.3.4 TA134.zrf Verifying the Load Modulation $V_{S2,pp}$ at Maximum Positive Modulation

This test verifies if a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool.

Test Code

TA134.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 7-18 for the test positions during verification of proper operation of a PCD when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool:

<table>
<thead>
<tr>
<th>Value for $z$</th>
<th>Value for $r$</th>
<th>Value for $f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
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<td>0</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
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<tr>
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</tr>
<tr>
<td>3</td>
<td>2</td>
<td>9</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
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</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 7-18—Test Positions of Test TA134.zrf

Procedure

Follow this procedure to verify proper operation of a PCD when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum positive load modulation \( V_{S2,pp} \). See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of \( V_{S2,pp} \).

5. Place the EMV – TEST PICC at the first position defined in Table 7-18.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with the each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-18.

**Acceptance Criteria**

The PCD shall function correctly when the EMV – TEST PICC, placed in a position \( z \) which is \( \geq 3 \) cm in height in the positioning tool, applies maximum positive load modulation characteristics. All responses shall be observed.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.3.5 TA135.zrf Verifying the Load Modulation $V_{S1,pp}$ at Minimum Negative Modulation

This test verifies if a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

**Test Code**

TA135.zrf

**Reference**

This test refers to requirement 3.4.5.1.

**Test Positions**

Use Table 7-19 for the test positions during verification that a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

<table>
<thead>
<tr>
<th>Value for $z$</th>
<th>Value for $r$</th>
<th>Value for $f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
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</tr>
<tr>
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<td>1</td>
<td>0</td>
</tr>
<tr>
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<tr>
<td>0</td>
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<td>0</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
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</tr>
<tr>
<td>2</td>
<td>2</td>
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<tr>
<td>2</td>
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<tr>
<td>2</td>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 7-19—Test Positions of Test TA135.zrf

**Procedure**

Follow this procedure to verify a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
   Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
   Connect the output J4 of the EMV – TEST CMR to the CH0 input of the
Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum negative load modulation $V_{S1,pp}$. See Chapter 7, section 7.3.2 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-19.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-19.

**Acceptance Criteria**

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool, applies minimum negative load modulation characteristics. All responses shall be observed.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.3.6 TA136.zrf Verifying the Load Modulation $V_{S2,pp}$ at Minimum Negative Modulation

This test verifies if a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool.

Test Code

TA136.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 7-20 for test positions during the verification that a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool.

<table>
<thead>
<tr>
<th>Value for $z$</th>
<th>Value for $r$</th>
<th>Value for $f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>3</td>
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<td>3</td>
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<td>6</td>
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<tr>
<td>3</td>
<td>2</td>
<td>9</td>
</tr>
<tr>
<td>4</td>
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<td>0</td>
</tr>
<tr>
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<td>1</td>
<td>0</td>
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<td>4</td>
<td>1</td>
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</tr>
<tr>
<td>4</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 7-20—Test Positions of Test TA136.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum negative load modulation $V_{s2pp}$. See Chapter 7, section 7.3.2 for details and Table B.1 in Appendix B for the value of $V_{s2pp}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-20.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-20.

**Acceptance Criteria**

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool, applies minimum negative load modulation characteristics. All responses shall be observed.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.3.7 TA137.zrf Verifying the Load Modulation $V_{S1,pp}$ at Maximum Negative Modulation

This test verifies if a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

**Test Code**

TA137.zrf

**Reference**

This test refers to requirement 3.4.5.1.

**Test Positions**

Use Table 7-21 for the test positions during verification that a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

<table>
<thead>
<tr>
<th>Value for $z$</th>
<th>Value for $r$</th>
<th>Value for $f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
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<tr>
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<td>1</td>
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<tr>
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<td>2</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>9</td>
</tr>
</tbody>
</table>

**Table 7-21—Test Positions of Test TA137.zrf**

**Procedure**

Follow this procedure to verify a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the
Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum negative load modulation $V_{S1,pp}$. See Chapter 7, section 7.3.2 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-21.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-21.

**Acceptance Criteria**

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool, applies maximum negative load modulation characteristics. All responses shall be observed.

**Expected Results**

Results are recorded with one of two statements:

- Pass message

- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.3.8 TA138.zrf Verifying the Load Modulation $V_{S2,pp}$ at Maximum Negative Modulation

This test verifies if a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool.

Test Code

TA138.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 7-22 for test positions during the verification that a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool.

<table>
<thead>
<tr>
<th>Value for $z$</th>
<th>Value for $r$</th>
<th>Value for $f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
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<tr>
<td>4</td>
<td>1</td>
<td>9</td>
</tr>
</tbody>
</table>

Table 7-22—Test Positions of Test TA138.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a maximum negative load modulation $V_{s2,pp}$. See Chapter 7, section 7.3.2 for details and Table B.1 in Appendix B for the value of $V_{s2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 7-22.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 7-22.

**Acceptance Criteria**

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool, applies maximum negative load modulation characteristics. All responses shall be observed.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
### 7.8.3.9 TA139.000 Verifying the FDT\textsubscript{A,\textsc{PICC}} tolerance

This test verifies if a PCD functions correctly when type A PICC responses occur at minimum and maximum values of the acceptable FDT\textsubscript{A,\textsc{PICC}} time window.

**Test Code**

TA139.000

**Reference**

This test refers to requirement 4.8.1.1.

**Procedure**

Follow this procedure to verify that a PCD functions correctly when type A PICC responses occur at minimum and maximum values of the acceptable FDT\textsubscript{A,\textsc{PICC}} time window.

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

3. Set up the EMV – TEST PICC to generate a nominal positive load modulation V\textsubscript{S1,pp}. See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of V\textsubscript{S1,pp}. 
4. Refer to Figure 7.13 to set-up the PICC Emulation Device FDT\textsubscript{APICC}:

![Block Diagram for the PICC Emulation Device FDT\textsubscript{APICC} Set-up]

\textbf{Figure 7.13—Block Diagram for the PICC Emulation Device FDT\textsubscript{APICC} Set-up}

5. Set the EMV – TEST CMR with the control software as shown in Table 7-23:

<table>
<thead>
<tr>
<th>Function</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>J8 (LETI)</td>
</tr>
<tr>
<td>Clock</td>
<td>CLK IN</td>
</tr>
<tr>
<td>Amplifier</td>
<td>Buffer</td>
</tr>
</tbody>
</table>

\textbf{Table 7-23—CMR Parameter Settings}

6. Place the EMV – TEST PICC at position \((z=0, r=0, \phi=0)\).

7. Display the TTA L1 - Analogue menu using the DTE.

8. Set the DTE in WUPA mode.

9. Set the Acquisition Device to capture 10 ms of signal at the start of the WUPA command.

10. Set the PICC Emulation Device to generate FDT\textsubscript{APICC,MIN} as required in Table C-2, without any correction.

11. Optimize the Acquisition Device settings for accurate measurement of type A waveform level and timing.

12. Send a correct ATQA answer.
13. Measure the FDT_{A,PICC} between the start of the WUPA last rising edge and the start of the PICC load modulation. Figure 7.14 shows the correct start cursor position, and Figure 7.15 shows the correct end cursor position.

Figure 7.14—Start Cursor Position for the FDT_{A,PICC} Measurement

Figure 7.15—End Cursor Position for the FDT_{A,PICC} Measurement

14. If the measured FDT_{A,PICC} is not the one required for the test, set the PICC Emulation Device to generate the required one.

Note

The setup of the FDT_{A,PICC,MIN} performed on the ATQA is enough to ensure that the next FDT_{A,PICC} values (UID, SAK for FDT_{A,PICC,MIN} and ATS Response to Select PPSE Command, etc. for FDT_{A,PICC,NOM}) should be correct if the FDT_{A,PICC,MIN} performed on the ATQA is correctly set up. There is no need to adjust the other FDT_{A,PICC} values in the frame trail.

15. Repeat steps 12 to 14 until the required value for FDT_{A,PICC} is reached.

16. Display the TTA L1 - Digital menu using the DTE.

17. Set the DTE in LOOPBACK mode.

18. Make the EMV – TEST PICC return the responses described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests using an FDT_{A,PICC} without any additional delay on all PICC responses.

19. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
20. Repeat steps 18 and 19 using an FDTA,PICC with an additional delay of 400 ns on all PICC responses.

You shall set the PICC Emulation Device to generate $FDT_{A,PICC,MIN}$ as required in Table C-2 without any correction on the first iteration, then with a 400 ns delay (Step 19).

Acceptance Criteria

The PCD shall function correctly when type A PICC responses occur at minimum and maximum values of the acceptable $FDT_{A,PICC}$ time window. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.4 Bit Level Coding Signal Interface for Type A Communications

This section presents the verifications applicable for Type A communications.

7.8.4.1 TA141.200 Verifying the PCD Transmitted Bit Rate

This test verifies the PCD to PICC bit rate during initialization.

Test Code

TA141.200

Reference

This test refers to requirement 4.2.1.1.

Procedure

Follow this procedure to verify the PCD to PICC bit rate during initialization:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

5. Place the EMV – TEST PICC at position (z=2, r=0, φ=0).

6. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.

7. Set the Acquisition Device to trigger to capture one WUPA command sent by the PCD.

8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.
Figure 7.16 shows the bit rate for the WUPA command:

![Figure 7.16—Bit Rate for the WUPA Command](image)

10. Place an X-cursor (or its equivalent) to identify the time when the PCD carrier envelope is at the start of the third pause within the WUPA command.

11. Place an X-cursor (or its equivalent) to identify the time when the PCD carrier envelope is at the identical point at the start of the sixth pause within the WUPA command.

12. Calculate the bit rate as $\frac{5}{\text{the difference between the times identified by the two X-cursors}}$.

**Acceptance Criteria**

The bit rate shall be between $f_c / 128 \pm 0.5\%$.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.4.2 TA142.200 Verifying the Bit Coding and De-synchronization PCD to PICC

This test verifies the PCD coding.

Test Code

TA142.200

Reference

This test refers to requirements 4.4.1.1 and 4.6.1.1.

Procedure

Follow this procedure to verify the PCD coding:

1. Confirm that the content of WUPA coded by the PUT is the value ‘52’ using EMV L1 digital tests.

2. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.

3. Display the TTA L1 - Analogue menu using the DTE.

4. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

5. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

6. Place the EMV – TEST PICC at position (z=2, r=0, φ=0).

7. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.

8. Set the Acquisition Device to trigger to capture one WUPA command sent by the PCD.

9. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

10. Launch the acquisition.

11. Place an X-cursor or its equivalent to identify the time when the PCD carrier envelope is at the start of the first pause within the WUPA. This cursor shall be referenced as X1.

12. Place an X-cursor or its equivalent to identify the time when the PCD carrier envelope is at the start of the second pause within the WUPA. This cursor shall be referenced as X2. The time between X1 and X2 is defined as the bit duration.

13. Identify the symbol between X1 and X2 using the following rules:
   a) if a low level occurs after a time of half a bit duration, identify the symbol as X.
   b) if no modulation occurs for a full bit duration, identify the symbol as Y.
c) if a low level occurs at the beginning of the bit duration, identify the symbol as Z.

d) if none of the previous cases has been identified, identify the symbol as an invalid symbol.

14. Complete Table 7-24 for the symbol you have identified.

15. Move the cursors X₁ and X₂ by the bit duration identified in step 12 to identify the Symbol over the next bit duration.

16. Repeat step 13 to 15 for all the other symbols in the sequence.

17. Compare the identified symbols with the expected ones. The sequence of expected symbols corresponds to a WUPA (0x52 Modified Miller coded with ASK 100% modulation).

<table>
<thead>
<tr>
<th>Identified Symbol</th>
<th>Expected Symbol</th>
<th>WUPA Bit Coding Correspondence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z</td>
<td>Start of Frame</td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td>End of Frame</td>
<td></td>
</tr>
</tbody>
</table>

Table 7-24—Symbols Identified

Acceptance Criteria

The PCD shall code a WUPA according to the sequence of expected symbols given in Table 7-24.

The symbols used shall be as follows:

- Symbol X: after a time of half the bit duration, a lower level occurs.
- Symbol Y: for the full bit duration, no modulation occurs.
- Symbol Z: at the beginning of the bit duration, a lower level occurs.
Figure 7.17 shows the WUPA bit coding:

![Waveform Graph 9](image)

### Figure 7.17—WUPA Bit Coding

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.4.3 TA143.200 Verifying the Bit Coding and De-synchronization PICC to PCD

This test verifies the PCD behavior when receiving a correct PICC answer.

Test Code

TA143.200

Reference

This test refers to requirements 4.4.2.2 and 4.6.1.3.

Procedure

Follow this procedure to verify the PCD behavior when receiving a correct PICC answer:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a nominal positive load modulation $V_{S1,pp}$. See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.

5. Place the EMV – TEST PICC at position ($z=2, r=0, \varphi=0$).

6. Make sure that the CARRIER is switched on and set the PCD under test in RATS mode.

7. Detect when the PCD sends a WUPA command.

8. Send a correct PICC ATQA answer with the content and timing as defined in Appendix C.

9. Observe if the PCD responds with the next command and confirm that the next command (AC CL1) is a valid command.

Acceptance Criteria

The PCD shall continue with the next command when receiving a correct PICC answer. This next command shall be a valid Type A command.

Expected Results

Results are recorded with one of two statements:

• Pass message

• Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.5 PCD to PICC Signal Interface for Type B Communications

This section presents the verifications applicable for Type B communications.

Figure 7.18 shows a typical PCD to PICC Type B modulation waveform. This waveform appears when the EMV – TEST PICC is positioned in the Operating Volume of the PCD.

![Figure 7.18—Typical PCD to PICC Type B Modulation Waveform](image)

The V (voltage) represents the envelope of the signal measured at the output of the pickup coil of the EMV – TEST PICC. If you are using asynchronous sampling, the envelope (V) is obtained by applying a moving average with a period of 1/fC on the magnitude of the complex Hilbert transform of the signal.

V1 is the initial value measured immediately before any modulation is applied by the PCD. V2 is the lower level. The modulation index (m_i), V3 and V4 are defined as follows:

\[ m_i = \frac{V_i - V_2}{V_1 + V_2} \]

\[ V_3 = V_1 - 0.1 \times (V_1 - V_2) \]

\[ V_4 = V_2 + 0.1 \times (V_1 - V_2) \]

**Note**

It is strongly recommended to perform these test cases using the same acquisitions to avoid any random behavior of the PCD under test.
7.8.5.1 TB121.z00 Verifying the Modulation Index

This test verifies the modulation index.

Test Code

TB121.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 7-25 for the test positions during verification of the modulation index:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 7-25—Test Positions of Test TB121.z00

Procedure

Follow this procedure to verify the modulation index:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

5. Place the EMV – TEST PICC in the first position defined in Table 7-25.

6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.

7. Set the Acquisition Device to capture 30 μs of signal with logic state changes.

8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude \( V_1 \).

11. Measure, using a cursor or its equivalent, the lower level amplitude \( V_2 \).

12. Calculate the modulation index \( m_i = \frac{V_1 - V_2}{V_1 + V_2} \).

13. Repeat steps 8 to 12 for all positions defined in Table 7-25.

**Acceptance Criteria**

The modulation index \( m_i \) of the signal shall be mod. Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for mod. Also use the procedure in Table 7-26 to determine the values to be used to calculate the modulation level.

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>The waveform has stable high and low levels. Where stable is defined as having more than 5% of the samples in the histogram bin identifying the high/low level when using the histogram method described in <em>IEEE Std 181-2003: IEEE Standard on Transitions, Pulses, and Related Waveforms</em> and using 256 bins for the upper/lower 40% region of the peak-peak range of the waveform.</td>
<td>Use the high and low levels identified by the histogram method to calculate the modulation level for comparison against both the maximum and minimum limit.</td>
</tr>
<tr>
<td>Waveform does not have stable high and low levels. Where stable is defined as above.</td>
<td>Use the maximum value of the unmodulated field as the high level and the minimum value of the modulated field as the low level to calculate the modulation level for comparison against maximum modulation index limit. Use the maximum value of the modulated field as the high level and the minimum value of the unmodulated field as the low level to calculate the modulation level for comparison against the minimum modulation index limit.</td>
</tr>
</tbody>
</table>

**Table 7-26—Procedure for determining values in calculations for TB121.z00**

When testing PCDs without a perfectly flat landing plane, refer to section 5.2.2. above and adjust the acceptance criteria according to the actual \( z \) distance used during testing. The distance is taken from the center of the EMV – Test PICC.

**Expected Results**

Results are recorded with one of two statements:
• Pass message

• Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.5.2 TB122.z00 Verifying the Fall Time

This test verifies the fall time.

Test Code

TB122.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 7-27 for the test positions during verification of the fall time for Type B communications:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 7-27—Test Positions of Test TB122.z00

Procedure

Follow this procedure to verify the fall time:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

5. Place the EMV – TEST PICC in the first position defined in Table 7-27.

6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.

7. Set the Acquisition Device to capture 30 μs of signal with logic state changes.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude \( V_1 \).

11. Measure, using a cursor or its equivalent, the lower level amplitude \( V_2 \).

12. Calculate \( V_3 = V_1 - 0.1 \times (V_1 - V_2) \) and place a Y-cursor (or its equivalent) \( Y_1 \) to identify the corresponding level.

13. Calculate \( V_4 = V_2 + 0.1 \times (V_1 - V_2) \) and place a Y-cursor (or its equivalent) \( Y_2 \) to identify the corresponding level.

14. Place an X-cursor (or its equivalent) \( X_1 \) at the timing corresponding to the first time that the voltage \( V \) crosses the \( Y_1 \) cursor level.

15. Place an X-cursor (or its equivalent) \( X_2 \) at the timing corresponding to the first time that the voltage \( V \) crosses the \( Y_2 \) cursor level.

16. Determine the fall time \( t_f \) as the difference between the timing indicated by \( X_2 \) and the timing indicated by \( X_1 \).

17. Repeat steps 8 to 16 for all positions defined in Table 7-27.

**Acceptance Criteria**

\( V \) shall decrease from \( V_3 \) to \( V_4 \) within a given time \( t_f \). Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for \( t_f \).

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.5.3 TB123.z00 Verifying the Rise Time

This test verifies the rise time.

Test Code

TB123.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 7-28 for the test positions during verification of the rise time:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 7-28—Test Positions of Test TB123.z00

Procedure

Follow this procedure to verify the rise time:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

5. Place the EMV – TEST PICC in the first position defined in Table 7-28.

6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.

7. Set the Acquisition Device to capture 30 μs of signal with logic state changes.

8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude \( V_1 \).

11. Measure, using a cursor or its equivalent, the lower level amplitude \( V_2 \).

12. Calculate \( V_3 = V_1 - 0.1 \times (V_1 - V_2) \) and place a Y-cursor (or its equivalent) \( Y_1 \) to identify the corresponding level.

13. Calculate \( V_4 = V_2 + 0.1 \times (V_1 - V_2) \) and place a Y-cursor (or its equivalent) \( Y_2 \) to identify the corresponding level.

14. Place an X-cursor (or its equivalent) \( X_1 \) at the timing corresponding to the second time the voltage \( V \) crosses the \( Y_1 \) cursor level.

15. Place an X-cursor (or its equivalent) \( X_2 \) at the timing corresponding to the second time the voltage \( V \) crosses the \( Y_2 \) cursor level.

16. Determine the rise time \( t_r \) as the difference between the timing indicated by \( X_1 \) and the timing indicated by \( X_2 \).

17. Repeat steps 8 to 16 for all positions defined in Table 7-28.

**Acceptance Criteria**

\( V \) shall increase from \( V_4 \) to \( V_3 \) within a given time \( t_r \). Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for \( t_r \).

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.5.4 TB124.z00 Verifying the Monotonic Rising Edge

This test verifies that the rising edge is monotonic.

Test Code

TB124.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 7-29 for the test positions during verification that the rising edge is monotonic:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 7-29—Test Positions of Test TB124.z00

Procedure

Follow this procedure to verify that the rising edge is monotonic:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 7-29.
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.
7. Set the Acquisition Device to capture 30 μs of signal with logic state changes.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude $V_1$.

11. Measure, using a cursor or its equivalent, the lower level amplitude $V_2$.

12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) $Y_1$ to identify the corresponding level.

13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) $Y_2$ to identify the corresponding level.

14. Observe $V$ increasing from $V_4$ to $V_3$. If the increase is continuous between $V_4$ and $V_3$, the increase is monotonic.

15. Repeat steps 8 to 14 for all points defined in Table 7-29.

Acceptance Criteria

The rising edge of the modulation shall be monotonic.

**Note**

If you are using asynchronous sampling, verify the monotonic parameter on the envelope ($V$) obtained by applying a moving average with a period of $1/f_C$ on the magnitude of the complex Hilbert transform of the signal. No deviation is permitted.

If you are using synchronous sampling, the edge could deviate from monotonic:

- Only strictly below $z=1$
- For two successive peaks (1 cycle maximum)
- Less than 8% of $(V_1 - V_2)$ between two peaks

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.5.5 TB125.z00 Verifying the Monotonic Falling Edge

This test verifies that the falling edge is monotonic.

Test Code

TB125.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 7-30 for the test positions during verification that the falling edge is monotonic:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 7-30—Test Positions of Test TB125.z00

Procedure

Follow this procedure to verify that the falling edge is monotonic:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

5. Place the EMV – TEST PICC at the first position defined in Table 7-30.

6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.

7. Set the Acquisition Device to capture 30 μs of signal with logic state changes.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude $V_1$.

11. Measure, using a cursor or its equivalent, the lower level amplitude $V_2$.

12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) $Y_1$ to identify the corresponding level.

13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) $Y_2$ to identify the corresponding level.

14. Observe $V$ decreasing from $V_3$ to $V_4$. If the decrease is continuous between $V_3$ to $V_4$, the decrease is monotonic.

15. Repeat steps 8 to 14 for all points defined in Table 7-30.

**Acceptance Criteria**

The falling edge of the modulation shall be monotonic.

---

**Note**

If you are using asynchronous sampling, verify the monotonic parameter on the envelope (V) obtained by applying a moving average with a period of $1/f_C$ on the magnitude of the complex Hilbert transform of the signal. No deviation is permitted.

If you are using synchronous sampling, the edge could deviate from monotonic:

- Only strictly below $z=1$
- For two successive peaks (1 cycle maximum)
- Less than 8% of $(V_1 - V_2)$ between two peaks

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.5.6. TB126.z00 Verifying Overshoots

This test verifies the overshoots.

Test Code

TB126.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 7-31 for the test positions during verification of the overshoots:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 7-31—Test Positions of Test TB126.z00

Procedure

Follow this procedure to verify the overshoots:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 7-31.
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.
7. Set the Acquisition Device to capture 30 μs of signal with logic state changes.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude $V_1$.

11. Measure, using a cursor or its equivalent, the lower level amplitude $V_2$.

12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.

13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.

14. Determine (using a cursor or its equivalent) the maximum peak following the falling edge from $V_3$ to $V_4$ and measure the overshoot.

15. Determine (using a cursor or its equivalent) the maximum peak following the rising edge from $V_4$ to $V_3$ and measure the overshoot.

16. Repeat steps 8 to 15 for all points defined in Table 7-31.

Acceptance Criteria

Overshoots immediately following the rising and falling edge shall be less than $V_{OU,B} \times (V_1 - V_2)$. Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for $V_{OU,B}$.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.5.7 TB127.z00 Verifying Undershoots

This test verifies the undershoots.

Test Code

TB127.z00

Reference

This test refers requirement 3.3.4.1.

Test Positions

Use Table 7-32 for the test positions during verification of the undershoots:

<table>
<thead>
<tr>
<th>Value for z</th>
<th>Value for r</th>
<th>Value for f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 7-32—Test Positions of Test TB127.z00

Procedure

Follow this procedure to verify the undershoots:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 7-32.
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.
7. Set the Acquisition Device to capture 30 μs of signal with logic state changes.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.
10. Measure, using a cursor or its equivalent, the upper level amplitude $V_1$.
11. Measure, using a cursor or its equivalent, the lower level amplitude $V_2$.
12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
14. Determine (using a cursor or its equivalent) the minimum peak following the falling edge from $V_3$ to $V_4$ and measure the undershoot.
15. Determine (using a cursor or its equivalent) the minimum peak following the rising edge from $V_4$ to $V_3$ and measure the undershoot.
16. Repeat steps 8 to 15 for all points defined in Table 7-32.

Acceptance Criteria

Undershoots immediately following the falling and rising edge shall be less than $V_{OUB} \times (V_1 - V_2)$. Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for $V_{OUB}$.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.6 PICC to PCD Signal Interface for Type B Communications

This section presents the verifications applicable for Type B communications.

**Note**

The tests in this section should have their timings adjusted for the actual carrier frequency of the PCD under test.

7.8.6.1 TB131.zrf Verifying the Load Modulation $V_{S1,pp}$ at Minimum Positive Modulation

This test verifies if a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

**Test Code**

TB131.zrf

**Reference**

This test refers to requirement 3.4.5.1.

**Test Positions**

Use Table 7-33 for the test positions during verification that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool:

<table>
<thead>
<tr>
<th>Value for $z$</th>
<th>Value for $r$</th>
<th>Value for $f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>3</td>
</tr>
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</tbody>
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*Table 7-33—Test Positions of Test TB131.zrf*
Procedure

Follow this procedure to verify that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is \( \leq 2 \) cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a minimum positive load modulation \( V_{ST,pp} \). See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of \( V_{ST,pp} \).
5. Place the EMV – TEST PICC at the first position defined in Table 7-33.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 7-33.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is \( \leq 2 \) cm in height in the positioning tool, applies minimum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.6.2 TB132.zrf Verifying the Load Modulation $V_{S2,pp}$ at Minimum Positive Modulation

This test verifies if a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool:

**Test Code**

TB132.zrf

**Reference**

This test refers to requirement 3.4.5.1.

**Test Positions**

Use Table 7-34 for the test positions during verification that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool.

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<td>6</td>
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<tr>
<td>4</td>
<td>1</td>
<td>9</td>
</tr>
</tbody>
</table>

*Table 7-34—Test Positions of Test TB132.zrf*

**Procedure**

Follow this procedure to verify that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum positive load modulation $V_{S2,pp}$. See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-34.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-34.

**Acceptance Criteria**

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool, applies minimum positive load modulation characteristics. All responses shall be observed.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.6.3 TB133.zrf Verifying the Load Modulation $V_{S1,pp}$ at Maximum Positive Modulation

This test verifies if a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

**Test Code**

TB133.zrf

**Reference**

This test refers to requirement 3.4.5.1.

**Test Positions**

Use Table 7-35 for the test positions during verification that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

<table>
<thead>
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</tr>
</tbody>
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Table 7-35—Test Positions of Test TB133.zrf
Procedure

Follow this procedure to verify that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool.

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum positive load modulation $V_{S1,pp}$. See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-35.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-35.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≤ 2 cm in height in the positioning tool, applies maximum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.6.4 TB134.zrf Verifying the Load Modulation $V_{S2.pp}$ at Maximum Positive Modulation

This test verifies if a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq$ 3 cm in height in the positioning tool.

**Test Code**

TB134.zrf

**Reference**

This test refers to requirement 3.4.5.1.

**Test Positions**

Use Table 7-36 for the test positions during verification that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq$ 3 cm in height in the positioning tool:

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</table>

*Table 7-36—Test Positions of Test TB134.zrf*

**Procedure**

Follow this procedure to verify that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq$ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a maximum positive load modulation $V_{S2,pp}$. See Chapter 7, section 7.3.1 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 7-36.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 7-36.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool, applies maximum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.6.5 TB135.zrf Verifying the Load Modulation $V_{S1,pp}$ at Minimum Negative Modulation

This test verifies if a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

**Test Code**

TB135.zrf

**Reference**

This test refers to requirement 3.4.5.1.

**Test Positions**

Use Table 7-37 for the test positions during verification that a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

<table>
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<th>Value for $z$</th>
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*Table 7-37—Test Positions of Test TB135.zrf*

**Procedure**

Follow this procedure to verify a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the
Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum negative load modulation $V_{S_{1,p}}$. See Chapter 7, section 7.3.2 for details and Table B.1 in Appendix B for the value of $V_{S_{1,p}}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-37.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-37.

**Acceptance Criteria**

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool, applies minimum negative load modulation characteristics. All responses shall be observed.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.6.6 TB136.zrf Verifying the Load Modulation $V_{S2,pp}$ at Minimum Negative Modulation

This test verifies if a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is ≥ 3 cm in height in the positioning tool.

Test Code

TB136.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 7-38 for the test positions during verification that a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is ≥ 3 cm in height in the positioning tool.

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Table 7-38—Test Positions of Test TB136.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is ≥ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a minimum negative load modulation $V_{S2pp}$. See Chapter 7, section 7.3.2 for details and Table B.1 in Appendix B for the value of $V_{S2pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 7-38.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 7-38.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool, applies minimum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.6.7 TB137.zrf Verifying the Load Modulation $V_{S1,pp}$ at Maximum Negative Modulation

This test verifies if a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

Test Code

TB137.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 7-39 for the test positions during verification that a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool.

<table>
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<th>Value for $z$</th>
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Table 7-39—Test Positions of Test TB137.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the
Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum negative load modulation $V_{S1\delta P}$. See Chapter 7, section 7.3.2 for details and Table B.1 in Appendix B for the value of $V_{S1\delta P}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-39.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-39.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\leq 2$ cm in height in the positioning tool, applies maximum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
**7.8.6.8 TB138.zrf Verifying the Load Modulation $V_{S2,pp}$ at Maximum Negative Modulation**

This test verifies if a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool.

**Test Code**

TB138.zrf

**Reference**

This test refers to requirement 3.4.5.1.

**Test Positions**

Use Table 7-40 for the test positions during verification that a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool.

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</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>9</td>
</tr>
</tbody>
</table>

*Table 7-40—Test Positions of Test TB138.zrf*

**Procedure**

Follow this procedure to verify a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum negative load modulation $V_{S2pp}$. See Chapter 7, section 7.3.2 for details and Table B.1 in Appendix B for the value of $V_{S2pp}$.

5. Place the EMV – TEST PICC at the first position defined in Table 7-40.

6. Set the DTE in LOOPBACK mode.

7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.

8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.

9. Repeat steps 7 to 8 for all points defined in Table 7-40.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position $z$ which is $\geq 3$ cm in height in the positioning tool, applies maximum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.7 Bit Level Coding Signal Interface for Type B Communications

This section presents the verifications applicable for Type B communications.

7.8.7.1 TB141.200 Verifying the PCD Transmitted Bit Rate

This test verifies the PCD to PICC bit rate during initialization.

Test Code

TB141.200

Reference

This test refers to requirement 4.2.1.1.

Procedure

Follow this procedure to verify the PCD to PICC bit rate during initialization:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

5. Place the EMV – TEST PICC at position \( z=2, r=0, \phi=0 \).

6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.

7. Set the Acquisition Device to capture one WUPB command sent by the PCD.

8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.
Figure 7.19 shows the bit rate for the WUPB command:

![Figure 7.19—Bit Rate for the WUPB Command]

10. Place an X-cursor (or its equivalent) to identify the falling edge when the PCD carrier envelope is at the beginning of the low level of the start bit of the second CRC byte (‘73’) within the WUPB command.

11. Place an X-cursor (or its equivalent) to identify the time when the PCD carrier envelope is at the equivalent point on the falling edge, at the start of a subsequent lower level within the WUPB command, where the two falling edges are 8 bit periods apart.

12. Calculate the bit rate as $\frac{8}{(\text{the difference between the times identified by the two X-cursors})}$.

**Acceptance Criteria**

The bit rate shall be between $f_c / 128 \pm 0.5\%$.

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.7.2 TB142.200 Verifying the Synchronization, Bit Coding and De-synchronization of PCD to PICC

This test verifies the PCD command coding.

Test Code
TB142.200

Reference
This test refers to requirements 4.3.2.1, 4.4.3.1, 4.5.1.1 and 4.6.2.1.

Procedure
Follow this procedure to verify the PCD command coding:

1. Confirm that the content of WUPB coded by the PUT is the value ‘05’ using EMV L1 digital tests.
2. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
3. Display the TTA L1 - Analogue menu using the DTE.
4. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
5. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
6. Place the EMV – TEST PICC at position (z=2, r=0, φ=0).
7. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.
8. Set the Acquisition Device to trigger to capture one WUPB command sent by the PCD.
9. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
10. Place an X-cursor or its equivalent to identify the time when the PCD carrier envelope is at the start of the first level change from high to low within the WUPB. This cursor shall be referenced as X1.
11. Place an X-cursor or its equivalent to identify the time - after X1 - when the PCD carrier envelope starts to change from low to high within the WUPB. This cursor shall be referenced as X2.
12. Measure the delay between X1 and X2. This duration is referenced as t_PCD,S,1.
13. Place X1 at the end of t_PCD,S,1 and place X2 to identify the time when the PCD carrier envelope starts to change from high to low after X1 within the WUPB.
14. Measure the delay between X1 and X2. This duration is referenced as \( t_{PCD,S,2} \).

15. Place X1 at the end \( t_{PCD,S,2} \) and place X2 at \( X1 + 1\text{etu} \), derived from the bit rate calculated in section 7.8.7.1 (TB141.200). The time between X1 and X2 is defined as the bit duration.

16. Identify the symbol between X1 and X2 as follows:
   a) If the carrier is low (modulation applied) for the full bit duration, identify the symbol as L.
   b) If the carrier is high (no modulation applied) for the full bit duration, identify the symbol as H.
   c) If none of the previous cases has been identified, identify as an invalid symbol.

17. Complete Table 7-41 for the symbol you have identified.

**Note**

If there is a difference between X2 and the start of the next bit - named as bit boundaries - do not take it into account, it shall be verified in section 7.8.7.5 (TB147.200). Also do not take into account the rising and falling edges, or overshoots and undershoots. These are verified in sections 7.8.5.2 to 7.8.5.7 (TB122.z00 to TB127.z00).

18. Move the cursors X1 and X2 by 1 etu to identify the symbol over the next bit duration.

19. Repeat steps 16 to 18 for all the other symbols in Table 7-41.

20. Compare the identified symbols with the expected ones. The sequence of expected symbols corresponds to the first byte of the WUPB (0x05 NRZ-L coded with ASK 10% modulation).

21. Place X1 at the start of the falling edge of the first start bit of the PCD command and place X2 at the start of the falling edge of the start bit of the second character of the PCD command.

22. Measure \( EGT_{PCD} = (X2 - X1 - 1280/fC) \).

23. Place X1 at the start of the falling edge of the last start bit of the PCD command and place X2 at the start of the EoS falling edge.

24. Measure \( EGT_{PCD,EoS} = (X2 - X1 - 1280/fC) \).

25. Place X1 at the start of the EoS rising edge.

26. Measure the delay between X2 and X1. This duration is referenced as \( t_{PCD,E} \).
<table>
<thead>
<tr>
<th>Identified Symbol</th>
<th>Expected Symbol</th>
<th>First WUPB Bit Coding Correspondence</th>
</tr>
</thead>
<tbody>
<tr>
<td>L.</td>
<td>Start Bit</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>L.</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>L.</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>L.</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>L.</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>L.</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>H.</td>
<td>Stop Bit</td>
<td></td>
</tr>
</tbody>
</table>

Table 7-41—Symbols Identified

Acceptance Criteria

The time between two consecutive characters sent by the PCD to the PICC shall be EGT_{PCD}. Refer to Table A.4 in Appendix A, Sequences and Frames for the applicable range of values for EGT_{PCD}.

The PCD shall code Start of Sequence (SoS) as follows:

- t_{PCD,S,1} with carrier low applied
- t_{PCD,S,2} with carrier high (no modulation applied)

The PCD shall code End of Sequence (EoS) as follows:

- A time t_{PCD,E} with carrier low (modulation applied) followed by a transition to carrier high.
- The EoS shall come immediately after the last bit of the last data character (i.e. EGT_{PCD,EoS} = 0).

Refer to Table A.4 in Appendix A, Signal Interface for Type B for the applicable range of values for t_{PCD,S,1}, t_{PCD,S,2} and t_{PCD,E}. Figure 7.20 shows an example of correct bit coding of the WUPB command.

Figure 7.20—WUPB Bit Coding
The PCD shall code the first byte of WUPB command according to the sequence of expected symbols given in Table 7-41. Figure 7.21 shows an example of correct coding of the first byte of WUPB command.

The symbols used shall be as follows:

- Symbol H: the carrier is high for the full bit duration.
- Symbol L: the carrier is low for the full bit duration.

![Figure 7.21—First Byte of WUPB Command Coding](image)

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.7.3 TB145.200 Verifying the Maximum Limit De-synchronization PICC to PCD (tFSOFF, MAX)

This test verifies the PCD behavior when receiving a PICC answer with a maximum limit de-synchronization parameter.

**Test Code**

TB145.200

**Reference**

This test refers to requirement 4.6.2.5.

**Procedure**

Follow this procedure to verify the PCD behavior when receiving a PICC answer with a maximum limit de-synchronization parameter:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a nominal positive load modulation VSLPP. See Chapter 7, section 7.3.1 for details and Appendix B for the value of for VSLPP.
5. Place the EMV – TEST PICC at position (z=2, r=0, φ=0).
6. Make sure that the CARRIER is switched on and set the PCD under test in ATTRIB mode.
7. Detect when the PCD sends a WUPB command.
8. Send a PICC answer ATQB with correct format and timings as defined in Appendix C with a maximum limit tFSOFF value of 272/fc.
9. Observe if the PCD continues with the next command (ATTRIB).

**Acceptance Criteria**

The PCD shall be capable of supporting a PICC that maintains the subcarrier on for a time tFSOFF.

The PCD shall continue with the next command when receiving a correct ATQB with a maximum limit tFSOFF of 272/fc.
Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.7.4 TB146.200 Verifying the Synchronization, Bit Coding and De-synchronization of PICC to PCD

This test verifies the PCD understanding of a correct PICC answer.

Test Code

TB146.200

Reference

This test refers to requirement 4.3.2.5, 4.4.4.1, 4.4.4.3 and 4.6.2.3.

Procedure

Follow this procedure to verify the PCD understanding of a correct PICC answer:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a nominal positive load modulation VS1,pp. See Chapter 7, section 7.3.1 for details and Appendix B for the value of VS1,pp.

5. Place the EMV – TEST PICC at position (z=2, r=0, φ=0).

6. Make sure that the CARRIER is switched on and set the PCD under test in ATTRIB mode.

7. Detect when the PCD sends a WUPB command.

8. Send a correct PICC ATQB answer as defined in Appendix C.

9. Observe if the PCD continues with the next command (ATTRIB).

Acceptance Criteria

The PCD shall continue with the next command when receiving a correct PICC answer.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.7.5 TB147.200 Verifying the Bit Boundaries with Type B Communications

This test verifies the PCD bit boundaries.

Test Code

TB147.200

Reference

This test refers to requirement 4.5.1.3.

Procedure

Follow this procedure to verify the PCD bit boundaries:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.

3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.

4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).

5. Place the EMV – TEST PICC at position (z=2, r=0, φ=0).

6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.

7. Set the Acquisition Device to capture one WUPB command sent by the PCD

8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.

10. Identify and select the first character within the WUPB command.
11. Figure 7.22 shows the bit boundaries:

![Figure 7.22—Bit Boundaries](image)

12. Place an X-cursor (or its equivalent) at the start of the falling edge of the first start bit of the WUPB command.

13. Place an X-cursor (or its equivalent) at the start of the first rising edge of the character.

14. Determine the timing as the difference between the times identified by the two X-cursors.

15. Repeat steps 13 to 14 to determine the intervals between the start of the start bit and the start of all edges of the selected character.

16. Repeat steps 12 to 15 for all characters of the WUPB command.

**Acceptance Criteria**

The PCD shall apply bit boundaries within a character that are between $(n \text{etu} - 8/fC)$ and $(n \text{etu} + 8/fC)$, where $n$ is the number of bit boundaries after the start bit falling edge ($1 \leq n \leq 9$).

**Expected Results**

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
7.8.7.6 TB148.200 Verifying the Minimum Limit
De-synchronization PICC to PCD \((t_{\text{FSOFF},\text{MIN}})\)

This test verifies the PCD behavior when receiving a PICC answer with a minimum limit de-synchronization parameter.

Test Code

TB148.200

Reference

This test refers to requirement 4.6.2.5.

Procedure

Follow this procedure to verify the PCD behavior when receiving a PICC answer with a minimum limit de-synchronization parameter:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a nominal positive load modulation \(V_{S1,pp}\). See Chapter 7, section 7.3.1 for details and Appendix B for the value of for \(V_{S1,pp}\).
5. Place the EMV – TEST PICC at position \((z=2, r=0, \phi=0)\).
6. Make sure that the CARRIER is switched on and set the PCD under test in ATTRIB mode.
7. Detect when the PCD sends a WUPB command.
8. Send a PICC answer ATQB with correct format and timings as defined in Appendix C with a minimum limit \(t_{\text{FSOFF}}\) value of \(0 / f_{C}\).

\[\text{Note}\]

If \(t_{\text{FSOFF}} = 0\), it means that the subcarrier is turned off at the time of the phase transition from \(\Phi_{0+180^\circ}\) to \(\Phi_0\), as a result the stopping of the subcarrier represents the end of the EoS.

9. Observe if the PCD continues with the next command (ATTRIB).
Acceptance Criteria

The PCD shall be capable of supporting a PICC that maintains the subcarrier on for a time $t_{\text{FSOFF}}$.

The PCD shall continue with the next command when receiving a correct ATQB with a minimum limit $t_{\text{FSOFF}}$ of $0/f_c$.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.
PCD Acceptance Criteria

This appendix provides values for acceptance criteria used during testing of a PCD.

A.1 Power and Parameters ...................................................................................................... A-1
A.1 Power and Parameters

Note

All the values in the tables of this appendix are based on those found in the EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification.

Table A.1 shows the RF parameters to measure on the unmodulated PCD under test carrier and associated values:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Transfer PCD → PICC</td>
<td>$V_{OV} (0 \leq z \leq 2)$</td>
<td>3.10 – 0.05z</td>
<td></td>
<td>8.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{OV} (2 \leq z \leq 4)$</td>
<td>3.45 – 0.225z</td>
<td></td>
<td>8.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$\Delta V_{SENSE,MAX}$</td>
<td>0</td>
<td></td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{OV,RESET}$</td>
<td>0</td>
<td></td>
<td>3.5</td>
<td>mV RMS</td>
</tr>
<tr>
<td></td>
<td>$V_{OV,POWEROFF}$</td>
<td>0</td>
<td></td>
<td>3.5</td>
<td>mV RMS</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>$f_c$</td>
<td>13.553</td>
<td>13.560</td>
<td>13.567</td>
<td>MHz</td>
</tr>
</tbody>
</table>

Table A.1—RF Power

Table A.2 shows the parameters to measure on the signal interface for Type A communications:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type A</td>
<td>$t_1$</td>
<td>2.06</td>
<td></td>
<td>2.99</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_2$</td>
<td>0.52</td>
<td></td>
<td>$t_1$</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_3$</td>
<td>0</td>
<td></td>
<td>1.18</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_4$</td>
<td>0</td>
<td></td>
<td>minimum (0.44, $t_3 / 1.5$)</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_5$</td>
<td>0</td>
<td></td>
<td>0.50</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$V_{OCL,A}$</td>
<td>0</td>
<td></td>
<td>0.10</td>
<td>-</td>
</tr>
</tbody>
</table>

Table A.2—Signal Interface for Type A
Table A.3 shows the parameters to measure on the signal interface for Type B communications:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCD → PICC modulation</td>
<td>mod_m</td>
<td>9.0+0.25z</td>
<td>15.0-0.25z</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>t_r</td>
<td>0</td>
<td></td>
<td>1.18</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>t_r</td>
<td>0</td>
<td></td>
<td>1.18</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>V_OU,B</td>
<td>0</td>
<td></td>
<td>0.1</td>
<td>-</td>
</tr>
</tbody>
</table>

Table A.3—Signal Interface for Type B

Table A.4 shows the parameters which are measured in the Chapter 7 tests relative to the Sequences and Frames section of the EMV Contactless specification:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type B</td>
<td>t_PCD,S,1</td>
<td>1280</td>
<td>1416</td>
<td>1/f_C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>t_PCD,S,2</td>
<td>248</td>
<td>392</td>
<td>1/f_C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>t_PCD,S,E</td>
<td>1280</td>
<td>1416</td>
<td>1/f_C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EGT_PCD</td>
<td>0</td>
<td>752</td>
<td>1/f_C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EGT_PCD,EOS</td>
<td></td>
<td>0</td>
<td>1/f_C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FWT_ATQB</td>
<td>7680</td>
<td></td>
<td>1/f_C</td>
<td></td>
</tr>
</tbody>
</table>

Table A.4—Sequences and Frames

Table A.5 shows the parameters which are measured in the Chapter 7 tests relative to the PCD processing section of the EMV Contactless specification:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>t_RESET</td>
<td>5.1</td>
<td>10</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Power-off</td>
<td>t_POWEROFF</td>
<td>15</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

Table A.5—PCD processing
Set-up Values for EMV Test Equipment

This appendix shows the test conditions used during testing of a PCD.

B.1 Load Modulation Parameters .......................................................... B-1
### B.1 Load Modulation Parameters

Table B.1 shows the load modulation amplitude parameters for EMV – TEST PICC tuning when testing the PCD for receptivity.

<table>
<thead>
<tr>
<th>Topic</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCD Nominal Power</td>
<td>$V_{N,ON}$</td>
<td></td>
<td>5.53</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Load Modulation</td>
<td>$V_{S1,PP}$</td>
<td>5.5</td>
<td>20</td>
<td>85</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$V_{S2,PP}$</td>
<td>3.5</td>
<td>20</td>
<td>40</td>
<td>mV</td>
</tr>
</tbody>
</table>

*Table B.1—Load Modulation Parameters*
C

PICC Emulation: Frame Trail

This appendix contains details on frame trails used during testing of a PCD. Frame trails show the sequence of command events from a PCD and related PICC responses for testing the PCD receptivity.

C.1 Frame Trail for Type A PCD Tests..............................................................C-1
C.2 FDT_A,PICC ..................................................................................................C-3
C.3 Frame Trail for Type B PCD Tests..............................................................C-4
C.4 FDT_B,PICC ..................................................................................................C-6
   C.4.1 PICC Start of Sequence ........................................................................C-6
   C.4.2 PCD Start of Sequence ........................................................................C-6
# C.1 Frame Trail for Type A PCD Tests

Table C.1 shows the frame trail for Type A PCD tests:

<table>
<thead>
<tr>
<th>Step</th>
<th>Exchanges</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCD \‘52’ (short frame) \ PICC</td>
<td>WUPA during polling</td>
</tr>
<tr>
<td>2</td>
<td>PCD \‘08 03’ (no CRC_A) sent using the delay FDT_APICC_MIN \ PICC</td>
<td>ATQA</td>
</tr>
<tr>
<td>3</td>
<td>PCD \‘50 00’ \ PICC</td>
<td>HLTA</td>
</tr>
<tr>
<td>4</td>
<td>PCD \‘05 00 08’ (Type B frame) \ PICC</td>
<td>WUPB</td>
</tr>
<tr>
<td>o1</td>
<td>PCD</td>
<td>The PCD is allowed to support other technologies than EMV CL Type A and B. These optional commands are disregarded by the test tool</td>
</tr>
<tr>
<td>o2</td>
<td>PCD II</td>
<td>If the PCD has sent at least one command for another technology than EMV CL Type A and B at step o1, then it shall perform a PICC Reset</td>
</tr>
<tr>
<td>5</td>
<td>PCD \‘52’ (short frame) \ PICC</td>
<td>WUPA</td>
</tr>
<tr>
<td>6</td>
<td>PCD \‘08 03’ (no CRC_A) sent using the delay FDT_APICC_MIN \ PICC</td>
<td>ATQA</td>
</tr>
<tr>
<td>7</td>
<td>PCD \‘93 20’ (no CRC_A) \ PICC</td>
<td>ANTI-COLLISION CL1</td>
</tr>
<tr>
<td>8</td>
<td>PCD \‘27 E9 3B 11’ + ‘E4’ (no CRC_A) sent using the delay FDT_APICC_MIN \ PICC</td>
<td>UID</td>
</tr>
<tr>
<td>9</td>
<td>PCD \‘93 70’ + ‘27 E9 3B 11’ + ‘E4’ \ PICC</td>
<td>SEL1 + UID CL1 + BCC</td>
</tr>
<tr>
<td>10</td>
<td>PCD \‘20’ sent using the delay FDT_APICC_MIN \ PICC</td>
<td>SAK</td>
</tr>
<tr>
<td>11</td>
<td>PCD \‘E0 80’ \ PICC</td>
<td>RATS</td>
</tr>
<tr>
<td>12</td>
<td>PCD \‘05 72 80 40 02’ sent using the delay FDT_APICC_NOM \ PICC</td>
<td>ATS</td>
</tr>
<tr>
<td>13</td>
<td>PCD I(0)0 [‘00 A4 04 00 0E’ + ‘2PAY.SYS.DDF01’ + ‘00’] \ PICC</td>
<td>Select PPSE Command</td>
</tr>
<tr>
<td>14</td>
<td>PCD I(0)0 [‘00 A4 04 00 0C’ + ‘01 02 … 0C’ + ‘00’ + ‘90 00’] sent using the delay FDT_APICC_NOM \ PICC</td>
<td>Correct response frame</td>
</tr>
<tr>
<td>15</td>
<td>PCD I(0)0 [‘00 A4 04 00 0C’ + ‘01 02 … 0C’ + ‘00’] \ PICC</td>
<td>Loop-back</td>
</tr>
<tr>
<td>16</td>
<td>PCD I(0)1 [‘EOT Command’ + ‘90 00’] sent using the delay FDT_APICC_NOM \ PICC</td>
<td>End of Test command</td>
</tr>
<tr>
<td>17</td>
<td>PCD II The PUT performs a PICC Reset (i.e. stops sending the carrier) \ PICC</td>
<td>PICC Reset</td>
</tr>
</tbody>
</table>
Table C.1—Frame Trail for Type A PCD Tests

Unless specified otherwise in the Test Cases, the Testing Laboratory shall use the values from Table C.2 during the tests:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PICC</th>
<th>Unit</th>
</tr>
</thead>
</table>
| FDT\textsubscript{A,PICC,MIN} | 1236 if last logic state 1  
1172 if last logic state is 0 | 1/f\textsubscript{C} |
| FDT\textsubscript{A,PICC,NOM} | 3156 if last logic state 1  
3092 if last logic state is 0 | 1/f\textsubscript{C} |
| Bit rate   | f\textsubscript{C} /128 | bps |

Table C.2—Parameter Values

Note: Unless specified in the test case, the EOT Command shall be set to “Removal procedure”.

Table C.1—Frame Trail for Type A PCD Tests

<table>
<thead>
<tr>
<th>Step</th>
<th>Exchanges</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>PUT ▶ ‘52’ (short frame) ▶ PICC</td>
<td>WUPA to poll for the PICC</td>
</tr>
<tr>
<td>19</td>
<td>PUT ▶ ‘52’ (short frame) ▶ PICC</td>
<td>WUPA to poll for the PICC</td>
</tr>
<tr>
<td>20</td>
<td>PUT ▶ ‘52’ (short frame) ▶ PICC</td>
<td>WUPA to poll for the PICC</td>
</tr>
</tbody>
</table>
C.2 FDT\textsubscript{A,PICC}

FDT\textsubscript{A,PICC} is a measurement starting from the rising edge of the last lower level of the PCD command to the start of the SoF of the PICC response.

The FDT\textsubscript{A,PICC} depends on the logic state of the last data bit transmitted by the PCD before the EoF.

\textbf{Note}

The Contactless Specification prohibits FDT\textsubscript{A,PICC} timing that falls below the nominal values in Table C.2. Unless specified otherwise in the test procedure, the laboratory shall increase the FDT\textsubscript{A,PICC} timing value used by an amount equal to half the FDT\textsubscript{A,PICC} time window.

Figure C.1 shows the timing diagram for FDT\textsubscript{A,PICC} measurement:

![Timing Diagram for FDT\textsubscript{A,PICC}](image)

\textbf{Note}

When establishing measurement points with a cursor (or its equivalent), unless otherwise stated in the test procedure, always use the reference points as specified in Appendix E. Do this consistently to maintain measurement accuracy.
### C.3 Frame Trail for Type B PCD Tests

Table C.3 shows the frame trail for Type B PCD tests:

<table>
<thead>
<tr>
<th>Step</th>
<th>Exchanges</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCD '05 00 08'</td>
<td>PCC WUPB during polling</td>
</tr>
<tr>
<td>2</td>
<td>PCD '50' + '46 B5 C7 A0' + '00 00 00 00' + '00 21 81' sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC ATQB</td>
</tr>
<tr>
<td>3</td>
<td>PCD '52' (Type A short frame)</td>
<td>PCC WUPA</td>
</tr>
<tr>
<td>o1</td>
<td>PCD The PCD is allowed to support other technologies than EMV CL Type A and B. These optional commands are disregarded by the test tool</td>
<td>PCC Optional polling for other technologies than EMV Contactless Type A and B</td>
</tr>
<tr>
<td>o2</td>
<td>PCD If the PCD has sent at least one command for another technology than EMV CL Type A and B at step o1, then it shall perform a PICC Reset</td>
<td>PCC Optional PICC Reset</td>
</tr>
<tr>
<td>4</td>
<td>PCD '05 00 08'</td>
<td>PCC WUPB</td>
</tr>
<tr>
<td>5</td>
<td>PCD '50' + '46 B5 C7 A0' + '00 00 00 00' + '00 21 81' sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC ATQB</td>
</tr>
<tr>
<td>6</td>
<td>PCD '1D' + '46 B5 C7 A0' + '00 08 01 00'</td>
<td>PCC ATTRIB</td>
</tr>
<tr>
<td>7</td>
<td>PCD '00' sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC ATTRIB Response</td>
</tr>
<tr>
<td>8</td>
<td>PCD I(0)0 ['00 A4 04 00 0E' + &quot;2PAY.SYS.DDF01&quot; + '00']</td>
<td>PCC Select PPSE Command</td>
</tr>
<tr>
<td>9</td>
<td>PCD I(0)1 ['00 A4 04 00 0C' + '01 02 ... 0C' + '00' + '90 00'] sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC Correct response frame</td>
</tr>
<tr>
<td>10</td>
<td>PCD I(0)j ['00 A4 04 00 0C' + '01 02 ... 0C' + '00']</td>
<td>PCC Loop-back</td>
</tr>
<tr>
<td>11</td>
<td>PCD I(0)j ['EOT Command&quot; + '90 00'] sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC End of Test command</td>
</tr>
<tr>
<td>12</td>
<td>PCD II The PUT performs a PICC Reset (i.e. stops sending the carrier)</td>
<td>PCC PICC Reset</td>
</tr>
<tr>
<td>13</td>
<td>PUT '05 00 08'</td>
<td>PCC WUPB to poll for the PICC</td>
</tr>
<tr>
<td>14</td>
<td>PUT '05 00 08'</td>
<td>PCC WUPB to poll for the PICC</td>
</tr>
<tr>
<td>15</td>
<td>PUT '05 00 08'</td>
<td>PCC WUPB to poll for the PICC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Step</th>
<th>Exchanges</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCD '05 00 08'</td>
<td>PCC WUPB during polling</td>
</tr>
<tr>
<td>2</td>
<td>PCD '50' + '46 B5 C7 A0' + '00 00 00 00' + '00 21 81' sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC ATQB</td>
</tr>
<tr>
<td>3</td>
<td>PCD '52' (Type A short frame)</td>
<td>PCC WUPA</td>
</tr>
<tr>
<td>o1</td>
<td>PCD The PCD is allowed to support other technologies than EMV CL Type A and B. These optional commands are disregarded by the test tool</td>
<td>PCC Optional polling for other technologies than EMV Contactless Type A and B</td>
</tr>
<tr>
<td>o2</td>
<td>PCD If the PCD has sent at least one command for another technology than EMV CL Type A and B at step o1, then it shall perform a PICC Reset</td>
<td>PCC Optional PICC Reset</td>
</tr>
<tr>
<td>4</td>
<td>PCD '05 00 08'</td>
<td>PCC WUPB</td>
</tr>
<tr>
<td>5</td>
<td>PCD '50' + '46 B5 C7 A0' + '00 00 00 00' + '00 21 81' sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC ATQB</td>
</tr>
<tr>
<td>6</td>
<td>PCD '1D' + '46 B5 C7 A0' + '00 08 01 00'</td>
<td>PCC ATTRIB</td>
</tr>
<tr>
<td>7</td>
<td>PCD '00' sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC ATTRIB Response</td>
</tr>
<tr>
<td>8</td>
<td>PCD I(0)0 ['00 A4 04 00 0E' + &quot;2PAY.SYS.DDF01&quot; + '00']</td>
<td>PCC Select PPSE Command</td>
</tr>
<tr>
<td>9</td>
<td>PCD I(0)1 ['00 A4 04 00 0C' + '01 02 ... 0C' + '00' + '90 00'] sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC Correct response frame</td>
</tr>
<tr>
<td>10</td>
<td>PCD I(0)j ['00 A4 04 00 0C' + '01 02 ... 0C' + '00']</td>
<td>PCC Loop-back</td>
</tr>
<tr>
<td>11</td>
<td>PCD I(0)j ['EOT Command&quot; + '90 00'] sent using the delay FDT&lt;sub&gt;PICC,NOM&lt;/sub&gt;</td>
<td>PCC End of Test command</td>
</tr>
<tr>
<td>12</td>
<td>PCD II The PUT performs a PICC Reset (i.e. stops sending the carrier)</td>
<td>PCC PICC Reset</td>
</tr>
<tr>
<td>13</td>
<td>PUT '05 00 08'</td>
<td>PCC WUPB to poll for the PICC</td>
</tr>
<tr>
<td>14</td>
<td>PUT '05 00 08'</td>
<td>PCC WUPB to poll for the PICC</td>
</tr>
<tr>
<td>15</td>
<td>PUT '05 00 08'</td>
<td>PCC WUPB to poll for the PICC</td>
</tr>
</tbody>
</table>
Unless specified otherwise in the Test Cases, the Testing Laboratory shall use the values from Table C.4 during the tests:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PICC</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDT\textsubscript{R,PICC,NOM}</td>
<td>3072</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>TR0</td>
<td>1536</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>TR1</td>
<td>1536</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>Bit rate</td>
<td>\textit{f}_C / 128</td>
<td>bps</td>
</tr>
<tr>
<td>t\textsubscript{R0,A,1}</td>
<td>1344</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>t\textsubscript{R0,A,2}</td>
<td>320</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>t\textsubscript{R0,E}</td>
<td>1344</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>t\textsubscript{SOFF}</td>
<td>8</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>EGT\textsubscript{P}</td>
<td>0</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>EGT\textsubscript{P,E}</td>
<td>272</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>EGT\textsubscript{P,E3,S}</td>
<td>0</td>
<td>1/\textit{f}_C</td>
</tr>
<tr>
<td>EGT\textsubscript{P,E3,S,MAX}</td>
<td>272</td>
<td>1/\textit{f}_C</td>
</tr>
</tbody>
</table>

Table C.4—Parameter Values

Note

Unless specified in the test case, the EOT Command shall be set to “Removal procedure”.
C.4 FDT\textsubscript{B,PICC}

For Type B communications, FDT\textsubscript{B,PICC} measurement starts at the end of the EoS of the PCD command and goes to the beginning of the SoS of the PICC response.

\[ \text{FDT}_{\text{B,PICC}} = \text{TR0} + \text{TR1} \]

C.4.1 PICC Start of Sequence

Figure C.2 shows the timing diagram between the end of a command sent to a PICC and the beginning of the PICC sequence response:

\[ \text{Figure C.2—PICC Start of Sequence} \]

\begin{itemize}
  \item Note
    When establishing measurement points with a cursor (or its equivalent), unless otherwise stated in the test procedure, always use the reference points as specified in Appendix E. Do this consistently to maintain measurement accuracy.
\end{itemize}

C.4.2 PCD Start of Sequence

Figure C.3 shows the timing diagram between the end of a PICC response and the beginning of a PCD command sequence:

\[ \text{Figure C.3—PCD Start of Sequence} \]
Note

When establishing measurement points with a cursor (or its equivalent), unless otherwise stated in the test procedure, always use the reference points as specified in Appendix E. Do this consistently to maintain measurement accuracy.
Reference Implementation

This appendix contains a specific Test Bench implementation using the peak sampling method. This implementation was used to perform the Test Cases in Chapter 7.

D.1 Reference Implementation Using Peak Sampling ....................................................... D-1
  D.1.1 Set Up of the EMV TEST PICC........................................................................... D-2
  D.1.2 Implementation Set-up Overview ....................................................................... D-4
  D.1.3 Test Bench for the PCD Test ............................................................................. D-5
  D.1.4 Implementation Set-up Overview ....................................................................... D-7
D.1 Reference Implementation Using Peak Sampling

The implementation defined in this appendix was used during the development of the Test cases described in this document. Other implementations are possible but all test functionalities must be correctly implemented according to specifications.

A step by step procedure for cabling and a functional overview accompanies each connectivity diagram. Refer to Chapter 4 for more information on the requirements with respect to the reference implementation.

Note

For all connections in the reference implementation, the standard cable is a high quality coaxial cable, such as RG-316, terminated by SMA connectors. The cable ends are then fitted with appropriate adaptors for the connections to be made. However, adaptors are not shown in the connectivity diagrams.

Note

Cables connected to Test Bench equipment shall be as short as possible, ideally less than 50 cm. However, cables connected to computers and power supplies may have a length of up to 100 cm. This allows physical separation of the equipment to minimize coupling of electromagnetic disturbances to sensitive components of the Test Bench.
D.1.1 Set Up of the EMV TEST PICC

Follow this procedure to set up the EMV – TEST PICC for PCD testing:

1. Refer to the connectivity diagram in Figure D.1:

   ![Connectivity Diagram](image)

   The length of each cable shall not exceed 50 cm.
   Note 1: Probe can be passive or active, >1 MΩ, <15 pF.
   The DSO input impedance shall match the probe impedance.
   Note 2: J9 must be terminated by a 50 Ω load at all times.

   **Figure D.1—Connectivity Diagram to Set up the EMV – TEST PICC for PCD Testing**

2. Connect a cable to the Out 1 connector of the PICC Coding Generator.
3. Connect the other end of the cable to the In connector of the Load Modulation Adjustment.
4. Connect a cable to the Out connector of the Load Modulation Adjustment.
5. Connect the other end of the cable to the input J2 connector of the EMV – TEST PICC.
6. Connect a probe to CH0 of a DSO.
7. Connect the other end of the probe to J1 of the EMV – TEST PICC.
To improve measurements repeatability and coherency, the cable connecting J1 of the EMV – Test PICC to CH0 of the DSO shall remain connected at all times during testing.

8. Connect a cable to the CLK input of the A/D converter.
9. Connect the other end of the cable to the output J3 of the EMV – TEST CMR.
10. Connect a cable to the input CH0 of the A/D converter.
11. Connect the other end of the cable to the output J4 of the EMV – TEST CMR.
12. Connect a cable to the input J2 of the EMV – TEST CMR.
13. Connect the other end of the cable to the output J2 of the PCD.
14. Connect a USB cable to the PC.
15. Connect the other end of the cable to the USB/I2C Converter.
16. Connect a cable to the other side of the USB/I2C Converter.
17. Connect the other end of the cable to the I2C connector on the EMV – TEST CMR.
18. Connect a cable to Out 1 connector of the Waveform Generator.
19. Connect the other end of the cable to the input of the RF Amplifier.
20. Connect a cable to the output of the RF Amplifier.
21. Connect the other end of the cable to input J1 of the PCD.
22. Connect all power supplies as required.
D.1.2 Implementation Set-up Overview

This implementation is based on an A/D converter using a peak sampling acquisition system. The EMV – TEST CMR generates the A/D converter CLK signal for peak sampling.

PICC signal generation comprises the PICC Coding Generator and the Load Modulation Adjustment. The output of the Load modulation Adjustment connects to the input J2 of the EMV – TEST PICC.

The PCD signal generator comprises the Waveform Generator and the RF Amplifier. The output of the Waveform Generator connects to the input of the RF Amplifier. The output of the RF Amplifier is connected on connector J1 of the EMV – TEST PCD.

The acquisition system comprises the EMV – TEST CMR and an A/D converter circuit board located in a PC. Connector J2 of the EMV – TEST PCD connects to the input J2 of the EMV – TEST CMR. The EMV – TEST CMR generates a clock on its output J3, which is connected on the CLK input of the A/D converter.

The output J4 of the EMV – TEST CMR is connected on CH0 of the A/D circuit board. The field strength of the EMV – TEST PCD is measured on the output J1 of the EMV – TEST PICC. This output connects to CH0 of the DSO, passing through a probe. The example Virtual Instrument (VI) provided with the EMV Test Equipment controls the EMV – TEST CMR.
D.1.3 Test Bench for the PCD Test

Follow this procedure to set up the test bench for PCD testing:

1. Refer to the connectivity diagram in Figure D.2:

The length of each cable shall not exceed 50 cm.

Note 1: Probe can be passive or active, >1 MΩ, <15 pF.

Note 2: A single Trigger A line is shown. In practice, a Trigger B line may also be used. See the text in this section for details.

Note 3: A Frequency Counter is used for some tests.

A Frequency Counter function in another test instrument may also be used.

Figure D.2—Connectivity Diagram to Set up the Test Bench for PCD Testing

In this implementation, the PICC Synchronization Device is controlled by the PC. The PICC Sync Device is capable of generating a trigger for both Type A and Type B transactions, as appropriate.

Since the PICC Coding Generator only features a single trigger (Trg A) input, either Trg A or Trg B shall be connected to it depending on the transaction Type for the test case. The connection depends on the PICC answer to be sent.

For a Type A PICC answer, connect Trg A to the PICC Coding Generator. For a Type B PICC answer, connect Trg B.
2. Depending on the Test Case, connect a cable to the Trg A connector of the PICC Coding Generator and connect the other end of the cable to the Trg A connector of the PICC Sync Device.

_or_

Connect a cable to the Trg B connector of the PICC Coding Generator and connect the other end of the cable to the Trg B connector of the PICC Sync Device.

3. Connect the antenna to the PICC Sync Device.

4. Connect a USB cable from the PC to the PICC Sync Device.

5. Connect a cable to the Out 1 connector of the PICC Coding Generator.

6. Connect the other end of the cable to the IN connector of the Load Modulation Adjustment.

7. Connect a cable to the Out connector of the Load Modulation Adjustment.

8. Connect the other end of the cable to the input J2 connector of the EMV – TEST PICC.

9. Connect a probe to CH0 of a DSO.

10. Connect the other end of the probe to J1 of the EMV – TEST PICC.

**Note**

To improve measurements repeatability and coherency, the cable connecting J1 of the EMV – Test PICC to CH0 of the DSO shall remain connected at all times during testing.

11. Connect a cable to the CLK input of the A/D converter.

12. Connect the other end of the cable to the output J3 of the EMV – TEST CMR.

13. Connect a cable to the input CH0 of the A/D converter.

14. Connect the other end of the cable to the output J4 of the EMV – TEST CMR.

15. Connect a cable to the input J8 of the EMV – TEST CMR.

16. Connect the other end of the cable to the output of a 20 MHz filter.

17. Connect a cable to the input of the 20 MHz filter.

18. Connect the other end of the cable to the output J9 of the EMV – TEST PICC.

19. Connect a USB cable to the PC.

20. Connect the other end of the cable to the USB/I2C Converter.

21. Connect a cable to the other side of the USB/I2C Converter.

22. Connect the other end of the cable to the I2C connector on the EMV – TEST CMR.

23. Connect all power supplies as required.
D.1.4 Implementation Set-up Overview

A PCD under test replaces the EMV – TEST PCD during actual testing. A PICC Synchronization device properly synchronizes the emulated PICC answer with the PCD commands.

PICC signal generation is composed of the PICC Coding Generator connected to a Load Modulation Adjustment. The output of the Load modulation Adjustment goes to input J2 of the EMV – TEST PICC.

The output J1 of the EMV – TEST PICC connects to CH0 of the DSO, passing through a probe, and allows measurement of the field strength of the PCD under test.

Connector J9 of the EMV – TEST PICC connects to input J8 of the EMV – TEST CMR, passing through a 20 MHz filter, and allows measurement of all other parameters.

The CMR generates a clock on its output J3 which connects to the input CLK of the A/D converter.

The output J4 of the EMV – TEST CMR connects to CH0 of the A/D board. An example VI is provided with the EMV Test Equipment and controls the EMV -TEST CMR.

**Note**

As the correct measurement result is the value of the signal at the input of the EMV – TEST CMR and not the one measured on the output, the EMV – TEST CMR gain shall be measured before a complete test session, as described in Chapter 6.
Timing Measurements Methods

This appendix contains important guidelines to maintain consistency across all laboratories in timing measurements.

E.1 Setup of Cursors and their Positioning
   E.1.1 Summary Tables
   E.1.2 Cursors Positioning details
E.1 Setup of Cursors and their Positioning

To maintain consistency across all laboratories in timing measurements, it is important to follow the guidelines described in this appendix.

For all these measurements, the test bench must capture the start and the end of the FDT in a single acquisition.

E.1.1 Summary Tables

Table E-1 summarizes the timing measurement methods regarding Type A:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>$FDT_{A,\text{PICC}}$</td>
<td>Last PCD rising edge</td>
<td>First PICC rising edge</td>
</tr>
<tr>
<td>$FDT_{A,\text{PCD}}$</td>
<td>Last PICC detectable edge</td>
<td>First PCD falling edge</td>
</tr>
</tbody>
</table>

$FDT_{A,\text{PICC}} = t_{\text{END}} - t_{\text{START}}$

$FDT_{A,\text{PCD}} = t_{\text{END}} - t_{\text{START}}$

Table E-1—Type A Summary Table
Table E-2 summarizes the timing measurement methods regarding Type B:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>TR0</td>
<td>Last PCD rising edge</td>
<td>First PICC rising edge</td>
</tr>
<tr>
<td></td>
<td>TR0 = t&lt;sub&gt;END&lt;/sub&gt; - t&lt;sub&gt;START&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>TR1</td>
<td>First PICC rising edge</td>
<td>First PICC phase shift</td>
</tr>
<tr>
<td></td>
<td>TR1 = t&lt;sub&gt;END&lt;/sub&gt; - t&lt;sub&gt;START&lt;/sub&gt; + 16/f&lt;sub&gt;c&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;PICC,S,1&lt;/sub&gt;</td>
<td>First PICC phase shift</td>
<td>Second PICC phase shift</td>
</tr>
<tr>
<td></td>
<td>t&lt;sub&gt;PICC,S,1&lt;/sub&gt; = t&lt;sub&gt;END&lt;/sub&gt; - t&lt;sub&gt;START&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;PICC,S,2&lt;/sub&gt;</td>
<td>Second PICC phase shift</td>
<td>Third PICC phase shift</td>
</tr>
<tr>
<td></td>
<td>t&lt;sub&gt;PICC,S,2&lt;/sub&gt; = t&lt;sub&gt;END&lt;/sub&gt; - t&lt;sub&gt;START&lt;/sub&gt;</td>
<td></td>
</tr>
</tbody>
</table>
## Type B Summary Table

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{PICC,E}}$</td>
<td><img src="image" alt="PICC phase shift preceding last phase shift or PICC last phase shift if $t_{\text{FSOFF}} = 0$" /></td>
<td><img src="image" alt="Last PICC phase shift or last subcarrier peak if $t_{\text{FSOFF}} = 0$" /></td>
</tr>
<tr>
<td></td>
<td>$t_{\text{PICC,E}} = t_{\text{END}} - t_{\text{START}}$ if $t_{\text{FSOFF}} \neq 0$</td>
<td>$t_{\text{PICC,E}} = t_{\text{END}} - t_{\text{START}} - 16/f_c$ if $t_{\text{FSOFF}} = 0$</td>
</tr>
<tr>
<td>$t_{\text{FSOFF}}$</td>
<td><img src="image" alt="Last PICC phase shift if $t_{\text{FSOFF}} \neq 0$" /></td>
<td><img src="image" alt="Last PICC subcarrier peak" /></td>
</tr>
<tr>
<td></td>
<td>$t_{\text{FSOFF}} = t_{\text{END}} - t_{\text{START}} - 16/f_c$</td>
<td></td>
</tr>
<tr>
<td>$E_{\text{GT}}_{\text{PICC}}$</td>
<td><img src="image" alt="Phase shift preceding character n start bit" /></td>
<td><img src="image" alt="Phase shift preceding character n+1 start bit" /></td>
</tr>
<tr>
<td></td>
<td>$E_{\text{GT}}<em>{\text{PICC}} = t</em>{\text{END}} - t_{\text{START}} - 1280/f_c$</td>
<td></td>
</tr>
<tr>
<td>PICC Bit Boundaries</td>
<td><img src="image" alt="Phase shift preceding character n start bit" /></td>
<td><img src="image" alt="Phase shift of each character bit" /></td>
</tr>
<tr>
<td></td>
<td>$\text{PICC Bit Boundary} = t_{\text{END}} - t_{\text{START}}$</td>
<td></td>
</tr>
</tbody>
</table>
### Type B Summary Table

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EGTPCD</strong></td>
<td>Start bit of character (n)</td>
<td>Start bit of character (n+1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{EGTPCD} = t_{\text{END}} - t_{\text{START}} - 1280/f_c)</td>
</tr>
<tr>
<td><strong>PCD Bit Boundaries</strong></td>
<td>Start bit of character (n)</td>
<td>Start of each character bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{PCD Bit Boundary} = t_{\text{END}} - t_{\text{START}})</td>
</tr>
<tr>
<td><strong>FDT_{B,PCD}</strong></td>
<td>Last PICC phase shift if (t_{\text{SOFF}} = 0), else previous phase shift (Start of EoS)</td>
<td>First PCD falling edge</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{FDT}<em>{\text{PCD}} = t</em>{\text{END}} - t_{\text{START}} - 16/f_c)</td>
</tr>
</tbody>
</table>

Table E-2—Type B Summary Table
E.1.2 Cursors Positioning details

The start of the lower level of the SoF of a PCD command is the point where the falling edge of the signal envelope passes through the 90% threshold as shown in Figure E.1:

![Figure E.1 — Type A PCD Start](image)

The end of the last lower level of a PCD command is the point where the rising edge of the last lower level of the signal envelope passes through the 5% threshold as shown in Figure E.2:

![Figure E.2 — Type A PCD End](image)

The start of the SoF of the PICC response begins at the start of the first detectable edge of the
modulation of the signal envelope. Three cases are represented in Figure E.3: start for positive modulation, negative modulation and modulation that is not purely negative or positive.

![Figure E.3 — Type A PICC Start](image)

The end of the last subcarrier modulation transmitted by the PICC corresponds to the end of the last detectable edge of the modulation of the signal envelope. Three cases are represented in Figure E.4: end for positive modulation, negative modulation and modulation that is not purely negative or positive.

![Figure E.4 — Type A PICC End](image)

The start of the SoS of a PCD command is when the first modulation of the signal envelope passes through the 90% level of the Δ threshold (Δ is the difference between modulated and unmodulated signal levels) as shown in Figure E.5:

![Figure E.5 — Type B PCD Start](image)
Figure E.6 indicates the end of the EoS of the PCD command. It is the point where the last modulation of the signal envelope passes through the 10% level of the Δ threshold (Δ is the difference between modulated and unmodulated signal levels).

![Figure E.6 — Type B PCD End](image)

The start of the PICC response begins at the start of the first detectable edge of the modulation of the signal envelope. Three cases are represented in figure E.7: start for positive modulation, negative modulation and modulation that is not purely negative or positive.

![Figure E.7 — Type B PICC Start](image)

The end of the last subcarrier modulation transmitted by the PICC corresponds to the last peak of the modulation of the signal envelope. Three cases are represented in Figure E.8: end for positive modulation, negative modulation and modulation that is not purely negative or positive.

![Figure E.8 — Type B PICC End](image)
As represented in Figure E.9, the nominal position of a phase shift is defined as the point where the signal envelope of the preceding subcarrier cycle passes through the local minimum (for a low phase shift) or the local maximum (for a high phase shift) plus the addition of $1/f_s$ (or $16/f_c$).

**Figure E.9 — Type B PICC Phase Shift**