Samsung S3C2410

World's First ARM-Based Processor with NAND Flash Support

Innovative Design for Mobile and Low-Power Applications

Samsung’s S3C2410 16/32-bit RISC microprocessor is a cost-effective, low-power, high-performance microcontroller solution in a small die size for handheld devices and general mobile applications. To reduce total system cost, the S3C2410 has the following features: separate 16KB instruction and 16KB data cache, MMU to handle virtual memory management, LCD controller (STN & TFT), NAND Flash bootloader, system manager (chip select logic, SDRAM controller), 3-channel UART with handshake, 4-channel DMA, 4-channel timers with PWM, I/O ports, RTC, 8-channel 10-bit ADC and a touch-screen interface, I2C-BUS interface, I2S-BUS interface, USB host, USB device, SD host and multimedia card interface, 2-channel SPI and PLL for clock generation.

By providing a complete set of common system peripherals, the S3C2410 minimizes overall system costs and eliminates the need to configure additional components.
The S3C2410 includes an ARM920T core, 0.18um CMOS standard cells and a memory compiler. Its low-power, simple, elegant and fully static design is particularly suitable for cost- and power-sensitive applications. Also, the S3C2410 adopts a new bus architecture, AMBA (Advanced Microcontroller Bus Architecture). The CPU core for the S3C2410, the 16/32-bit ARM920T RISC processor designed by Advanced RISC Machines, Ltd., was optimized for next-generation mobile devices. By providing a complete set of common system peripherals, the S3C2410 minimizes overall system costs and eliminates the need to configure additional components.

Features

ARM920T CPU Core
- 64-way set-associative cache with:
  I-Cache (16KB) and D-Cache (16KB)
- Write-through and Write-back cache operation
- MMU supports MS WinCE, Linux, Palm OS and Symbian
- Internal AMBA bus architecture

Operating Conditions
- Core: 203/266 MHz
- External I/O: 3.3V
- Memory: 2.5V/3.3V

Package
- 272 FPBGA (14 Body)

Benefits
- Built-in NAND Flash bootloader, SD Host
- Various embedded IP
- Design time reduction with a supporting reference board & RTOS
- Various design applications

On-Chip Peripherals
- Power Management: normal, idle, slow, power-off
- 4-channel 16-bit PWM (Pulse Width Modulation), 1-ch 16-bit timer for OS
- RTC: 32.768 KHz, alarm interrupt
- GPIO:117 (multiplexed I/O)
- 3-channel UART
- 4-channel 16-bit DMA controllers
- 8-channel 10-bit A/D (Max. 500KSPS), including TSP controller
- TFT LCD/STN LCD controller (16bit, 640x480 maximum)
- 16-bit watch-dog timer
- 1-channel I2C-bus interface
- I2S-bus interface
- 2-channel SPI (Synchronous Serial I/O)
- SD Host/MMC (Multi Media Card) I/F
- USB Host/Device interface (ver. 1.1)
- 2-channel USB Host interfaces (1-channel dedicated host and 1-channel selective host/device)
- 1-channel USB Device interface (12Mbps)
- Debug TEST
- NAND Flash controller (4kb internal buffer)
- 24-channel external interrupts controller (wake-up source 16-channel)

Key Applications
- Wireless PDA
- Smartphone
- Game machines
- Point-of-Sale terminals
- Portable media players

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