RTL8201F-CG
RTL8201FN-CG
RTL8201FL-CG

SINGLE-CHIP/PORT 10/100 FAST ETHERNET PHYCEIVER

LAYOUT GUIDE
(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

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1. Introduction

The RTL8201F/RTL8201FN/RTL8201FL is a single-chip/single-port PHYceiver that supports:

- MII (Media Independent Interface)
- RMII (Reduced Media Independent Interface)
- SNI (Serial Network Interface)

The RTL8201F(x) implements all 10/100M Ethernet Physical-layer functions including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), with an auto MDIX function, 10Base-TX Encoder/Decoder, and Twisted-Pair Media Access Unit (TPMAU).

A PECL (Pseudo Emitter Coupled Logic) interface is supported to connect with an external 100Base-FX fiber optical transceiver. The chip utilizes an advanced CMOS process to meet low voltage and low power requirements. With on-chip DSP (Digital Signal Processing) technology, the chip provides excellent performance under all operating conditions.
2. **Design and Layout Basics**

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8201F(x). Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

(1) Create a low-noise, power-stable environment.

(2) Reduce the degree of EMI/EMC and their influence on the RTL8201F(x).

(3) Simplify the task of routing signal traces.

In order to achieve maximum performance using the RTL8201F(x), good design practices are required throughout the process. The following are some recommendations for implementing a high-performance system.

### 2.1. **Placement**

- The RTL8201F(x) should be placed as close as possible to the magnetics

- The resistor connected to the RSET Pin should be placed as close as possible to the RTL8201F(x). Ideally it should be placed away from TX±/−, RX±/−, and clock signals (50mils min.)

- For good EMI performance, the PHY device should be placed as close (less than 8 inches) as possible to the MAC

- The distance between the RJ-45 and Mag. (L3) should be as short as possible

- The traces between the RTL8201F(x) and Mag. (L2) should be as short as possible. For practical implementation convenience, this could be sacrificed. However, it is important to keep the TX±, RX± signal traces symmetrical, and L2 still needs to be kept within a reasonable range; approximately 12cm maximum
• The signal trace length difference between TX+ and TX- (RX+ and RX-) should be kept within 2cm.

Figure 1. MII/RMII and MDI Placements

2.2. Magnetics
• The 10/100M magnetics should be placed as close as possible to the RJ-45 connector.
• The magnetics device, or devices with magnetic fields, should be separated and mounted at 90° to each other.

2.3. Crystal/OSC
• The Crystal should be placed far away from I/O ports, important or high frequency signal traces (TX, RX, power), magnetics, or board edges.
• The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI. The retaining straps of the OSC, if any, need good grounding as well.

2.4. Ferrite Beads and De-Coupling Capacitors
Every PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0Ω resistors. Decoupling capacitors (Z5U, Y5V types are recommended) should be placed as close as possible to the power pins, such that the distance from the IC power pin to the capacitor is less than 200mils.
3. Signal and Trace Routing

Noise, ringing, and data lines have to be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, crosstalk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

- Avoid digital signal (such as MII/RMII or Clock signals) interference with analog signals (TX±, RX±, RTset trace) and Power traces. If it is necessary to cross digital signals with Analog/Power, the cross should be made at a 90° angle (Figure 2).

![Figure 2. Digital Signals Avoidance and Crossing](image-url)
3.1. **MDI Signals**

- Traces routed from the RTL8201F(x) to the 10/100M magnetics, and to the RJ-45 connector, should be as short as possible. The 12cm maximum length between the RTL8201F(x) and magnetics is achievable only when there is no interference.

  It is also very important to keep all differential pair signal traces (MDI0+/-, MDI1+/-, etc.) at matching lengths (within 25mil). MDI impedance is 50ohm common mode, 100ohm differential mode).

  The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong cancelling effect on noise. D1 can be the width of each of the two differential traces. E.g., if the width of the trace is 8mil, then D1 can be 8mil wide (Figure 3).

![MDI Signals](image)

**Figure 3.** MDI Signals

- We suggest that there should be more than 50mil spacing between different differential pairs to minimize crosstalk coupled from other pairs (D2 in Figure 3). In addition, Ground Plane shielding can be used to separate all four signal pairs. However, a good layout should avoid the following situations:
  --Intersection of any two pairs of signal traces.
  --Intersection of the two signal traces of the same differential pair.

- To minimize impedance mismatch, we recommend not using vias on the differential pairs.

- Signals crossing a plane split (see Figure 4) may cause unpredictable return path currents and would likely result in signal quality failure, as well as creating EMI problems.

![Signal Trace](image)

**Figure 4.** Signal Trace
3.2. **MII/RMII Signals**

- Ninety-degree trace turns should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 5. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.

![Figure 5. Signal Trace Angles](image)

- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. Clock and other high speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a GND plane to surround them.

- RXC and TXC are high-speed (25MHz or 50MHz, RMII mode) signals; keep a 20mils spacing between clock and data signals.

- Match each MII TX and RX (RXC/RXD/RXCTL) group trace length to within 100mils.

- Route the MII traces at 50 ohms impedance and use stripline to reduce radiation.

- Keep all MII traces as short as possible.

- All MII traces should be referenced to an unbroken ground or power plane.
- Place R1/C1 (RXC) and R2/C2 (TXC) close to the PHY in MII mode (Figure 6; Only RTL8201F/FN/FL support MII mode).

![Figure 6. R1C1/R2C2 Placement (MII Mode)](image)

- Place the RC filter component close to the source of the reference clock in RMII mode. Figure 7 illustrates when the reference clock is input, i.e., from MAC to PHY. Figure 8 illustrates when the reference clock is output, i.e., from PHY to MAC.

![Figure 7. RC Placement (RMII Mode; Reference Clock is Input)](image)

![Figure 8. RC Placement (RMII Mode; Reference Clock is Output)](image)
• Some return current paths, e.g., clock buffer and clock trace, can couple with the heat sink via parasitic capacitance, then radiate to air from the heat sink. To avoid this, MII traces must be routed away from the heat sink (Figure 9).

![Figure 9. Clock and Heat Sink](image)

• Route MII traces away from I/O traces to avoid crosstalk (Figure 10).

![Figure 10. Clock and I/O Trace](image)
- MII traces (TXC and RXC) and RMII traces (REF_CLK) between the PHY and the MAC should be surrounded by GND trace (see Figure 11 and Figure 12).

![Figure 11. MII Mode Clock (TXC & RXC)](image1)

![Figure 12. RMII Mode Clock (REF_CLK)](image2)
4. Power Supply and Ground Plane

4.1. Power Plane Partition

We recommend using at least a 4-layer PCB. The digital power plane should be separate from analog areas, which are extremely sensitive to noise.

- MDI and MII signals are routed on layer 4 and reference layer 3 (GND plane).

![Four-Layer Stack-Up Diagram](https://via.placeholder.com/150)

Any analog circuitry on the same plane as the digital power will experience an energy fluctuation due to the fast switching time of digital components. This could improperly bias transistors, and cause the circuits to malfunction. A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration (Figure 14, page 10). Keep power traces to the RTL8201F(x) as short and wide as possible and make good use of vias.

(a) Keep the Digital Power Plane as a whole, and leave some space for the Analog Power Plane

![Power Plane Diagram](https://via.placeholder.com/150)
To improve the performance of the power plane, try to keep the contact area between the RTL8201F(x) VDD pins and power plane as large as possible, rather than using small narrow traces (Figure 16).
4.2. **Ground Plane Layout**

- Isolated separation between Analog and Digital Ground domains is not recommended, as bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. Clock and other high-speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces.

![Figure 17. Ground Plane Under Traces](image)

- The RTL8201F(x) has only one ground plane for analog power (AVDD33 and AVDD12) and digital power (DVDD33, DVDD12). In the center of the IC, there is an Exposed Pad (EPAD) ground (RTL8201F and RTL8201FN only). The RTL8201F center EPAD ground size is 3.35x3.35mm (the RTL8201FN is 4.3x4.3mm). The PCB layout requires vias to connect the EPAD to the lower layer ground plane (see Figure 18).

![Figure 18. Ground Plane Layout-1](image)
To achieve better GND plane performance, keep the plane as large and uniform as possible. Figure 19 illustrates a not so good (left) and a good ground plane layout (right).

![Figure 19. Ground Plane Layout-2](image)

The plane area beneath the magnetics should be left void. The void area is to keep transformer-induced noise away from the power and system ground planes (Figure 20).

![Figure 20. Ground Plane Separation](image)

The Chassis Ground as shown in Figure 20 is known as an ‘Isolated Ground’. It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, a 2kV (3kV recommended) high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

It is important to keep the gap (D in Figure 20) between Chassis GND and System GND wider than 60mils for better isolation.
5. Trace Connection of MII Interface to LAN Controller

- Figure 21 shows the RTL8201F(x) LAN-on-Motherboard suggested trace lengths using an optional CNR or ACR connector. The trace length between the LAN controller and the RTL8201F(x) should be as short as possible and, if possible, shorter than 8 inches.

- Be sure that the length mismatch between data signals and the related clock does not exceed 1 inch, i.e., between trace groups such as TXD[0:3] and TXCLK, RXD[0:3] and RXCLK.

- When the RTL8201F(x) is linked at 100Mbps, the TXCLK and RXCLK is 25MHz clock to MAC. When linked at 10Mbps, the TXCLK and RXCLK is 2.5MHz clock to MAC. In RMII mode, TXCLK is 50MHz clock at 10/100M speed. Both TX data and RX data are latched at the rising edge of the clock. For detailed MII timing descriptions and specifications, refer to IEEE 802.3u clause 22.

![Figure 21. LAN-on-Motherboard Suggested Trace Lengths](image)
6. Analog Performance Tips

- Keep a void area of at least 100mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effects and lower EMI emissions.

- The GND pins must maintain a good ground return path, so avoid using single-ended ground. Enlarge the GND plane and try to return the analog circuit’s return current back to the real GND (from the ACR slot) as soon as possible. This is especially important for 2-layer PCB layouts.

- For improved EMI performance when reading/writing from the MII interface, add some decoupling capacitors (0.1µF~10µF) between the system GND and power planes.

- When using a regulator to convert 5V to 3.3V, the rated current of the regulator should be at least 300mA.

- When using an oscillator as the clock source (25MHz or 50MHz), avoid attaching a capacitor to the clock trace.

- When using a 25MHz crystal as the clock source, be sure the crystal meets the requirements shown in Table 1. When using a crystal, two matching capacitors (27pF) should be attached to the X1 and X2 pins.

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<tr>
<td>Frequency</td>
<td>25MHz</td>
</tr>
<tr>
<td>Temperature Stability</td>
<td>±10ppm</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>50% ±10%</td>
</tr>
<tr>
<td>Tolerance</td>
<td>±50ppm</td>
</tr>
<tr>
<td>ESR</td>
<td>Max 30ohm</td>
</tr>
<tr>
<td>Aging</td>
<td>5ppm/year, max.</td>
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Table 1. Reference Clock