Novel Viterbi Decoder VLSI Implementation and its Performance

Shuji Kubota, Shuzo Kato, Member, IEEE, and Tsunehachi Ishitani

Abstract—This paper presents an advanced, high-speed, and universal-coding-rate Viterbi decoder VLSI implementation. Two novel circuit design schemes have been proposed: "scarce state transition (SST)" and "direct high-coding-rate convolutional code generation and variable-rate Viterbi decoding." SST makes it possible to omit the final decision circuit and to reduce the required path memory length without degrading \( P_e \) performance. Moreover, the power consumption of the SST Viterbi decoder is significantly reduced when implemented as a CMOS device. These features overcome the speed limits of high-speed and high-coding-gain Viterbi decoder VLSI's in the rate one-half mode imposed by the thermal limitation. Moreover, the proposed direct high-coding-rate convolutional code generation and variable-rate Viterbi decoding scheme make it possible to realize a simple and variable coding-rate forward-error-correction circuit by changing only the branch metric calculation ROM tables. By employing these schemes, high-speed (25 Mb/s) and universal-coding-rate Viterbi decoder VLSI's have been developed. Experimental results employing developed Viterbi decoder VLSI's confirm satisfactory \( P_e \) performance and high operation speeds under various conditions, for example, AWGN (additive white Gaussian noise), CCI and ACI environments.

I. INTRODUCTION

Forward-Error-Correction (FEC) schemes have been studied and used in radio and satellite communication systems to counter received signal attenuation and to counter \( P_e \) (Probability of errors) performance degradation due to hardware imperfection, adjacent/cochannel interference (ACI/CCI), and so on. Among FEC schemes, convolutional encoding and Viterbi decoding [1] are the most popular because of their powerful coding-gain performances.

In low-speed applications, it is relatively easy to implement high-coding-gain Viterbi decoders and they are widely used. However, in high-speed applications, wider use of Viterbi decoders has been prevented by their massive hardware size, large power consumption, and expensive cost. The hardware size of high-speed Viterbi decoders would be greatly reduced if they could be realized as one-chip LSI's. Such decoder LSI's which can operate in higher coding-rate modes are urgently needed to achieve the high-efficiency use of the limited frequency bands.

Against this background, this paper proposes two new schemes for high-speed and universal-coding-rate VLSI Viterbi decoders. The proposed new schemes make it possible to reduce hardware size and power consumption, and to realize universal-coding-rate Viterbi decoder CMOS VLSI's which can operate at information bit rates of up to 25 Mb/s. The performance and advantages of the developed Viterbi decoder VLSI's are confirmed by satisfactory experimental results under various conditions, for example, AWGN (additive white Gaussian noise), CCI and ACI environments.

II. VITERBI DECODERS REVIEWED

A. Major Functions and Components

To define terms used and components referred to in subsequent sections, the following functions and components are clarified.

1) Branch Metric Calculation: The branch metric is the likelihood metric of received convolutional codes (branch of trellis), and is calculated based on the correlation between the trellis and received convolutional codes.

2) Path metric Calculation and Storage: The path metric of each convolutional code state is calculated by the ACS (Add Compare Select) circuit consisting of adders, a comparator, a selector, and several registers. The number of "states" \( N_s \) of a convolutional encoder which generates \( n \) encoded bits is a function of the constraint length \( K \) and input bits \( b \):

\[
N_s = 2^b (K-1),
\]

Here, the coding rate \( R \) is defined by (2):

\[
R = \frac{b}{n}.
\]

3) Path Selection and Memory: There are two major path memory circuit configurations. One is a path memory cell matrix \( (N_t \parallel\text{parallel}) \) and \( T \)-length, where \( T \) represents the path memory length scheme in which the likelihood path series themselves are selected and memorized. The other one is the trace-back scheme which memorizes only path select signals,
Fig. 1 Block diagram of high-speed Viterbi decoder.

and the likelihood path series are searched by the trace-back operation.

4) Maximum Likelihood Decision: The maximum likelihood decision (MLD) circuit determines the decoding output from among the last bits of \( N_2 \) path memory series. There are three final decision schemes as follows.

a.) Among the \( N_2 \) path memory series, the last bit of path memory series with the maximum likelihood (the largest path metric) is selected as the decoding output.

b.) The decoder output is determined by a majority vote on the last bits of each path memory series.

c.) The last bit of the one of the \( N_2 \) path memory series is selected without any operation.

B. Low-Speed Viterbi Decoder

In low-speed Viterbi decoders, the ACS circuit can be time-shared by several states, thus, the number of ACS circuits can be smaller than \( N_2 \). Many low-speed Viterbi decoders employ the trace-back scheme for the path memory circuit because it allows smaller hardware size than the path memory cell matrix scheme.

C. High-Speed Viterbi Decoder

In high-speed Viterbi decoders, there must be \( N_2 \) ACS circuits, and the path memory circuit consists of a path memory cell matrix. A block diagram of a general high-speed Viterbi decoder is shown in Fig. 1.

D. LSI Implementation Strategies

Several approaches have been created to implement Viterbi decoders as VLSI’s.

1) Low-speed Viterbi decoder LSI’s (ACS circuit LSI) with the external path memory circuit composed of random access memory (RAM).

2) High-speed multichip Viterbi decoder LSI’s (ACS circuit LSI’s) using external path memory circuits or other path memory LSI’s.

3) High-speed one-chip Viterbi decoder LSI (ACS and path memory circuit LSI) [2]–[6].

By employing CMOS full custom technologies, the last approach can accommodate 64-state ACS circuits and path memory circuits in one-chip VLSI’s [7], [8]. However, there is still a strong need for higher speed (\( \geq 25 \text{ Mb/s} \)) one-chip Viterbi decoder LSI’s with easy coding-rate changeability. In order to meet this need, a reduction in the required number of gates and power consumption is most important.

III. PROPOSED HIGH-SPEED VITERBI DECODER IMPLEMENTATION SCHEMES

A. SST Scheme

1) Details: In order to reduce the hardware size and power consumption of high-speed Viterbi decoder VLSI’s, the SST (scarce state transition) scheme has been proposed. An SST Viterbi decoder is composed of a conventional Viterbi decoder (narrow-sense Viterbi decoder: a branch metric calculator, ACS circuits, and a path memory circuit) and some additional circuits. A schematic block diagram of the SST Viterbi decoder with \( R = 1/2 \) and \( K = 7 \) for 3 b soft decision data (natural binary quantization) is shown in Fig. 2.

The mathematical expression of the decoding procedure in SST Viterbi decoders can be explained as follows. Codes are described with the Galois field represented as GF(2) = \( (0, 1) \), and they can be added in ordinary modulo-2 addition. The source signal sequence is defined by (3), where \( I_u \) is the source signal at time \( u \):

\[
I = (I_0, I_1, I_2, \ldots, I_u, \ldots).
\]  

(3)

The generator polynomials of the convolutional encoder are expressed as follows, where \( \bar{D} \) denotes delay operator and "\( + \)" denotes modulo-2 addition:

\[
G^{(1)} = 1 + D + D^2 + D^3 + D^6
\]  

(4.1)

\[
G^{(2)} = 1 + D^2 + D^3 + D^5 + D^6.
\]  

(4.2)
Then the transmitted convolutionally encoded data at time $u$, $T_u^{(1)}$ and $T_u^{(2)}$ are expressed by the following equations:

$$T_u^{(1)} = I_u + I_{u-1} + I_{u-2} + I_{u-3} + I_{u-6} \quad (5.1)$$

$$T_u^{(2)} = I_u + I_{u-2} + I_{u-3} + I_{u-5} + I_{u-6}. \quad (5.2)$$

By defining channel errors at time $u$ as $E_u^{(1)}$ and $E_u^{(2)}$ for $T_u^{(1)}$ and $T_u^{(2)}$, respectively, with the value of “1” when an error occurs, the received convolutionally encoded data at time $u$ are expressed by (6.1) and (6.2) as follows:

$$R_u^{(1)} = T_u^{(1)} + E_u^{(1)} \quad (6.1)$$

$$R_u^{(2)} = T_u^{(2)} + E_u^{(2)} \quad (6.2)$$

In the (6.1) and (6.2), $E_u^{(1)}$ and $E_u^{(2)}$ express hard decision errors for the hard decision mode. However, they can be easily extended to the soft decision mode by letting $E_u^{(1)}$ and $E_u^{(2)}$ be the sign bits (MSB) of soft decision errors and using the magnitude bits (BIT2 and BIT3).

The SST Viterbi decoder first uses the simple predecoder, such as the inverse circuit for a convolutional encoder [9], to predecode the source signal from $R_u^{(1)}$ and $R_u^{(2)}$. The predecoded source signal $Q_u$ at time $u$ is expressed by (7):

$$Q_u = \sum_{i=0}^{4} E_u^{(i)} + R_u^{(i)} + R_u^{(i-4) \pmod{4}} \quad (7)$$

Finally, the reencoder with the generator polynomials $G^{(1)}$ and $G^{(2)}$, $P_u^{(1)}$ and $P_u^{(2)}$ actually represent convolutionally encoded data of $E_u^{(1)}$ which are coupled with channel errors. Therefore, if the second terms of (11.1) and (11.2) are corrected perfectly by the narrow-sense Viterbi decoder, the output datum of this decoder $D_u$ is obtained as $E_u^{(1)}$, which is the original source signal of $T_u^{(1)}$ and $T_u^{(2)}$. When the throughput delay of the narrow-sense Viterbi decoder is $\tau$, $D_u$, the output signal at time $u$ is expressed by (12):

$$D_u = E_u^{(1)} + E_u^{(2)} \quad (12)$$

Next, the reencoded data with the generator polynomials $G^{(1)}$ and $G^{(2)}$ generates convolutionally reencoded data $R_u^{(1)}$ and $R_u^{(2)}$ from $Q_u$:

$$R_u^{(1)} = T_u^{(1)} + T_{e,u}^{(1)} \quad (9.1)$$

$$R_u^{(2)} = T_u^{(2)} + T_{e,u}^{(2)} \quad (9.2)$$

where $T_u^{(1)}$ and $T_u^{(2)}$ are defined by (10.1) and (10.2) and represent convolutionally encoded data of $E_u^{(1)}$ according to $G^{(1)}$ and $G^{(2)}$:

$$T_u^{(1)} = E_u^{(1)} + E_{u-1}^{(1)} + E_{u-2}^{(1)} + E_{u-3}^{(1)} + E_{u-6}^{(1)} \quad (10.1)$$

$$T_u^{(2)} = E_u^{(2)} + E_{u-2}^{(2)} + E_{u-3}^{(2)} + E_{u-5}^{(2)} + E_{u-6}^{(2)} \quad (10.2)$$

The results of modulo-2 addition of the convolutionally reencoded data $R_u^{(1)}$, $R_u^{(2)}$ and 1b delayed received data $R_{u-1}^{(1)}$, $R_{u-1}^{(2)}$, denoted by $P_u^{(1)}$ and $P_u^{(2)}$ at time $u$, are obtained from (6.1), (6.2), (9.1), and (9.2).

$$P_u^{(1)} = R_u^{(1)} + R_u^{(1)} = T_u^{(1)} + E_u^{(1)} + T_{e,u}^{(1)}$$

$$P_u^{(2)} = R_u^{(2)} + R_u^{(2)} = T_u^{(2)} + E_u^{(2)} + T_{e,u}^{(2)} \quad (11.1)$$

Since $T_{e,u}^{(1)}$ and $T_{e,u}^{(2)}$ are convolutionally encoded data of $E_u^{(1)}$ with generator polynomials $G^{(1)}$ and $G^{(2)}$, $P_u^{(1)}$ and $P_u^{(2)}$ actually represent convolutionally encoded data of $E_u^{(1)}$ which are coupled with channel errors. Therefore, if the second terms of (11.1) and (11.2) are corrected perfectly by the narrow-sense Viterbi decoder, the output datum of this decoder $D_u$ is obtained as $E_u^{(1)}$, which is the original source signal of $T_u^{(1)}$ and $T_u^{(2)}$. When the throughput delay of the narrow-sense Viterbi decoder is $\tau$, $D_u$, the output signal at time $u$ is expressed by (12):

$$D_u = E_u^{(1)} + E_u^{(2)} \quad (12)$$

Finally, the output signals of the SST Viterbi decoder at time $u$, $DI_u$ are obtained by modulo-2 addition of $D_u$ and $E_u^{(1)} - E_u^{(2)}$ as follows:

$$DI_u = D_u + E_u^{(1)} - E_u^{(2)} = I_u-\tau - I_u-\tau-1 \quad (14)$$

In the SST Viterbi decoding scheme, the source signal according to the input signals of the narrow-sense Viterbi decoder $E_u$ is “zero,” but not when channel error occurs. Therefore, in this scheme, the state which corresponds to all “zero” almost always has the maximum path metric, while in the conventional methods, the distribution probability of the maximum likelihood state is equal since input signals are usually random.

On the other hand, syndrome decoders employing formers at the input of the narrow-sense Viterbi decoder have been proposed [10] to simplify hard decision Viterbi decoders. However, the major difference of SST Viterbi decoders compared to syndrome decoders is that SST Viterbi decoders operate according to the state transition of soft decision channel errors ($E_u^{(1)}$) while syndrome decoders operate according to the state of the syndrome former.

2) Hardware Reduction: For Viterbi decoder VLSI implementation, the configuration without the MLD circuit [the third method in Section II-A (4)] is most suitable because of its simple circuit and wiring configuration. With the SST scheme, the state which corresponds to all “zero” almost always has the largest path metric. Thus, without degrading $Pe$ performance, it is possible to omit the MLD circuit and shorten the required path memory length. The required path memory
lengths of the SST and conventional Viterbi decoders which suffer no Pe performance degradation while omitting MLD circuits are shown in Fig. 3. As shown in this figure, the SST Viterbi decoder requires a shorter path memory length than the conventional one (ΔL₁). Furthermore, the SST Viterbi decoder makes it possible to reduce the ΔL₁ + ΔL₂ path memory length with a slight degradation in Pe performance.

3) Power Consumption Reduction: In the SST Viterbi decoder, data stored in the path memory circuit are almost always “zero,” except the data affected by channel errors. Thus, ON or OFF switchings of gates seldom occur in the path memory circuit. Therefore, the power consumption of a CMOS SST Viterbi decoder is significantly less than that of conventional decoders, as shown in Fig. 4. For example, the power consumption reduction is 40% at Pe = 1 x 10⁻⁴.

Moreover, the proposed SST scheme makes it possible to omit the MLD circuit and reduce the required path memory length without Pe performance degradation. This hardware reduction also contributes to power consumption reduction. As a result, the total power consumption of a CMOS SST Viterbi decoder VLSI is less than 1 W in the nominal operation range (Pe = 5 x 10⁻⁴) at an information bit rate of 25 Mb/s. This satisfies the important requirement of low power consumption for higher density accommodation of IC’s and the LSI’s without enforced cooling.

The SST scheme, with its very low power consumption characteristics, makes it possible to develop single-chip Viterbi decoders that have higher speed ACS circuits [11] or longer constraint length (K = 8 or more).

B. Universal-Coding-Rate Operation

Higher coding-rate Viterbi decoders are urgently required to achieve high-efficiency use of the limited frequency band. Unfortunately, implementing such Viterbi decoders in a straight forward manner requires massive hardware and large power consumption. It is well known that the “punctured” convolutional coding scheme [12], [13] can realize high-coding-rate Viterbi decoders with the use of low-coding-rate encoders and decoders. However, this method requires bit complicated processing operations such as bit stealing on the transmission side and matching dummy bit insertion at the receiving side according to the deletion pattern at the transmission side. To remove this complexity, a simple decoding scheme and easier coding-rate changeability were needed.

The proposed high-coding-rate scheme permits high-speed and higher coding-rate operation without any additional operations such as the bit stealing, dummy bit insertion, and complicated timing control required in the “punctured” scheme [13]. Block diagrams of the convolutional encoder and the variable-rate Viterbi decoder are shown in Fig. 5 and Fig. 6, respectively. On the transmission side, source signals are fed to a direct high-coding-rate convolutional encoder and encoded directly into transmission data according to generator polynomials. On the receiving side, received convolutionally encoded signals (soft decision data) are entered to the branch metric calculator with the synchronization signals, and the branch metrics are calculated at the channel signal rate. The output branch metrics are conveyed to speed converter FIFO (fast-in fast-out) memories, and their speeds are converted from the channel data rate to a source signal rate. The output branch metrics are then conveyed to the ACS circuits and decoded according to the well-known Viterbi decoding algorithm. The speed conversion operation of the proposed scheme and the
dummy bit insertion operation of the conventional punctured scheme are compared in Fig. 7. In the proposed scheme, the number of FIFO bits is four times the number of branch metric bits, but FIFO uses very simple circuits suitable for LSI implementation, and by employing this configuration, the complicated punctured clock in channel signal rate is no longer needed. This variable-rate Viterbi decoder is applicable for all $R = (n-1)/n$ convolutional codes such as $R = \frac{1}{2}, \frac{3}{4}, \frac{7}{8}, \frac{15}{16}$, and so on. Only the branch metric calculation table (ROM table) and speed conversion rate at the FIFO memories need to be changed.

IV. VLSI IMPLEMENTATION

A. Function Assignment

To implement the VLSI Viterbi decoder, the following conditions should be satisfied to ensure its universal applicability ($R = \frac{1}{2} - \frac{15}{16}$) and high-speed ($\geq 25 \text{ mb/s}$) performance.

1) Multiple LSI's are needed for high-coding-rate modes because state-of-the-art VLSI technology cannot offer the required number of gates on one chip.

2) Because a rate one-half Viterbi decoder (constraint length of 7) is most common, it should be implemented on one-chip.

3) Operation speed should not be limited by junction temperature limitation caused by high power consumption.

4) The final chip set should have the minimum number of VLSI chips.
5) Interface conditions between LSI’s shall be simple. From conditions 1) and 2), the universal-coding-rate Viterbi decoder VLSI (constraint length 7) was divided into a rate one-half Viterbi decoder VLSI (NUFEC TYPE 1 VLSI) and a path memory VLSI (NUFEC TYPE 2 VLSI). To satisfy condition 3), the SST operation was employed for the rate one-half mode and electrically shutting off of the path memory circuit was employed for higher coding-rate modes (>1/2) on the NUFEC TYPE 1 VLSI. The power consumption characteristics of the NUFEC TYPE 1 VLSI with/without the SST scheme and with the electrically shutting off of the path memory circuit are shown in Fig. 8. As seen from this figure, the power consumption of the NUFEC TYPE 1 VLSI without the SST scheme easily exceeds 1.2 W at speeds higher than 25 MHz, which is the limit for VLSI without enforcing cooling. The maximum operation speed is limited to less than 20 MHz due to thermal effects, while the NUFEC TYPE 1 VLSI with the SST scheme has a power consumption less than 1.2 W at a clock rate of 25 MHz. Electrically shutting off of the path memory circuit for higher coding-rate operation achieves power consumption characteristics less than 0.6 W at a clock rate of 25 MHz. Thus, these two tactics make it possible for the NUFEC TYPE 1 VLSI to be stably operated at a clock rate of 25 MHz. Moreover, the latter tactic simultaneously satisfies the condition 5), the last condition to be solved is 4), but it partly contradicts condition 3). The required path memory length and the number of VLSI’s versus coding-rates are shown in Fig. 9. In this figure, a path memory length of 64 is assumed for the NUFEC TYPE 2 VLSI since this is the maximum available path memory length on a one-chip VLSI at the present time. By employing the path memory circuit in the NUFEC TYPE 1 VLSI, the required number of VLSI’s is fewer by 1 than without it. However, in the former configuration, the NUFEC TYPE 1 VLSI will not operate at a clock rate of 25 MHz due to thermal limitation, as discussed above.

Therefore, the best configuration for the universal-coding-rate Viterbi decoder was determined to be an SST Viterbi decoder VLSI (NUFEC TYPE 1 VLSI) with the electrically shutting off of the path memory circuit function followed by 64-stage path memory VLSI’s (NUFEC TYPE 2 VLSI). For higher coding-rate operation, two or more cascaded NUFEC TYPE 2 VLSI’s can be used.

B. NUFEC VLSI Features

1) NUFEC TYPE 1 VLSI: The NUFEC TYPE 1 VLSI is composed of a branch metric calculator, an ACS circuit block which has 64 states, a path memory block for an $R=1/2$ mode, and a speed converter FIFO for high-coding-rate modes. It accommodates the predecoder and reencoder needed for SST functions.

2) NUFEC TYPE 2 VLSI: The NUFEC TYPE 2 VLSI is composed of the path memory circuit with a path memory length $T$ of 60. This VLSI is cascaded as the path memory for higher coding-rate (>1/2) modes.

The major parameters of both VLSI’s are summarized in Table I, and a chip microphoto of the NUFEC VLSI’s is shown in Figs. 10 and 11. This VLSI implementation reduces the hardware size (number of IC’s) to 1/2400 and the power consumption to 1/200 from conventional high-speed $R=1/2$ and $K=7$ Viterbi decoders composed of discrete IC’s.

3) NUFEC TYPE 3 LSI: Furthermore, to realize a convolutional encoder with various coding rates and a self code-synchronization circuit in a one-chip LSI, the NUFEC TYPE 3 LSI has been developed by employing CMOS master slice LSI technologies. It also operates up to an information bit rate of 25 Mb/s. The major parameters of the NUFEC TYPE 3 LSI are shown in Table II.

V. PERFORMANCE OF NUFEC VLSI

A. Probability of Errors

Measured $P_e$ performance of the developed NUFEC Viterbi decoder VLSI’s with coding rates of 1/2, 3/4, 7/8, and 15/16 at a bit rate of 25 MHz is shown in Fig. 12. The net-coding gains in each coding rate at $P_e = 1 \times 10^{-6}$ are 5.5, 4.5,
TABLE I
MAJOR PARAMETERS OF NUFEC TYPE 1 AND NUFEC TYPE 2 VLSI

<table>
<thead>
<tr>
<th></th>
<th>NUFEC TYPE 1</th>
<th>NUFEC TYPE 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process (device)</td>
<td>CMOS 1.5 μm full custom</td>
<td>CMOS 1.5 μm full custom</td>
</tr>
<tr>
<td>Number of gates</td>
<td>45 000</td>
<td>45 000</td>
</tr>
<tr>
<td>Maximum data rate</td>
<td>25 mb/s</td>
<td>25 Mb/s</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>+5 V</td>
<td>+5 V</td>
</tr>
<tr>
<td>Number of pins</td>
<td>208</td>
<td>280</td>
</tr>
<tr>
<td>Major function</td>
<td>$R = 1/2, K = 7$ convolutional encoded/Viterbi decoder</td>
<td>60-stage path memory circuit</td>
</tr>
</tbody>
</table>

Coding gain at $P_e = 10^{-4}$

- $R = 1/2$ 4.5 dB (employing 1 NUFEC TYPE 1)
- $R = 3/4$ 3.7 dB (employing 1 NUFEC TYPE 1, 1 NUFEC TYPE 2)
- $R = 7/8$ 2.8 dB (employing 1 NUFEC TYPE 1, 2 NUFEC TYPE 2)
- $R = 15/16$ 1.5 dB (employing 1 NUFEC TYPE 1, 3 NUFEC TYPE 2)

3.3 and 2.2 dB, respectively. As seen from these results, the developed NUFEC VLSI's have satisfactory high-coding-gain performances in various coding rates.

B. Bit Error Pattern After Decoding

In order to expand the application fields of the proposed FEC scheme, it is important to clarify the burst error characteristics of decoded data. For this purpose, conditional probabilities of errors after 1 b error occurrence in decoded data were measured and are shown in Fig. 13. As seen from this figure, longer burst errors occur at higher coding rates, and the required interleaving bit length can be determined from these data.

C. Improvement on $P_e$ Performance Degradation due to CCI

The advantages of the FEC technique include not only a reduction in the required $C/No$ ($E_b/No$), but also improved $P_e$ performance in interference environments. This $P_e$ performance improvement also increases the effective frequency utilization efficiency. To clarify $P_e$ performance improvements

Fig. 10 Chip microphotograph of NUFEC TYPE 1.

Fig. 11 Chip microphotograph of NUFEC TYPE 2.

Fig. 12 $P_e$ performance of NUFEC VLSI's (25 Mb/s).

Fig. 13 Probability of decoded errors (conditional probability of decoded errors).
of the developed Viterbi decoder in CCI environments, the following experiments were carried out employing the experimental system shown in Fig. 14. The desired signal and the CCI (undesired) signal were both QPSK signals which were nonlinearly amplified (hard-limited), and the desired/undesired signal power ratios $D/U_s$ were set to 15, 20, and infinite (interference free). The $P_e$ performances with/without the $R = 7/8$ convolutional encoder and the NUFEC Viterbi decoder in CCI (cochannel interference) environments are shown in Fig. 15. Even if in the heavy interference environment of $D/U = 15 \text{ dB}$, a $P_e$ of $1 \times 10^{-6}$ is achieved with only 1 dB degradation by employing FEC, there is more than 2 dB of $P_e$ performance degradation without FEC.

D. Improvement on $P_e$ Performance Degradation due to ACI

By employing the above-mentioned experimental system, the $P_e$ performances with/without the $R = 7/8$ convolutional encoder and the NUFEC Viterbi decoder in an ACI environment were measured and are shown in Fig. 16. The desired and ACI signals were nonlinearly amplified (hard-limited) QPSK signals and the frequency utilization efficiency is 1.0 b/s/Hz. The $P_e$ performance degradation without FEC at $P_e = 1 \times 10^{-6}$ is more than 3 dB. However, the employment of the $R = 7/8$ FEC reduced it to about 1 dB. These results show a significant performance improvement in ACI environments, and confirm that the frequency utilization efficiency can be increased by employing high-coding-rate NUFEC Viterbi decoders.

VI. CONCLUSION

Novel high-speed and high-coding-gain Viterbi decoder VLSI implementation strategies have been proposed. The SST scheme has made it possible to realize high-speed $R = 1/2$ and $K = 7$ Viterbi decoder CMOS full custom VLSI's by reducing hardware size and power consumption significantly. Moreover, to realize high-speed and a simple universal-coding-rate function, a direct high-coding-rate convolutional code generation and decoding scheme was proposed to simplify Viterbi decoder VLSI implementation. The developed NUFEC VLSI's operate at 25 Mb/s by employing the SST scheme for the rate one-half mode and the electrical path memory shutting-off technique for higher coding-rate modes (>1/2 mode). They also show high-coding-gain performances in the various coding-rate modes from $R = 1/2$ to 15/16. The powerful coding gain of these Viterbi decoder VLSI's makes it possible not only to reduce the required channel $E_b/N_0$, but also to restrict the degradation in $P_e$ performance caused by various distortion or interference factors, such as CCI or ACI, hardware imperfection, and so on. The advent of these VLSI's makes it possible to significantly reduce hardware size and cost while improving reliability. Moreover, the proposed Viterbi decoder LSI implementation strategies can realize higher operation speeds and higher coding-gain (in other words, longer constraint length) Viterbi decoder VLSI's.

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Fig. 15 $P_e$ performance in cochannel interference environment ($D/U$ = infinite, 20, and 15 dB).

Fig. 16 $P_e$ performance in adjacent channel interference environment ($E_b/N_0 = 1.0$ b/s/Hz).

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Shuji Kubota was born in Tokyo, Japan, on January 2, 1957. He received the B.E. degree from the University of Electro-Communications, Tokyo, Japan, in 1980.

Since joining NTT in 1980, he has been engaged in research and development of forward-error-correction schemes and modulation schemes for satellite and personal communication systems. From 1991 to 1992, he was with the University of California, Davis, as a Visiting Researcher. He is currently a Senior Research Engineer in the Personal Communication Equipment Group of NTT Radio Communication Systems Laboratories.

Shuzo Kato (S'75–M'77) was born in Hokkaido, Japan, on November 17, 1949. He received the B.E. degree in electrical engineering from Kitami Institute of Technology, Japan, in 1971, and the M.E. and Ph.D. degrees in electrical and communication engineering from Tohoku University, Japan, in 1973 and 1976, respectively.

He has been with NTT Electrical Communication Laboratories since 1976, working on research and development of TDMA equipment, modems, and forward-error-correction schemes for satellite communications. From 1981 to 1982 he was with the University of Ottawa, Ont., Canada, doing research on modems as a Postdoctoral Fellow. He currently is a Group Leader, Personal Communication Equipment, NTT Radio Communication Systems Laboratories, responsible for portable terminals and base stations research and development for personal communications and TDMA equipment, modem, and forward-error-correction technologies for satellite communications.

Dr. Kato has been serving as an Editor for IEEE TRANSACTION ON COMMUNICATIONS and as Vice Chairman of the Satellite and Space Communications Committee, IEEE Communications Society.

Tsunehachi Ishihata was born in Kyoto, Japan, in 1949. He received the B.S. degree from Shizuoka University, Shizuoka, Japan, in 1972. In 1972 he joined the NTT Electrical Communication Laboratories, where he worked on the research and development of high-speed bipolar logic LSI's and VLSI communication processing for packet switching. Since 1983 he has been engaged in the development of high-performance CMOS logic VLSI's. He is now an LSI Design Manager in the MOS Digital LSI Design Section, NTT Electronics Technology Corporation, Kanagawa, Japan.

Mr. Ishihata is a member of the Institute of Electronics, Information, and Communication Engineers of Japan.