Imaging and Entertainment Solutions
With Networking Computing Systems Group

Reliability & Quality Audit Report
(By Monitor Center)

Fourth Quarter 1998
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Section 1

Test Methodology

- Motorola’s Reliability Audit Program
- Reliability Data Analysis Methods and
- Reliability Stress Test Descriptions
- Reference:

- Commonly Used Abbreviations
- Technology description for products
MOTOROLA’S RELIABILITY AUDIT PROGRAM

The Motorola Reliability and Quality Audit Program is designed to generate an ongoing database of reliability and quality performance for various categories of products. This program allows Motorola to develop a large database of reliability results that can be reported to customers and will identify any negative trends requiring corrective action.

The reliability monitor tests are conducted on sample groups pulled on a quarterly basis from products representing a matrix of processing and packaging technologies. Product mix, sample availability, and equipment capacity may cause the specific products chosen for testing to vary from quarter to quarter. Each sample group is subjected to a specific set of reliability tests appropriate for that product type. At the end of each quarter, results are reported for all sample groups that have completed testing within the past one year.

These testing and reporting systems combine to form a comprehensive reliability monitor program for each fabrication and assembly process used to produce Motorola integrated circuits.

For Reliability Data Analysis Methods and Reliability Stress Test Descriptions Refer to http://www.mot.com/SPS/HPESD/quality/csg/3Q98/index.html

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### ABBREVIATIONS USED THROUGHOUT THE DOCUMENT

**ASSY SITE:**
- AIZ - Aizu, Japan
- AMT - Batam Island, Indonesia
- ANAM - Anam, Korea
- ANM(BC) - Buchon, Korea
- ANM(BY) - Bupyung, Korea
- ASE(K) - Kaohsiung, Taiwan
- ASE(M) - Penang, Malaysia
- ASTRA - Astra, Indonesia
- ATX - Austin, Texas
- CHAN - Chandler, Arizona
- CIT - Citizen Watch, Tanashi
- FUJITSU - Fujitsu Miyagi, Japan
- GDL - Mexico
- HTY - Hitachi Yonezawa, Yamagata, Japan
- KLM - Kuala Lumpur, Malaysia
- MCEL - Tianjin, China
- METL - Chung-Li, Taiwan
- MHT - Mitsui Kitakyushu, Japan
- MKL - Seoul, Korea
- NIC - Nihon Inter, Japan
- OHT - Oak Hill, Texas
- P1 - Profit Industrial Bldg., Hong Kong
- ROHM - Fukuoka, Yukuhashi Japan
- SEN - Sendai, Japan
- SHC - Silicon Harbor Center, Hong Kong
- SKO - Shinko Denki, Japan
- STL - Swire, Hong Kong

**FAB SITE:**
- BP1 - Mesa, Arizona
- BP2 - Mesa, Arizona
- BP3 - Mesa, Arizona
- BP4 - Toulouse, France
- IWATE - Sendai, Japan
- LGS1 - Gumi, Lucky Goldstar
- LGS2 - Cheong Ju, Lucky Goldstar
- MOS1 - East Kilbride, Scotland
- MOS3 - Austin, Texas
- MOS5 - Mesa, Arizona
- MOS6 - Mesa, Arizona
- MOS7 - Aizu, Japan
- MS7A - Aizu, Japan
- MOS8 - Austin, Texas
- MOS9 - East Kilbride, Scotland
- MS10 - Irvine, California
- MS11 - Oakhill, Texas
- MS12 - Phoenix, Arizona
- MS13 - Austin, Texas
- MS15 - North Carolina
- MS20 - Toulouse, France
- ND - Nippon Denso; Aichi-Kota, Japan
- NWL - Newport Wales Limited
- PHX - Phoenix
- SEP - Seiko Epson, Japan
- THINK-O - Ibara, Japan
- TOWER - Migdal Haemek, Israel
- TSC - Sendai, Japan
- TSC8 - Sendai, Japan
- ZENER - Phoenix

**PACKAGE: Package Type**
- **BGA** - Ball Grid Array
- **CERDIP** - Ceramic Dual In-Line Package
- **LQFP** - Low Profile QFP
- **MFP** - Mini Flat Pack
- **PDIP** - Plastic Dual In-line Package
- **PGA** - Pin Grid Array
- **PLCC** - Plastic Leaded Chip Carrier
- **QFP** - Quad Flat Pack
- **SDIP** - Shrink Dual In-line Package
- **SPDIP** - Shrink PDIP
- **SOIC** - Small Outline Integrated Circuits (150mils)
- **SOP** - Small Outline Package
- **SOWB** - SOIC Wide Body (300mils)
- **SVMFP** - Short MFP
- **SP** - Plastic DIP
- **TDIP** - Tape Automated Bonding
- **TQFP** - Thin Quad Flat Pack

**Technology**
- **SLM:** Single Layer Metal
- **DLM:** Double Layer Metal
- **TLM:** Triple Layer Metal
- **CMOS:** Complimentary Metal Oxide Semiconductor
- **HCMOS:** High Density CMOS
- **EEPROM:** Electrical EPROM
- **EPROM:** Erasable Programmable Read Only Memory
- **EPI:** Epitaxial
- **MOSAIC:** Motorola Self Aligned IC
- **MS:** MOSAIC 1
- **MS15:** MOSAIC 1.5
- **STDLI:** Standard Linear (Analog)
Technology Descriptions

HCMOS PROCESS
HCMOS stands for High Density Complementary Metal Oxide Semiconductor. It is used to describe the basic CMOS process (using both p-channel and n-channel MOSFET transistors) for a given shrink level. Devices with 1.0 micron and greater effective gate length are built using a single layer of polysilicon for transistors and interconnections, and a single layer of metal for both signal and power routing. Sub-micron devices may use one, two, or three layers of metal. Circuits built using this process are generally described as digital logic, including CPU's timers, SCI, SPI communications circuits, and RAM and ROM memory arrays.

DOUBLE POLY ANALOG PROCESS
This process employs a two different polysilicon layers, one for transistor gates and a second layer for analog components, such as capacitors. Metal usage is the same as described for HCMOS.

EPROM AND EEPROM PROCESS
EPROM and EEPROM devices use an electrically isolated (floating) poly-silicon gate to store charge for data retention as well as high voltage transistors for energy switching to the EPROM and/or EEPROM arrays. EEPROM devices contain an internal capacitive charge pump which boosts the 5 volt $V_{DD}$ up to the necessary voltage to achieve tunneling required for programming the memory cells. EPROM devices use external power supplies to provide programming power. Both the EPROM and EEPROM processes are supersets of the double poly analog process.

CMOS AND HMOS PROCESSES
These processes are used for older generation devices. No new products are being introduced using these technologies. CMOS processes include both metal gate and polysilicon gate transistors while HMOS uses n-channel, polysilicon gate transistors. All devices built from this group using these two technologies are single layer polysilicon and single level metal, with the exception of HMOS EPROM micro-controllers which use two layers of polysilicon in the same manner as their HCMOS counterparts.

EPI85
EPI85 is a Bipolar Epitaxial process with the operating voltage not exceeding 3.0 Volts, limited to 20 Volts if any NPN transistor of the design is forced to a BVceo configuration.

**EPI92**
EPI92 is a Bipolar Epitaxial process with the operating voltage not exceeding 2.0 Volts, limited to 12 Volts if any NPN transistor of the design is forced to a BVceo configuration.

**MOSAIC 1.5**
MOSAIC is a Bipolar Analog process, with oxide isolation, Ion implantation of all dopants, and Master Mask Techniques associated. The maximum power supply of this process is 5 Volts.

**SMARTMOS 2.5**
SmarTMOS 2.5 is a Power Bipolar, CMOS, DMOS process, having on the same chip dense logic, analog functions and one or several TMOS power transistors. It is well adapted to the automotive environment, with 60V blocking capability and a maximum current of 15A.
Section 2

Japan Monitor Center

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- Fabrication Cross Reference Table
- Assembly Cross Reference Table
- Reliability Data by Wafer Process
- Reliability Data by Package
- External Visual after Preconditioning
- Reliability Data by Device
- Failure Analysis
### DEVICE CROSS REFERENCE TABLE

#### (1) WAFER PROCESS / DEVICE CROSS REFERENCE TABLE

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<td>MOS7</td>
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## (2) PACKAGE TYPE / DEVICE CROSS REFERENCE TABLE

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### RELIABILITY AUDIT PROGRAM RESULTS

(1) Reliability Data by Wafer Process

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<th>Process</th>
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(2) Reliability Data by Package

a. Temperature Humidity Bias (GTLCC80HS was performed static condition)

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b. Temperature Cycle

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|              | TOTAL        | 3/3971         | 0/1157                     | 0.08   |
(3) External Visual after Precondition for QFP

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(4) Reliability Data by Device

HTOL (125°C, VoprMAX, Dynamic)

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HTOL (145°C, VoprMAX, Static)

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**TEMPERATURE HUMIDITY BIAS WITH PRECONDITIONING** (JBD1201ZU was not biased)

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<td>EME5000LS</td>
<td>2</td>
<td>0/90</td>
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<tr>
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<td>PDIP20</td>
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<td>ST10F</td>
<td>4</td>
<td>1/180</td>
<td>0/45</td>
<td>0.56</td>
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</table>

<table>
<thead>
<tr>
<th>WSSG</th>
<th>Device Type</th>
<th>Package Type</th>
<th>Assy Type</th>
<th>Site</th>
<th>Compound</th>
<th>#of LOT</th>
<th>96hrs</th>
<th>288hrs</th>
<th>ACCUM%</th>
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<tbody>
<tr>
<td>MC145158F2</td>
<td>MFP16</td>
<td>AIZ</td>
<td>EME5000LS</td>
<td>1</td>
<td>0/45</td>
<td>0/45</td>
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<td>SRFIC1521</td>
<td>VQFP48</td>
<td>AIZ</td>
<td>CEL9000N</td>
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<td>0/75</td>
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<tr>
<td>MC145159VF1</td>
<td>VMFP20</td>
<td>MHT</td>
<td>EME6300HE</td>
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<td>0/45</td>
<td></td>
<td>0.00</td>
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</table>

**TOTAL**: 91 5/4067 22/1197 0.67
FAILURE ANALYSIS

All failures are analyzed by Product Analysis Lab. In AIZU plant. After that, will be decide action items and schedule by discussion with all concerned organization members.

Failure Summary

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>MBG</th>
<th>WAFER FAB</th>
<th>WAFER PROCESS TECHNOLOGY</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC141627FT</td>
<td>CSG</td>
<td>TSC</td>
<td>0.8umDLM</td>
</tr>
<tr>
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<tr>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

HTOL 168hrs 2/90pcs failed.
One device failure caused by inner lead – 2nd neck or stitch – damage (CATS#196250A, 196252A).
Another one device failure caused is not cleared (CATS#197399A).

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>MBG</th>
<th>ASSY SITE</th>
<th>PACKAGE TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC141627FT</td>
<td>CSG</td>
<td>AIZ</td>
<td>LQFP48 (CEL9200N)</td>
</tr>
<tr>
<td></td>
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<tr>
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</tr>
<tr>
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<td></td>
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</tr>
</tbody>
</table>

T/C 100cyc 5/90pcs, 1000cyc 19/85pcs failed.
All failure caused by inner lead – 2nd neck or stitch – damage (CATS#196250A, 196252A, 198882A, 204066A).

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>MBG</th>
<th>ASSY SITE</th>
<th>PACKAGE TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC44200FT</td>
<td>CSG</td>
<td>AIZ</td>
<td>LQFP44 (CEL9200N)</td>
</tr>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

T/C 1000cyc 3/90pcs failed.
Two device failure caused by inner lead – 2nd neck – damage (CATS#206363A).
Another one device failure caused is not cleared (CATS#210915A).

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>MBG</th>
<th>ASSY SITE</th>
<th>PACKAGE TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MMQF2N06VL</td>
<td>SCG</td>
<td>AIZ</td>
<td>MFP20 (EME5000LS)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AUTOCLAVE 96hrs 2/45pcs failed.
All failure caused by pad corrosion (CATS#184813A).

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>MBG</th>
<th>ASSY SITE</th>
<th>PACKAGE TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LS244N</td>
<td>SCG</td>
<td>AIZ</td>
<td>PDIP20 (ST10F)</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AUTOCLAVE 96hrs 1/45pcs failed.
Failure caused by pad corrosion (CATS#204082A).
Section 3
Hong Kong, Malaysia, U.S. Monitor Centers

Prepared by Andrea Musat
e-mail: ra0857@email.sps.mot.com

This section included data obtained through Hong Kong reliability center from Sam-Cheung and the KLM reliability center from Said Nazri.

- Device Cross Reference Table
- FITs Level by Technology
- Reliability Data by Package
- Reliability Data by Device
- Failure Analysis
### Device Cross Reference Table

**Imaging and Entertainment Solutions**  
(formerly Imaging Systems Division)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Mask</th>
<th>Fab Site</th>
<th>Design Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>414256</td>
<td>G78K</td>
<td>MOS 10</td>
<td>0.65μ DLM</td>
</tr>
<tr>
<td>414277</td>
<td>G61B</td>
<td>MOS8</td>
<td>0.65μ TLM</td>
</tr>
<tr>
<td>414294</td>
<td>G85K</td>
<td>MOS8</td>
<td>0.65μ TLM</td>
</tr>
<tr>
<td>414339</td>
<td>G97K</td>
<td>MOS8</td>
<td>0.65μ TLM</td>
</tr>
<tr>
<td>414355</td>
<td>J21C</td>
<td>MS11</td>
<td>0.42μ TLM</td>
</tr>
<tr>
<td>414361</td>
<td>H18H</td>
<td>MS11</td>
<td>0.42μ TLM</td>
</tr>
<tr>
<td>414362</td>
<td>H11H</td>
<td>MOS8</td>
<td>0.65μ TLM</td>
</tr>
<tr>
<td>414379</td>
<td>J89C</td>
<td>TSC8</td>
<td>0.65μ TLM</td>
</tr>
<tr>
<td>56004</td>
<td>H70G</td>
<td>MOS10</td>
<td>0.65μ DLM</td>
</tr>
<tr>
<td>56007</td>
<td>J52E</td>
<td>TSC8</td>
<td>0.65μ DLM</td>
</tr>
<tr>
<td>56009</td>
<td>J89E</td>
<td>TSC8</td>
<td>0.55μ DLM</td>
</tr>
<tr>
<td>56009</td>
<td>H30H</td>
<td>MOS10</td>
<td>0.65μ DLM</td>
</tr>
<tr>
<td>56012</td>
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<td>0.55μ DLM</td>
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<tr>
<td>56362</td>
<td>H76G</td>
<td>MOS 13</td>
<td>0.34μ TLM</td>
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</table>

**Networking & Computing Systems Group**  
(Many products moved to this group from Imaging Systems Division in 4Q98)

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>5204</td>
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<tr>
<td>5204</td>
<td>H14N</td>
<td>MOS13</td>
<td>0.34μ TLM</td>
</tr>
<tr>
<td>5206</td>
<td>G10J</td>
<td>MOS8</td>
<td>0.65μ TLM</td>
</tr>
<tr>
<td>5206e</td>
<td>J22G</td>
<td>MOS13</td>
<td>0.34μ TLM</td>
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<tr>
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<td>H39G</td>
<td>MOS13</td>
<td>0.42μ TLM</td>
</tr>
<tr>
<td>5307</td>
<td>H55J</td>
<td>MOS13</td>
<td>0.34μ TLM</td>
</tr>
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<td>56301</td>
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<td>MOS13</td>
<td>0.34μ TLM</td>
</tr>
<tr>
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<td>0.42μ TLM</td>
</tr>
<tr>
<td>68HC000/1</td>
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</tr>
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<td>0.8μ DLM</td>
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<td>0.65μ DLM</td>
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<td>0.65μ DLM</td>
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<td>TSC</td>
<td>1.0μ SLM</td>
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<td>E13G</td>
<td>TSC</td>
<td>1.0μ DLM</td>
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<td>F91C</td>
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<td>1.0μ SLM</td>
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<td>0.42μ TLM</td>
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<tr>
<td>68302</td>
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<td>0.65μ DLM</td>
</tr>
<tr>
<td>Component</td>
<td>Device</td>
<td>Package</td>
<td>Technology</td>
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<td>G58E</td>
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</tr>
<tr>
<td>68328</td>
<td>H58B</td>
<td>MOS8</td>
<td>0.65 μm</td>
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<tr>
<td>68328</td>
<td>H51K</td>
<td>TSC</td>
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<td>68332 (TSG)</td>
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<td>0.65 μm</td>
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<td>823/850</td>
<td>H89G</td>
<td>MOS11</td>
<td>0.34 μm</td>
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<td>860</td>
<td>J24A</td>
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<tr>
<td>860</td>
<td>F84C</td>
<td>MOS11</td>
<td>0.5 μm</td>
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</tbody>
</table>
Reliability Audit Program (RAP) Results

(I) High Temperature Operating Life Test's FITs
Level by Technology:
(This section includes results from the last one year of monitor testing for each fabrication process family. Individual device data is shown in Part-3.)

<table>
<thead>
<tr>
<th>Process Family</th>
<th>Readpoints</th>
<th>Total Device Hours *</th>
<th>FIT Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># Failures / Sample Size</td>
<td>24 Hrs</td>
<td>168 Hrs</td>
</tr>
<tr>
<td>1.0-1.5µm</td>
<td>0/460 0/460 0/460 0/460</td>
<td>4.64e+05</td>
<td>932 FIT</td>
</tr>
<tr>
<td>0.7-0.8µm</td>
<td>0/1270 1/790 0/602 0/437</td>
<td>5.67e+05</td>
<td>329 FIT</td>
</tr>
<tr>
<td>0.65µm</td>
<td>0/1416 2/1416 0/1163 0/950</td>
<td>1.11e+06</td>
<td>356 FIT</td>
</tr>
<tr>
<td>0.3 -0.55µm</td>
<td>15/3827 2/3033 1/2579</td>
<td>2.96e+06</td>
<td>975 FIT</td>
</tr>
</tbody>
</table>

* As production of older technologies ramps down, the total device hours collected during monitor testing is reduced, thus resulting in an increased FIT rate (particularly when device hours are less than 1E6).

The fit rate for the 0.3 - 0.55µm technology is particularly higher than previous quarter's data due to the performance of one particular part in one fab. Corrective actions are being pursued. Excluding this part from the analysis, FIT is 119 at 60% C.L. and 437 at 90% C.L.
1.0µ-1.5µ Process Family Failure Rate Trends

Early Life Failure Rate Trend (PPM)

Intrinsic Failure Rate Trend (FITs)

Failure Rate as a Function of Operating Temperature
0.7µ-0.8µ Process Family Failure Rate Trends

Early Life Failure Rate Trend (PPM)

Intrinsic Failure Rate Trend (FITs)

Failure Rate as a Function of Operating Temperature
Early Life Failure Rate Trend (PPM)

Intrinsic Failure Rate Trend (FITs)

Failure Rate as a Function of Operating Temperature
0.3μ-0.55 Process Family Failure Rate Trends

The fit rate for the 0.3 - 0.55μm technology is particularly higher than previous quarter's data due to the performance of one particular part in one fab. Corrective actions are being pursued. Excluding this part from the analysis, FIT is 119 at 60% C.L. and 437 at 90% C.L.
(II) Reliability Data by Package:

(Sample sizes and results in this section include the last one year of cumulated monitor data. Individual device data is shown in Part-3.)

**PQFP Reliability Test Data**

(Level-1 or Level-3 preconditioning is performed prior to these reliability stresses. Please see the individual device data for specific information.)

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Readpoints # Failures / Sample Size</th>
<th>% Failures</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature Cycling</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(-65°C/+150°C)</td>
<td>Precond 100 Cy 500 Cy 1000 Cy</td>
<td>0%</td>
</tr>
<tr>
<td></td>
<td>0/2086 0/2085 0/1480 0/981</td>
<td></td>
</tr>
<tr>
<td><strong>Temperature Humidity Bias</strong></td>
<td>Precond 168 Hrs 504 Hrs 1008 Hrs</td>
<td>0%</td>
</tr>
<tr>
<td>(85°C, 85%RH)</td>
<td>0/496 0/498 0/486 0/438</td>
<td></td>
</tr>
<tr>
<td><strong>Autoclave</strong></td>
<td>Precond 48 Hrs 144 Hrs</td>
<td>0.11%</td>
</tr>
<tr>
<td>(121°C, 100%RH, 15 psig)</td>
<td>0/1861 2/1861 0/1425</td>
<td></td>
</tr>
</tbody>
</table>

**TQFP Reliability Test Data**

(Level-1, Level-3, or Level-4 preconditioning is performed prior to these reliability stresses. Please see the individual device data for specific information.)

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Readpoints # Failures / Sample Size</th>
<th>% Failures</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature Cycling</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(-65°C/+150°C)</td>
<td>Precond 100 Cy 500 Cy 1000 Cy</td>
<td>0%</td>
</tr>
<tr>
<td></td>
<td>0/552 0/556 0/278 0/201</td>
<td></td>
</tr>
<tr>
<td><strong>Autoclave</strong></td>
<td>Precond 48 Hrs 144 Hrs</td>
<td>0%</td>
</tr>
<tr>
<td>(121°C, 100%RH, 15 psig)</td>
<td>0/231 0/231 0/231</td>
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</tr>
</tbody>
</table>
### CQFP Reliability Test Data

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Readpoints</th>
<th># Failures / Sample Size</th>
<th>% Failures</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Cycling</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(-65°C/+150°C)</td>
<td>100 Cy</td>
<td>0/360</td>
<td>0%</td>
</tr>
<tr>
<td></td>
<td>500 Cy</td>
<td>0/360</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1000 Cy</td>
<td>-</td>
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</tbody>
</table>

### PLCC Reliability Test Data

(Leve-3 preconditioning is performed prior to these reliability stresses.)

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Readpoints</th>
<th># Failures / Sample Size</th>
<th>% Failures</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Cycling</td>
<td>Precond</td>
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<td></td>
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| Autoclave                   | Precond    |                          |            |
| (121°C, 100%RH, 15 psig)    | 48 Hrs     | 0/820                    | 0%         |
|                             | 144 Hrs    | 0/820                    |            |

### CPGA Reliability Test Data

<table>
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<th>Readpoints</th>
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<th>% Failures</th>
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### (III) Reliability Data by Device

#### Life Test Data

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<td>LEVEL-3</td>
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<td>0 / 77</td>
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<tr>
<td>823/850</td>
<td>0.34</td>
<td>MS11</td>
<td>METL</td>
<td>ZT</td>
<td>9824</td>
<td>LEVEL-3</td>
<td>0 / 77</td>
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<td>823/850</td>
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<td>MS11</td>
<td>METL</td>
<td>ZT</td>
<td>9824</td>
<td>LEVEL-3</td>
<td>0 / 77</td>
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<tr>
<td>823/850</td>
<td>0.34</td>
<td>MS11</td>
<td>METL</td>
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<td>823/850</td>
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<td>METL</td>
<td>ZT</td>
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<td>0 / 77</td>
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<tr>
<td>860</td>
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<td>MS11</td>
<td>KLM</td>
<td>ZP</td>
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Summary of Failures

Reports on all failures, where the mechanism is identified, are sent to the organization responsible for the defect. In addition, the failure mechanism information is added to a computer database which allows signature analysis of failure mode. Mechanism summaries are created and discussed periodically with our manufacturing sites. Continuous improvement plans are required from all manufacturing sites.

<table>
<thead>
<tr>
<th>LOTNO</th>
<th>DEVICE</th>
<th>ASSY</th>
<th>TECH</th>
<th>FAB</th>
<th>QTY</th>
<th>READ PT/ FAILURE MODE/MECHANISM</th>
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<tr>
<td>125°C HIGH TEMPERATURE OPERATING LIFE (HTOL) TEST</td>
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<tr>
<td>Rel200008-01</td>
<td>68HC000</td>
<td>KLM</td>
<td>0.8</td>
<td>MS10</td>
<td>1</td>
<td>168hour/ Functional fail- F/A not completed</td>
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<tr>
<td>RelSB459021</td>
<td>68SEC000</td>
<td>KLM</td>
<td>0.65</td>
<td>MS10</td>
<td>1</td>
<td>168hour/ Short,Sagging wire</td>
</tr>
<tr>
<td>Rel200031-01</td>
<td>414362</td>
<td>SHC</td>
<td>0.65</td>
<td>MOS8</td>
<td>1</td>
<td>168 hour/ Bin 2 functional failure - unable to do F/A</td>
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<tr>
<td>Rel200044-01</td>
<td>5204</td>
<td>SHC</td>
<td>0.34</td>
<td>MS13</td>
<td>1</td>
<td>504 hour/ IDDQ failure- F/A not completed</td>
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<tr>
<td>Rel 134911-1</td>
<td>5204</td>
<td>SHC</td>
<td>0.34</td>
<td>MS13</td>
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<td>504 hour/ Scan failure confirmed in F/A as intermittent</td>
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<tr>
<td>Rel136207-1</td>
<td>56303</td>
<td>KLM</td>
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<td>MS11</td>
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<td>168 hour/ functional fail-recovered during liquid crystal</td>
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<tr>
<td>Rel136207-1</td>
<td>56303</td>
<td>KLM</td>
<td>0.42</td>
<td>MS11</td>
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<td>1008 hour/ Stop IDD @68Vt; unable to determine cause</td>
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<tr>
<td>Rel200027-03</td>
<td>68LC060</td>
<td>KLM</td>
<td>0.42</td>
<td>MS11</td>
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<td>168 hour/ Leakage - sample in F/A</td>
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<tr>
<td>Rel200043-1</td>
<td>56009</td>
<td>P1</td>
<td>0.55</td>
<td>TSC8</td>
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<td>168 hour/ ICC stop - F/A revealed no anomalies</td>
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<td>KBE855864</td>
<td>68EC060</td>
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<td>KBE863773</td>
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<td>168 hour/ functional failures due to gate oxide failure</td>
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TEMPERATURE CYCLING (T/C) TEST

<table>
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<tr>
<th>LOTNO</th>
<th>DEVICE</th>
<th>CLASS</th>
<th>ASSY</th>
<th>TECH</th>
<th>FAB</th>
<th>QTY</th>
<th>PKG</th>
<th>READ PT/ FAILURE MODE/MECHANISM</th>
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<tr>
<td>Rel134041-2</td>
<td>860</td>
<td>III</td>
<td>KLM</td>
<td>0.5</td>
<td>MS11</td>
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<td>ZP</td>
<td>1000 CYC/ Unknown</td>
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AUTOCLAVE (A/C) TEST

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<thead>
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<th>LOTNO</th>
<th>DEVICE</th>
<th>CLASS</th>
<th>ASSY</th>
<th>TECH</th>
<th>FAB</th>
<th>QTY</th>
<th>PKG</th>
<th>READ PT/ FAILURE MODE/MECHANISM</th>
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<tr>
<td>Rel200030-4</td>
<td>414294</td>
<td>III</td>
<td>ANAM</td>
<td>0.65</td>
<td>MOS8</td>
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<td>FT</td>
<td>48 HRS/ Unknown</td>
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<tr>
<td>Rel200095-2</td>
<td>823/850</td>
<td>III</td>
<td>METL</td>
<td>0.34</td>
<td>MS11</td>
<td>2</td>
<td>ZT</td>
<td>144 HRS/ 1 fails high freq clock, other lo freq EZ</td>
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</tbody>
</table>