A Guide to Designing with the GV7601 Aviia™ HD Receiver

Design Guide
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Overview
This document serves as a reference for designing with the GV7601 Aviia™ HD Receiver for HDcctv applications. This document contains two main areas of focus:

1. Considerations in the schematic design.
2. Recommended PCB layout practices when designing with the GV7601.

The figure below shows the features and the functions of the GV7601.

HDcctv Rx Block Diagram

1. Power

1.1 Power Supply
The GV7601 requires stable (+10%) power with low noise. Ideally, these voltages are provided by linear voltage regulators.

The GV7601 requires two voltages; +3.3V and +1.2V with optional +1.8V for the digital I/Os which can be powered either by +1.8V or +3.3V.

The +1.2V powers the digital core as well as the analog portions of the chip, such as the PLL components. The +3.3V powers the on-chip cable driver, serial digital input buffer, other sensitive analog circuitry and digital I/O. For optimal performance, it is essential that these supplies are isolated to avoid external noise coupling.

It is recommended to use separate power planes for those supplies, as well as two separate ground planes; one for analog and one for digital.

These supplies, together with an adjacent ground plane, can be broken down into four groups: +1.2V/AGND, +3.3V/AGND, +1.2V/GND and IO_VDD/GND. See Figure 1-1: GV7601 Power Supply Filtering and Decoupling.
The following guidelines are suggested when designing power for the GV7601:

- Use coupled power and ground planes i.e. use minimum spacing between power and ground planes. Power and ground planes form a natural capacitor, which will increase capacitance.
- Do not overlap power planes. If it is unavoidable, different power planes should be isolated from each other with the ground plane between them.
- Power and ground planes should be placed near the component side, which will reduce inductance of vias.
- If possible, use multiple vias to connect components to power supply.
- Use low ESL, low ESR capacitors.

Isolate the power plane and ground from the main plane in a 'moat'. Gennum recommends that power and ground connections to this 'island' be made through 0Ω resistors, which are decoupled on both sides. In the case where better filtering is required, 0Ω resistors can be replaced with an inductor or ferrite beads. Place at least 1μF capacitor on the entrance of the power plane. If possible, running high-speed traces across a moat should be avoided. See Figure 1-2.

1.2 Power Filtering and Decoupling

It is recommended to decouple each power supply pin with a 10nF capacitor. Decoupling capacitors should be connected between a power supply and the related ground, see Figure 1-2.
All decoupling and filtering ceramic capacitors should be placed as close as possible to the related pins of the GV7601. Please see Figure 1-1.

Ideally, the bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. See Figure 1-3.

![Power Filtering and Decoupling Diagram](image)

**Figure 1-3: Power Filtering and Decoupling**

For the power pins of the outside rows of a BGA, the decoupling capacitors should be placed on the top layer. For the power pins of the inner rows of a BGA, the decoupling capacitors can be placed on the bottom layer, close to the related power pin.

See Figure 1-1: GV7601 Power Supply Filtering and Decoupling for power decoupling and filtering.

### 1.2.1 1.2V Power Supply Considerations

The GV7601 is very sensitive to low-frequency supply noise on the 1.2V VCC and any noise will directly phase modulate the output.

Gennum recommends that separate decoupling capacitors and filtering ferrite beads are added on the 1.2V_A power supply to minimize noise coupled from the 1.2V core current.

For best performance, a separate regulator (linear) may be used for the 1.2V_A rail. While the GV7601 is not sensitive to latch-up, consideration must be given to power sequencing in this case.

Use local linear regulation whenever possible.

### 1.3 VCO Decoupling

To minimize jitter, it is particularly important to maintain low noise on the VCO power supply. It is recommended to connect VCO_VDD pin to the 1.2V analog power plane through the RC filter shown in Figure 1-4. The RC components should be placed as close as possible to the GV7601, and further away from noise sources.
2. Serial Digital Input and Output

2.1 Serial Digital Input

The GV7601 has one serial digital input, which accepts data rates of 270Mb/s, 1.485Gb/s and 2.97Gb/s. To meet HDcctv performance requirements, the GV7601 includes an integrated cable equalizer.

Special consideration must be paid to component layout when designing high-speed Serial Digital Interfaces. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note that the following PCB artwork features are used to optimize performance:

- PCB trace width for 1.485Gb/s signals is closely matched to SMT component width to minimize reflections due to change in trace impedance
- The PCB ground plane is removed under the GV7601 input compounds to minimize parasitic capacitance
- High-speed traces are curved to minimize impedance changes

The GV7601 circuit schematic is shown in Section 6., including the upstream communications channel. However, designs which do not require the upstream communications channel will need to use the simplified input schematic shown in Figure 2-1. The PCB layout of the serial digital input is shown in Figure 2-2, also without the upstream communications channel.
Figure 2-1: Serial Digital Input without Upstream Communications Channel

Figure 2-2: Layout without Upstream Communications Channel
2.2 Serial Digital Output

The serial digital input is equalized and re-timed, and sent to the loop-through outputs, SDO/SDI. These are differential signals with a 100Ω impedance. The serial digital output can be used for HDcctv repeater applications, where multiple runs of coaxial cable can be connected together using repeaters for long distance transmission. In order to meet HDcctv performance requirements, a cable driver is required. Gennum’s GV8500 is the recommended cable driver for use with the GV7601.

See Section 2.1 for high-speed signal layout recommended practices.

Termination of the SDO/SDO traces should be placed close as possible to the GV8500. See Figure 2-3.

![Figure 2-3: Termination of the SDO/SDO Traces](image)

Anti-pads also apply to the pull-up resistor for the RSET pin. Any impedance transition shall be avoided on these transmission lines. Running high-speed traces through vias should be avoided.

![Figure 2-4: Anti-pad for shunt component on transmission lines](image)

![Figure 2-5: Anti-pad for serial components on transmission lines](image)
2.3 Loop Filter and Bandgap Inputs

Figure 2-6 shows the recommended loop filter and bandgap components.

![Figure 2-6: Loop filter and bandgap components](image)

Since these are noise-sensitive inputs, place the components close to the GV7601, and avoid routing the other digital signals under them or close to them.

Table 2-1: LB_CONT Setting

<table>
<thead>
<tr>
<th>LB_CONT</th>
<th>Full HD</th>
<th>HD</th>
<th>SD</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>6</td>
<td>3</td>
<td>0.55</td>
<td>MHz</td>
</tr>
<tr>
<td>Floating</td>
<td>3</td>
<td>1.5</td>
<td>0.27</td>
<td>MHz</td>
</tr>
<tr>
<td>VCC</td>
<td>1.5</td>
<td>0.75</td>
<td>0.14</td>
<td>MHz</td>
</tr>
</tbody>
</table>

Since these are noise-sensitive inputs, place the components close to the GV7601, and avoid routing the other digital signals under them or close to them.
3. Upstream Communications Channel

3.1 HDcctv Communication Channel Overview

In addition to the high-speed (1.485Gb/s) serial digital video downstream channel, the Aviia solution provides for a bidirectional communication channel that supports full duplex data rates up to 10Mb/s. In order to implement this communication channel over a single coaxial cable, two technologies are being deployed.

1. The Downstream communication channel is multiplexed with the downstream serial digital video using the ancillary data space allocated to each video frame.

2. The Upstream communication channel is implemented using a frequency multiplexing technique over the same communication media (coax cable) as the main serial digital video channel. The Upstream channel digital data is encoded using a 4b/5b technique to be compatible with an AC-coupled communication channel.

For detailed implementation of the serial digital video and communication protocol please refer to the HDcctv standard.

3.2 Upstream Transmit Filter

In order to support a high speed upstream communication channel without affecting the high performance of the downstream serial digital video, the transmit band pass of the upstream channel is precisely shaped using a high quality Active Low Pass Filter (LPF). The block diagram of this module is presented in the Figure 3-1 below:

Figure 3-1: HDcctv Upstream Transmit Filter Block Diagram
The active filter is designed as a three-pole Butterworth low-pass filter, with a cut-off frequency of 7MHz and a pass-band gain of 1. The input stage into the active filter uses a LVC buffer to ensure that proper voltage swing levels are being applied to the input op amp stage.

The peak-to-peak voltage amplitude of the communication channel signal is 1V +/- 10%.

Coupling between the active filter output and transmission line is accomplished using a LPF ferrite that insures minimal interference between the high-speed and low-speed devices.

The single-pole passive High Pass Filters (HPF) at the input of the GS7601 device prevents the low frequency channel from interfering with the operation of the high-speed video channel.

Additionally, a proprietary crosstalk cancellation technique is used at the high-speed input of the serial digital video receiver device to further improve the signal integrity of the link.

### 3.3 Filter Layout Recommendations

In order to maximize efficiency of the active filter and prevent undesirable ripples, the filter circuitry is required to be grouped and located in a compact area of the board, providing good isolation from external noise sources like switchers and oscillators. The traces on the input and output of the op amps have to be routed with low parasitic capacitance and inductance, in such manner that the input and output signal paths are not being intertwined. The serial impedance matching resistors R21 and R22, illustrated in Figure 3-2 below, should be placed as close as possible to the output pin of the op amp U3.

![Figure 3-2: Output Section of the Upstream Communications Channel](image-url)
It is important that the L3 and L4 ferrites are placed as close as possible to the transmission lines that they couple into. Layout guidelines presented for the transmission line apply to L3 and L4, where it is recommended to open the ground plane underneath the ferrite devices, and place the coupling pad embedded into the transmission line to minimize impedance discontinuities.

4. Parallel Outputs (Clock and Data)

The GV7601 features an ITU-R BT.1120 parallel video output which operates at a pixel rate of 74.25MHz for a 20-bit wide bus, or 148.5MHz for a 10-bit multiplexed data bus.

The primary consideration with clock and I/O data, is to route them in a manner that reduces capacitive and inductive crosstalk, while maintaining equivalent lengths.

To get a reasonable timing margin, keep the routing lengths of the bus signals and synchronous signals to approximately the same length (<±0.5" tolerance).

If a 10-bit wide output is not required, or the length of the traces is not more than 2", trace length matching is not required.

To minimize the crosstalk, the clock traces must be at least 3x the trace width away from adjacent signals, or the clock trace can be isolated by low impedance reference (power or ground).

Try to avoid vias on the clock nets. Always use smooth-curving traces for all clock signals.

The digital outputs of the GV7601 (DOUT[19:0], PCLK and STAT[5:0]) have programmable drive strength. Serial termination resistors on these signals are not normally required when the traces are not very long and the signals are not going through a connector.
5. Digital Audio Output

The GV7601 audio outputs (AOUT1/2, AOUT3/4, AOUT5/6 and AOUT7/8) provide CMOS level S/PDIF or AES encoded outputs. The outputs can also be configured for I²S serial audio for device-to-device audio connectivity.

NOTE: For most applications, the GV7601 does not drive external audio interfaces. In order to connect to an external digital audio interface, a 5V differential cable driver is needed. See Figure 5-1 for the balanced AES, unbalanced AES and S/PDIF interfaces.

Figure 5-1: Balanced and Unbalanced Digital Audio Interfaces
6. GV7601 Schematic

Figure 6-1: GV7601 Schematic
7. HDcctv Repeater

The HDcctv repeater design utilizes the serial digital loop-through output of the GV7601, connected to a GV8500 Cable Driver, as shown in Figure 7-1 below.

Figure 7-1: HDcctv Repeater Schematic