A 50-MHz Multibit Sigma–Delta Modulator for 12-b 2-MHz A/D Conversion

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Abstract—Oversampling techniques offer several advantages for the implementation of high-resolution analog-to-digital (A/D) converters in VLSI technologies. This paper examines the application of oversampling techniques to A/D conversion at rates exceeding 1 MHz. A cascaded multibit sigma–delta (ΣΔ) modulator that substantially reduces the oversampling ratio required for 12-b conversion while avoiding stringent component matching requirements is introduced. Issues concerning the design and implementation of the modulator are presented. At a sampling rate of 50 MHz and an oversampling ratio of 24, an implementation of the modulator in a 1-μm CMOS technology achieves a dynamic range of 74 dB at a Nyquist conversion rate of 2.1 MHz. The experimental modulator is a fully differential circuit that operates from a single 5-V power supply and does not require calibration or component trimming.

I. INTRODUCTION

OVERSAMPLED analog-to-digital (A/D) converters based on sigma–delta (ΣΔ) modulation have previously been used for high-resolution signal acquisition in voice-band telecommunications, digital audio, and ISDN applications. In these applications, the use of oversampling techniques has resulted in robust implementations by exploiting the enhanced speed and circuit density of scaled VLSI technologies to overcome resolution limitations resulting from component mismatch and reduced supply voltages. This work examines the application of oversampling techniques to A/D conversion at rates exceeding 1 MHz with a resolution of 12 b or more. While Nyquist-rate converters are capable of achieving this level of performance in a CMOS technology using a pipelined architecture [1], there are several distinct advantages to using an oversampling approach. Oversampled A/D converters can achieve high resolution without trimming or calibration because of their tolerance for component mismatch and circuit nonidealities. These converters also simplify system integration by reducing the burden on the supporting analog circuitry. Specifically, they do not require precision sample-and-hold circuitry and they relax the performance requirements on the analog antialias filter that precedes the sampling operation. Oversampled A/D converters include an inherent digital filtering capability and their resolution versus conversion rate is easily tailored to allow use of the same converter in a variety of applications.

Increasing the conversion rate of an oversampled A/D converter may be accomplished by increasing the modulator sampling rate or decreasing the oversampling ratio, which is the ratio of the modulator sampling rate to the conversion rate. To achieve conversion rates above 1 MHz using CMOS switched-capacitor circuit techniques, it is advantageous to reduce the oversampling ratio below the range of 64 to 512 typically used in oversampling converters. For 12-b resolution, an oversampled A/D converter based on a second-order ΣΔ modulator [2] would require an oversampling ratio of 50 in an ideal implementation. In a practical implementation, an oversampling ratio of 64 or higher may be required to compensate for circuit nonidealities such as electronic noise. One method of reducing the oversampling ratio below that required for a second-order ΣΔ modulator is to increase the order of the noise shaping by including additional integrators in the modulator's forward path [3]. However, at low oversampling ratios the effectiveness of increasing the order of the modulator's noise shaping is significantly reduced. Moreover, the performance improvement is further reduced when gain factors less than unity are included in the modulator's forward path to improve stability.

Alternatively, the 1-b quantizer typically used in a ΣΔ modulator can be replaced by a multibit quantizer to increase the dynamic range (DR) according to

\[ DR \text{ Increase } = 20 \log (2^N - 1) \text{ dB} \] (1)

where \( N \) is the resolution of the multibit quantizer in bits. For example, when a 4-b quantizer is used instead of a 1-b quantizer, the quantization level spacing is reduced by a factor of 15 for constant outermost quantization levels, resulting in a dynamic range increase of nearly 24 dB. Note that the dynamic range improvement is independent of the oversampling ratio and is therefore particularly attractive in the present application. However, while modulators based on multibit quantization are tolerant of nonlinearity in the quantizer's analog-to-digital converter...
(ADC) because of noise shaping, they may impose stringent linearity requirements on the quantizer’s digital-to-analog converter (DAC). In these modulators, the error due to DAC nonlinearity effectively enters the modulator at its input. Therefore, the modulator’s linearity and resolution are limited by the precision of the multibit D/A converter. Section II introduces a cascaded multibit modulator that avoids the sensitivity to DAC precision. Issues concerning the implementation of this modulator are then addressed in Section III. The design of an experimental implementation is described in Section IV, and measurement results characterizing its performance are presented in Section V.

II. CASCaded MULTibit Sigma-Delta MODulator

The cascaded multibit modulator shown in Fig. 1 avoids sensitivity to the DAC precision by placing the multibit quantizer in the final stage of a third-order cascaded modulator. The more critical first-stage quantizer has only two analog output levels and is therefore inherently linear. The modulator consists of a second-order stage with a 1-b quantizer followed by a first-order stage with a multibit quantizer and is similar to a cascade of two stages with 1-b quantization proposed previously [4]. The input to the second stage is a weighted difference of the output and the input of the first-stage quantizer. When the coupling coefficients, \( \beta \) and \( \alpha \), are unity, the input to the second stage is the quantization error of the first stage. This cascaded modulator is more tolerant of imperfections in the circuits used for its implementation than a cascade of three first-order stages [5], [6], as will be discussed in Section III.

Fig. 2 shows a linear approximation of the modulator in Fig. 1 wherein the quantizers are modeled by signal-independent additive error sources, while the integrators are represented by their transfer functions in the z domain. \( E_1(z) \) and \( E_2(z) \) model the quantization error of the first and second-stage A/D converters, respectively. \( E_3(z) \) also contains a representation of nonlinearity in the sec-
second-stage A/D converter, and $E_D(z)$ models the error resulting from nonlinearity in the multibit D/A converter in the second stage. A corresponding error source does not appear in the first stage because of the inherent linearity of the 1-b D/A converter.

For the linearized model of Fig. 2, the $z$ transform of the output of the first-stage is

$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})^2 E_1(z).$$

(2)

Thus, the output of the first stage includes the input to the modulator delayed by one sample period plus the second-order difference of the first-stage quantization error $E_1(z)$. When $\alpha = \beta = 1$, the input to the second stage is $E_1(z)$ and the transform of the second-stage output is

$$Y_2(z) = z^{-1}(E_1(z) - E_D(z)) + (1 - z^{-1}) E_2(z).$$

(3)

The error cancellation logic combines the digital outputs from the two stages according to

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z)$$

so as to cancel the quantization error of the first stage.

The resulting output of the overall modulator is obtained by substituting (2) and (3) into (4):

$$Y(z) = z^{-2}X(z) + z^{-1}(1 - z^{-1})^2 E_D(z) - (1 - z^{-1})^3 E_2(z).$$

(5)

Thus, ideally the quantization error of the first stage is cancelled and the quantization error of the second stage is attenuated in the baseband by third-order shaping. As in a cascade of three first-order stages, third-order shaping is achieved without instability because the constituent stages are independently stable. Also, because the quantization error of the second stage originates from a multibit quantizer, the modulator’s dynamic range is improved according to (1).

In contrast to a single-stage multibit modulator, the error resulting from DAC nonlinearity, $E_D(z)$, does not enter this modulator at its input but instead is attenuated in the baseband by second-order shaping, as is evident in (5). The second-order shaping makes the cascaded multibit modulator much more tolerant of DAC nonlinearity than the single-stage modulator, as indicated in Fig. 3. This figure compares the simulated [7] baseband spectra for the modulator of Fig. 1 with that of third-order single-stage multibit modulator under the circumstance of 5-b DAC integral linearity. The spectrum for the single-stage modulator exhibits a substantially increased noise floor and harmonic distortion, while the spectrum of the cascaded modulator exhibits a noise floor only slightly higher than that resulting from an ideal DAC. More importantly, the cascaded modulator does not display any harmonic distortion, a consequence of the second-order shaping and the fact that the input to the second stage contains the quantization error of the first stage, which is substantially decorrelated from the input to the modulator.

Therefore, the cascaded multibit modulator is substantially decorrelated from the input to the modulator.

In Fig. 4 it is seen that the single-stage modulator achieves a 6-dB larger dynamic range for DAC linearity greater than 12 b. This is a consequence of a signal range reduction that must be performed in the cascaded modulator. With the coupling coefficients $\alpha$ and $\beta$ equal to unity, the input to the second stage is the entire quantization error of the first stage. The large amplitude of the quantization error produced by the second-order first stage would overload the input range of the second stage (which is the same as the input range of the first stage) and therefore must be attenuated by reducing $\alpha$ and $\beta$. When $\alpha$ and $\beta$ are reduced equally, the output of the second stage, $Y_2(z)$, must be digitally scaled by $\alpha^{-1}$ before the error cancellation logic described by (4) is performed. The resulting output of the modulator is then

$$Y(z) = z^{-2}X(z) + \alpha^{-1} \left[ z^{-1}(1 - z^{-1})^2 E_D(z) - (1 - z^{-1})^3 E_2(z) \right].$$

(6)
Note that both error terms increase because of the scaling of the second-stage output by $\alpha^{-1}$. This scaling is responsible for the 6-dB loss in dynamic range for DAC linearity exceeding 12 b seen in Fig. 4, where $\alpha = 0.5$. Note that it is advantageous to make $\alpha^{-1}$ a power of 2 so that the digital scaling may be implemented with a simple shift of bit significance.

It is not necessary that $\alpha$ equal $\beta$. When $\alpha$ is not equal to $\beta$, the input to the second stage is given by

$$Y_{z_2}(z) = (\beta - \alpha) Y_{z_1}(z) + \alpha E_t(z).$$

Thus a component of $Y_{z_1}(z)$ will be present in the output of the second stage, $Y_{z_2}(z)$. However, this component can be easily removed digitally prior to the error cancellation logic described in (4) by preprocessing the outputs of both stages according to

$$Y_{z_2p}(z) = \alpha^{-1} [Y_{z_2}(z) - z^{-1}(\beta - \alpha) Y_{z_1}(z)].$$

$Y_{z_2p}(z)$ takes the place of $Y_{z_2}(z)$ in (4) and the combined output of the modulator is given by (6). Again, it is useful to make $\alpha^{-1}$ and $(\beta - \alpha)$ powers of 2.

Suitable values of $\alpha$ and $\beta$ may be determined through simulation. Fig. 5 shows the simulated signal-to-(noise + distortion) ratio (SNDR) for three pairs of coupling coefficients. For input signals smaller than $-5$ dB, the SNDR is independent of $\beta$, consistent with its absence in (6). Therefore, $\beta$ may be optimized to constrain the signal range at the input to the second stage to allow the largest possible value of $\alpha$. It is evident that there are trade-offs between small-signal performance, large-signal performance, and hardware complexity. If $\alpha = 0.5$ and $\beta = 1$, the dynamic range is maximized. If $\alpha = 0.25$ and $\beta = 1$, the signal amplitude at which the SNDR begins to decrease is maximized. Finally, if $\alpha = 0.25$ and $\beta = 0$, the hardware complexity is reduced by eliminating the subtraction node at the input to the second stage.

Fig. 6 shows the simulated probability density functions at the input to the second stage for a $-5$-dB modulator input and the same three pairs of coupling coefficients considered in Fig. 5. A fairly even distribution is produced if $\alpha = 0.5$ and $\beta = 1$. Both the $\alpha = 0.5$, $\beta = 1$ and the $\alpha = 0.25$, $\beta = 0$ couplings result in small tails that extend beyond $\pm 0.5\Delta$, which defines the input range of both the first and second stages. For modulator inputs larger than $-5$ dB, these tails grow and result in the premature reduction in SNDR for increasing signal amplitudes seen in Fig. 5. Additional information concerning the selection of appropriate coupling coefficients is presented elsewhere [8].

III. IMPLEMENTATION

Fig. 7 shows a fully differential, switched-capacitor CMOS implementation of the cascaded multibit $\Sigma\Delta$ modulator. The first stage consists of two parasitic-insensitive integrators, a comparator that serves as the 1-b ADC, and a distributed two-level (1 b) DAC. The second stage consists of a single integrator, a 3-b flash ADC, and a 3-b differential DAC. The modulator operates on a two-phase nonoverlapping clock consisting of a sampling phase and an integration phase. During phase 1, the integrators sample their inputs by closing switches $S1$ and $S3$ and the first-stage comparator and second-stage ADC are strobed. The nodes labeled $V_{cm}$ set the common-mode input voltage of the fully differential operational amplifiers.
Switches $S_2$ and $S_4$ conduct during phase 2 to perform the subtraction and integration functions. Switches $S_3$ and $S_4$ are opened slightly ahead of switches $S_1$ and $S_2$, respectively, to reduce signal-dependent charge injection [9]. Note that the pipelined nature of this implementation reduces the critical path to one integrator delay per clock cycle.

Two modifications of the modulator in Fig. 1 are evident in Fig. 7. First, both integrators in the first stage include delays in their forward paths, as well as gain factors of $1/2$ at their inputs that are set by the ratio of their sampling and integrating capacitors. Thus, the transfer function of both first-stage integrators is

$$H(z) = \frac{z^{-1}}{2(1-z^{-1})}. \quad (9)$$

This configuration reduces the signal range required at the outputs of the first-stage integrators to about 1.5 times the modulator's input range, $\pm 0.5\Delta$ [10]. The output of the first stage given in (2) is changed only slightly to include an additional delay preceding $X(z)$.

The second modification present in Fig. 7 is that the input to the second stage is simply the differential output of the second integrator in the first stage. The combination of this simple coupling and the $1/2$ gain factors in the first-stage integrators implement $\alpha = 0.25$ and $\beta = 0$. In the experimental circuit presented in Section V, two additional sampling capacitors and additional switches were included in the second-stage integrator, as shown in Fig. 8, to allow selection among the three pairs of coupling coefficients listed in Fig. 5. The nodes labeled $V_{cmo}$ in Fig. 8(b) are biased at the reference voltage used to establish the common-mode output level of the operational amplifiers.

The performance of cascaded modulators is typically more sensitive to circuit nonidealities than single-stage modulators because of the absence of feedback around the entire modulator. The cancellation of the first-stage quantization error depends on the noise shaping specified in (2) precisely matching the shaping performed in the error cancellation logic. In practical implementations the first-stage noise shaping deviates from that given in (2) because of circuit nonidealities such as capacitor mismatch and the finite dc gain and bandwidth of operational amplifiers. As a result, the quantization error of the first stage is not completely cancelled, and it degrades the modulator's performance. However, the modulator of Fig. 1 has an advantage over a cascade of three first-order stages [5], [6] in that uncancelled quantization error from the first stage is attenuated in the baseband by second-order shaping rather than only first-order shaping [8]. The sensitivity to first-stage error leakage is further reduced in the present application because of the reduced oversampling ratio. The difference between second and third-order shaping is reduced at low oversampling ratios. Thus, the impact of the uncancelled second-order shaped error from the first stage is not as great as at higher oversampling ratios.

The expected magnitude of the uncancelled quantization error from the first stage influences the resolution chosen for the multibit quantizer in the second-stage. In an ideal implementation, the multibit quantizer resolution
Fig. 8. Configuration of the second-stage integrator for (a) \( \alpha = 0.5, \beta = 1 \); and (b) \( \alpha = 0.25, \beta = 1 \).

can be increased indefinitely to improve the dynamic range according to (1). However, in a practical implementation, increasing the resolution of the multibit quantizer reduces the second-stage quantization error and thereby increases the sensitivity to uncancelled quantization error from the first stage. Fig. 9 presents analytical results derived using the linear model of Fig. 2 [11], as well as supporting simulation results, that provide a basis for choosing the resolution of the second-stage multibit quantizer. With the quantizer resolution as a parameter, the increase in dynamic range provided by the second stage relative to the first stage is plotted as a function of the error in the 1/2 gain factors in the first-stage integrators. For example, the second-order first stage provides a dynamic range of 49 dB at an oversampling ratio of 16. A second stage with a 3-b quantizer increases the dynamic range of the modulator by 26 dB when the error in the ratio of the sampling and integrating capacitor sizes is 2%.

Several observations can be made concerning the results shown in Fig. 9. Increasing the resolution of the multibit quantizer increases both the dynamic range and the sensitivity to gain error. At increasing levels of gain error, the performance of the modulator becomes dominated by uncancelled first-stage quantization error and less benefit is derived from increasing the second-stage quantizer resolution. The use of a 1-b quantizer in the second stage as reported previously [4], [12] increases the dynamic range by less than 10 dB at low oversampling ratios but results in a large tolerance for gain error. The use of a multibit second stage provides a means of trading some of this tolerance for increased dynamic range without imposing strict constraints on the precision of the multibit D/A converter. Thus, a designer can tailor the modulator to the expected capacitor matching of the fabrication process.

A 2% gain error tolerance was selected to ensure a robust implementation of the modulator in the present work. While this tolerance may be larger than required by capacitor matching considerations, it eases the requirements on other circuit nonidealities, such as incomplete linear settling of the integrator outputs. At a gain error of 2%, the benefit of a 4-b over a 3-b quantizer is approximately 4.5 dB and does not justify doubling the size and loading of the second-stage quantizer. Hence, as indicated in Fig. 7, a 3-b quantizer was chosen for the second stage. At higher oversampling ratios the performance of a cascaded modulator is more sensitive to uncancelled quantization error from the first stage and the additional tolerance provided by a 1-b second-stage quantizer may be required. Thus, the use of multibit quantization in the second stage is most attractive at low oversampling ratios.

The performance of a cascaded modulator may also be degraded by integrator leakage resulting from the finite dc gain of the operational amplifiers. The transfer function of a leaky integrator is given by

\[
H(z) = \frac{1}{1 - (1 - A_{dc}^{-1})z^{-1}} \tag{10}
\]

where \( A_{dc} = H(1) \) is the dc gain of the operational amplifier. For this case the transform of the output of the first
stage given in (2) becomes approximately
\[ Y(z) = z^{-1}X(z) + \left[ (1 - z^{-1})^2 + 2A_d z^{-1}(1 - z^{-1}) + A_d^2 z^{-2} \right] E_1(z). \] (11)
The first term in the bracket is cancelled by the error cancellation logic. However, the second and third terms are not cancelled and result in first-order shaped and unshaped quantization error appearing at the combined modulator output \( Y(z) \). The first-order shaped error is inversely proportional to \( A_d \), while the unshaped error is inversely proportional to the square of \( A_d \). The resulting baseband quantization error power, relative to the power of a sine wave with a peak-to-peak amplitude of \( A \), is given by
\[ S_p = S_{p0} + \frac{8\pi^2}{9M^2A_d^2} + \frac{2}{3MA_d^2} \] (12)
where \( S_{p0} \) is the nominal baseband error power with infinite dc gain. For typical dc gain values and oversampling ratios, the contribution of the unshaped error represented by the last term in (12) is negligible.

Fig. 10 shows the dependence of the baseband error power on operational amplifier dc gain, simulations indicate that the second-stage quantization error is free from discrete noise tones. The second-order first stage can produce tones as strong as 52 dB below full scale at an oversampling ratio of 16 [13]. In the absence of integrator gain error and leakage, the tones are cancelled. In the presence of 1% and 2% gain errors, the tones are reduced by 40 and 34 dB, respectively. An operational amplifier dc gain of 60 dB results in tones that are 91 dB below full scale.

IV. CIRCUIT DESIGN

The cascaded multibit \( \Sigma \Delta \) modulator depicted in Fig. 7 has been designed for fabrication in a 1-\( \mu \)m CMOS VLSI technology with the goal of verifying experimentally the aforementioned attributes of this modulator. The performance objective was a Nyquist conversion rate greater than 1 MHz and a dynamic range of 12 b while operating from a single 5-V power supply.

The operational amplifier used in the integrators is the most critical element of the modulator. Simulations indicate that the signal range required at the output of the second-stage integrator is less than that needed in the first-stage integrators. Approximately 60 dB of dc gain is required to prevent performance degradation. This gain is lower than required for a cascade of three first-order stages, wherein unshaped first-stage quantization error inversely proportional to the dc gain is leaked to the output of the modulator [6].

Cascaded modulators are susceptible to the appearance of discrete noise tones in their output when the first-stage quantization error is not entirely cancelled by integrator gain error or leakage [13]. These tones arise from repetitive patterns that occur in the first-stage quantization error for certain modulator inputs [14]. In an ideal cascaded modulator, the first-stage quantization error, including the tones, is cancelled. Moreover, while quantizer overload has prevented an exact analysis of the cascade of a second-order and a first-order stage [15],
changes in the common-mode output are coupled to node $A$, which returns the common-mode output voltage to the desired level through negative feedback. During phase 1, corrective charges are transferred onto $C1$ and $C2$ from refresh capacitors to prevent drift in the common-mode output voltage.

The performance of the modulator is relatively insensitive to offset and hysteresis in the first-stage comparator because the effects of these impairments are attenuated in the baseband by second-order noise shaping. A fast regenerative latch [17] without preamplification, as described in [13], has been used to implement the first-stage comparator. The modulator performance is also very tolerant of nonlinearity and hysteresis in the second-stage 3-b A/D converter because their effects are attenuated in the baseband by third-order noise shaping. The design of this A/D converter is complicated by the fact that it must compare the differential output voltage of the second-stage integrator to seven differential reference voltages. This is accomplished by charging seven pairs of capacitors to unique differential voltages derived from a reference resistor string during phase 1, as shown in Fig. 12 [18]. During phase 2, the left sides of the capacitors are driven by the outputs of the second-stage integrator. Seven regenerative latches of the same type used for the first-stage comparator are strobed at the end of phase 2 to perform the 3-b conversion. In the actual implementation, source followers are placed at the outputs of the second-stage integrator to buffer the loading resulting from the seven comparators. Equivalent buffers are placed between the comparator and the comparators to compensate for gain error and nonlinearity introduced by the source followers.

The modulator’s tolerance of nonlinearity in the second-stage 3-b DAC permits the use of a simple differential tapped resistor string for its implementation, as is also illustrated in Fig. 12. A 1-out-of-8 code produced by the AND gates in the 3-b flash ADC selects the proper pair of taps from the resistor string. The 1-out-of-8 code is also converted into the 3-b binary output of the second stage by simple encoding circuitry (not shown).

V. EXPERIMENTAL RESULTS

The cascaded multibit $\Sigma\Delta$ modulator has been fabricated in a 1-µm CMOS technology with metal-to-polycide capacitors and polysilicon resistors [19]. Fig. 13 is a die photograph of the modulator, which has an area of 0.65 mm² and operates from a single 5-V supply with a power dissipation of 41 mW.

The performance of the modulator was evaluated by driving its input with a high-quality differential sinusoidal signal source [20], acquiring the digital outputs from the first and second stages, and transferring the acquired data to a workstation for processing. A simple digital logic required to cancel the quantization error of the first stage, as well as decimation filtering and signal analysis, were performed on a workstation with the same software used for simulations of the modulator [7]. Performance metrics such as SNDR were determined using the sinusoidal minimum error method [21].
Fig. 13. Die photograph of the cascaded multibit ΣΔ modulator.

Fig. 14. Measured SNDR for a 1-MHz baseband.

Fig. 15. Measured baseband spectrum.

Fig. 14 shows the measured SNDR as a function of the input sine-wave amplitude. An input level of 0 dB represents a sine wave whose peak-to-peak amplitude equals the input range of the modulator Δ, which is 3 V (differential) in this implementation. The frequency of the input sine wave was 100 kHz and the modulator sampling rate was 50 MHz, which produced a 2.1-MHz Nyquist conversion rate at an oversampling ratio of 24. The modulator achieves a 74-dB dynamic range and a peak SNDR of 69 dB.

The measured baseband spectrum for a 100-kHz sine-wave input, obtained from a 4096-point fast Fourier transform, is shown in Fig. 15. The small second and third harmonic components present in the spectrum also appear in the output spectrum of the first stage and are therefore not attributable to nonlinearity in the multibit D/A converter in the second stage. The linearity of the metal-to-polycide capacitors was far better than required in this application, as established earlier [13]. The noise floor is higher than predicted from thermal noise generated by the sampling switches onto the 200-fF sampling capacitors in the first integrator. The noise floor is also higher than calculated for thermal and flicker noise in the operational amplifiers. Quantization noise limitations alone should allow a dynamic range exceeding 80 dB at an oversampling ratio of 24.

Both the noise floor and the harmonic distortion were quite sensitive to changes in package and test board features such as the grounding configuration, the location of decoupling capacitors, and the loading on the output pins. A second generation of the test board, designed around a leadless chip carrier instead of a 40-pin DIP, extended the sampling rate from 36 to 50 MHz. There was also strong evidence of substrate coupling from the output pad drivers to the modulator. On-chip circuitry performed a serial-to-parallel conversion to slow the output data rate by a factor of 4. However, this increased the number of output pad drivers from four to 16. The voltage swing of these CMOS drivers had to be reduced to 1.5 V to minimize the coupling to the sensitive analog circuitry.

As mentioned previously, the experimental modulator was designed to allow selection among the three pairs of coupling coefficients listed in Fig. 5. Experimentally, there was less than a 2-dB difference in dynamic range among the three pairs of coupling coefficients because the modulator's performance was not limited by quantization noise. The results presented in Figs. 14 and 15 were obtained for α = 0.25 and β = 0 since this coupling eliminates the need for the subtraction node at the input of the second stage.

The performance of the modulator degrades above a sampling rate of 50 MHz principally because of incomplete settling of the integrator outputs. At 50 MHz, the integrator outputs have about 3.5 time constants in which to settle. This is equivalent to a gain error of 3% if the settling is linear. Thus, at sampling rates above 50 MHz, it is expected that the quantization noise will increase and surpass the noise due to packaging and substrate cou-
pling. The frequency of the sine-wave input was limited to 100 kHz by the signal generator.

Key performance parameters for the modulator and the operational amplifier are summarized in Tables I and II, respectively. The operational amplifier performance measurements were obtained from isolated test structures. Measurements of the unity-gain frequency, slew rate, and settling time constant were obtained using low-capacitance active probes [22].

VI. CONCLUSION

The implementation of CMOS oversampling A/D converters with conversion rates exceeding 1 MHz is facilitated by lowering the oversampling ratio. $\Delta\Sigma$ modulators based on multibit quantization are particularly attractive at low oversampling ratios, but they may impose stringent linearity requirements on DAC linearity. The cascaded multibit modulator presented here avoids the dependence on DAC linearity by placing the multibit quantizer in the second stage, where the effects of DAC nonlinearity are attenuated by second-order noise shaping.

An experimental implementation of the proposed modulator has demonstrated that oversampling analog-to-digital converters can achieve 12-b resolution at conversion rates exceeding 2 MHz in a 1-$\mu$m CMOS technology. The advantages of using an oversampling approach are evident in this modulator's ability to achieve 12-b resolution without requiring more than 6-b precision in any of the analog circuit components. While the sampling rate of the modulator is limited by the settling of the integrator outputs, the resolution of the modulator could possibly be extended through improved packaging and test fixturing as well as better isolation techniques to reduce substrate coupling.

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REFERENCES


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