QN8035
Design Guide and Application Note

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Agenda:

- QN8035 Features
- QN8035 Performance Summary
- QN8035 Hardware Design
- QN8035 Software Programming Guide
- QN8035 EVB Schematic
- QN8035 Related Document and Support
QN8035 Features

Features Changing ---comparing with QN8025

- **FM Band**: 60MHz to 108MHz
- **Clock source**: supports external clock only. Support 32.768KHz and greater than and equal to 1MHz clock injection
- **PIN Assignment**: No CEN, VIO, XTAL pins
- **Package**: QFN16 (2.5x2.5mm) and MSOP10 (3x3mm)
- **VCC**: Integrated LDO, and supports 2.7V to 5V supply
- **Volume Control**: Audio gain : -47 dB to 0 dB, attenuation only.
- **Audio Driver**: Supports 32Ω load only (Vout=1Vpp, THD=0.05%)
- **INT**: Needs a pull-up resistor to output high level.
- **RFI**: Integrates *Cap-bank tuning* to improve sensitivity.
QN8035 Performance Summary

<table>
<thead>
<tr>
<th>Function and Performance</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX_Current</td>
<td>12.6mA (Typical)</td>
</tr>
<tr>
<td>RX_Current (standby)</td>
<td>50uA (room temperature) 130uA (85°C)</td>
</tr>
<tr>
<td>RX_Current (Idle)</td>
<td>643uA</td>
</tr>
<tr>
<td>RX_SNR</td>
<td>64dB (stereo)</td>
</tr>
<tr>
<td></td>
<td>57dB (Mono)</td>
</tr>
<tr>
<td>RX_THD</td>
<td>0.03% (stereo)</td>
</tr>
<tr>
<td></td>
<td>0.04% (mono)</td>
</tr>
<tr>
<td>RX_L/R Separation</td>
<td>40dB</td>
</tr>
<tr>
<td>RX_Sensitivity</td>
<td>-114dBm with matching network and enable cap-bank tuning</td>
</tr>
<tr>
<td>RDS_Sensitivity</td>
<td>-98dBm with matching network and enable cap-bank tuning</td>
</tr>
<tr>
<td>RX_AGC</td>
<td>OK</td>
</tr>
<tr>
<td>RX_Stereo/Mono Switch</td>
<td>Ok</td>
</tr>
<tr>
<td>RX_AUDIO Mute</td>
<td>OK</td>
</tr>
</tbody>
</table>
## QN8035 Performance Summary

<table>
<thead>
<tr>
<th>Function and Performance</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Audio Volume Control (Analog)</td>
<td>6dB attenuation</td>
</tr>
<tr>
<td>Audio Volume Control (Digital)</td>
<td>1dB adjustment</td>
</tr>
<tr>
<td>De-emphasis</td>
<td>75μs, 50μs support</td>
</tr>
<tr>
<td>Clock Frequency Support</td>
<td>Supports 32.768KHz and greater than and equal to 1MHz</td>
</tr>
<tr>
<td>External Clock Input</td>
<td>Supports three kinds of external clock input,</td>
</tr>
<tr>
<td>RX_CCA</td>
<td>After software patch, chip will work normally.</td>
</tr>
<tr>
<td>RX_CCA_Interrupt</td>
<td>OK</td>
</tr>
<tr>
<td>RX_RDS</td>
<td>OK</td>
</tr>
<tr>
<td>RX_RDS_Interrupt</td>
<td>OK</td>
</tr>
<tr>
<td>RX_1KHz Tone Output</td>
<td>OK</td>
</tr>
<tr>
<td>Input IP3</td>
<td>(102dBuV) (88.1MHz)</td>
</tr>
<tr>
<td>AM Suppression</td>
<td>86dB (88.1MHz)</td>
</tr>
<tr>
<td>Adjacent /Alternate channel Selectivity</td>
<td>48.4dB/200KHz  54dB/400KHz (88.1MHz)</td>
</tr>
<tr>
<td>Pilot Rejection</td>
<td>44.2 dB (Relative to Pilot) 64.9dB (Relative to 75KHz)</td>
</tr>
<tr>
<td>Audio Output Voltage</td>
<td>100mV rms (FM deviation = 22.5k, VOL_CTL[5:0]=0x07)</td>
</tr>
</tbody>
</table>

**Note:** all upper data are tested at 88MHz
QN8035-Hardware Design

QN8035-NCNA Reference Schematic

Cap-bank Inductor for improving antenna efficiency

! INT must have a pull-up resistor to output

Directly drive 32 ohm load
QN8035-SANA Reference Schematic

Cap-bank Inductor for improving antenna efficiency

Directly drive 32 ohm load

INT must have a pull-up resistor to output

Audio Driver

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QN8035 Hardware Design

- **Power Supply:** QN8035 provides integrated voltage regulator, and typical application is one decoupling capacitor (0.1uF) and one by-pass (10uF) capacitor.
- **Clock Selection and Setting:** (Refer to chapter 5.3 on datasheet for details)
  - Clock Frequency: Supports 32.768KHz and greater than and equal to 1MHz.
  - Clock Input: Supports two types of input clock waveforms (single ended and digital clock).
  - XTAL Setting: \( \text{XTAL\_DIV}[10:0] = \text{Round}(\text{Freq_xtal}/32.768\text{KHz}) \), then write \( \text{XTAL\_DIV}[10:0] \) to Reg15h and Reg16[2:0]. Default is 32.768KHz. Frequency of clock, i.e. 32768
  - PLL Configuration: \( \text{PLL\_DLT}[12:0] = \text{Round}(14.592\text{GHz}/(\text{Freq_xtal}/\text{XTAL\_DIV}[10:0]))-442368 \) Frequency of clock, i.e. 32768

Write PLL\_DLT[12:0] into Reg16h[7:2] and Reg17h. Note: default are for 32.768KHz clock input.
- **Audio Interface:** 1. When driver 32Ω load, don’t need external audio driver. When driver no 32Ω load, needs external driver for best performance.

![Audio Interface Diagram](image-url)
QN8035 Hardware Design

- **Antenna:** Three ferrite beads are used to prevent interference of FM signal with audio signal. A typical ferrite bead value is about 2.5K@100MHz.
- **RFI:** A 330nH // 100pF LC series matching for cap-tuning for best sensitivity.
- **Hardware Interrupt:** Generate an interrupt signal to a MCU during auto seek or RDS reception, in order to relieve the MCU from continuous polling on QN8035’s registers.

![Diagram of interrupt signal](image)

INT 4.55ms
Audio out traces should be also far away from high frequency interference source and digital interference source and the two traces should be as short as possible. The two traces should be shield by ground.

RFI trace must be shielded by ground for best EMC. Especially in cell phone system, RFI should far away all kinds interference.

AGND, GND and middle expose pad should be connected together on surface layer and the middle expose pads should have sufficient ground connection.

The distance of between SDA and SCL traces should be far enough and the two traces should be also far away from QN8035. The two pull-up resistors of I2C should be placed from QN8035 as far as possible. Make I2C trace as short as possible.
I2C Communication Protocol

**I2C Write Operation**

1. Start I2C
2. slave Address R/W
3. Base Address
4. ACK by QN8035
5. QN8035
6. Data Byte 1
7. ACK by QN8025
8. QN8025
9. Data Byte 2
10. ACK by QN8035
11. QN8035
12. Data Byte 3
13. ACK by QN8025
14. QN8025
15. Data Byte n
16. ACK by QN8025
17. QN8025
18. Stop

**I2C Read Operation**

1. Start I2C
2. slave Address R/W
3. Base Address
4. ACK by QN8035
5. QN8035
6. Data Byte 1
7. ACK by micro
8. micro
9. Data Byte 2
10. ACK by QN8025
11. QN8025
12. Data Byte 3
13. ACK by micro
14. micro
15. Data Byte n
16. ACK by micro
17. micro
18. Stop

**Note:**
- **Write Address:** 0x20
- **Read Address:** 0x21

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QN8035 Software Programming Guide
I2C Communication Protocol

I2C Write Data Protocol

I2C Read Data Protocol

From master to slave  \[\text{Ack} = \text{acknowledge (SDA LOW)}\]

From slave to master  \[\text{Ack} = \text{not acknowledge (SDA HIGH)}\]
QN8035 System Initialization

Start

Hardware Connection

Power Up

Software Reset
Write 0x81 to Reg00h

Delay 10ms

1. Clock Type Selection
   (Sine-wave or Digital-wave injection)
   Write corresponding data to Reg01h[7]

2. Clock Frequency Selection
   (32.768KHz or other frequencies clock)
   Write corresponding data to Reg15h and Reg16h

3. PLL Configuration
   Write corresponding data to Reg16h to Reg17h

Software Initialization

End

Note: All registers address are hex

Clock Type Selection

① Input clock is sine wave, set Reg01h[7] bit low
   Input clock is digital wave, set Reg01h[7] bit high
QN8035 Software Programming Guide

QN8035 System Initialization

Start

Hardware Connection

Power Up

Software Reset
Write 0x81 to Reg00h

Delay 10ms

Clock Type Selection
(Sine-wave or Digital-wave injection)
Write corresponding data to Reg01h[7]

Clock Frequency Selection
(32.768KHz or other frequencies, clock)
Write corresponding data to Reg15h and Reg16h

PLl Configuration
Write corresponding data to Reg16h to Reg17h

Software Initialization

End

Note: All registers address are hex

Clock Frequency Selection

② XTAL_DIV[10:0] =Round(Freqxtal /32.768KHz)
Write hex result XTAL_DIV[10:0] into Reg15h and Reg16h[2:0]
Note: default values of Reg16h and Reg17h are for 32.768KHz clock input.
QN8035 System Initialization

1. Start
   - Hardware Connection
   - Power Up
   - Software Reset
     Write 0x81 to Reg00h
   - Delay 10ms

2. Clock Type Selection
   (Sine-wave or Digital-wave injection)
   Write corresponding data to Reg01h[7]

3. Clock Frequency Selection
   (32.768KHz or other frequencies clock)
   Write corresponding data to Reg15h and Reg16h

PLL Configuration

   Write PLL_DLT[12:0] into Reg16h[7:3] and Reg17h.
   Note: default are for 32.768KHz clock input

Note: All registers address are hex
QN8035 Software Programming Guide

QN8035 System Initialization

Software Initialization

Start Initialization
- Write 0x47 to Reg54h
- Write 0x40 to Reg19h
- Write 0xD6 to Reg2Dh
- Write 0x10 to Reg43h
- Write 0x51 to Reg00h
- Write 0x21 to Reg00h
- Delay 50ms

Prepare to go to Receive

Before entering Receive
- Set Reg1Bh[3] bit low
- Set Reg2Ch[5:0] = 0x12
- Set Reg1Dh[6] bit low
- Set Reg41h[3:0] = 0x0A
- Set Reg45h = 0x50
- Set Reg41h[7:5] = 0x06
- Set Reg41h[7] bit high
- Set Reg34h[6:0] = 0x37
- Set Reg35h[6:0] = 0x21
- Set Reg36h[6:0] = 0x13

End

For whole system performance adjusting

For receiver performance adjusting

Start
- Hardware Connection
- Power Up
- Software Reset
  - Write 0x81 to Reg00h

Software Reset
- Write corresponding data to Reg15h and Reg16h

Clock Frequency Selection
(32.768KHz or other frequencies clock)
- Write corresponding data to Reg15h and Reg16h

PLL Configuration
- Write corresponding data to Reg16h to Reg17h

Software Initialization
- Set Reg1Bh[3] bit low
- Set Reg2Ch[5:0] = 0x12
- Set Reg1Dh[6] bit low
- Set Reg41h[3:0] = 0x0A
- Set Reg45h = 0x50
- Set Reg41h[7:5] = 0x06
- Set Reg41h[7] bit high
- Set Reg34h[6:0] = 0x37
- Set Reg35h[6:0] = 0x21
- Set Reg36h[6:0] = 0x13

End

For receiver performance adjusting

Stop at Standby
- Write 0x51 to Reg00h
- Write 0x21 to Reg00h

End

Note: All registers address are hex
Receive, Idle and Standby Modes

- Three Modes Switching

- Manual Channel Tuning

<table>
<thead>
<tr>
<th>Mode</th>
<th>Bit</th>
<th>STNBY (Reg00h[5])</th>
<th>RXREQ (Reg00h[4])</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receive</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Idle</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Standby</td>
<td>1</td>
<td></td>
<td>x</td>
</tr>
</tbody>
</table>

Note: All Registers address are hex
Note: Reg00h=0x1 l, the chip will enable FM receive function only.
IMR Function

To improve FM receiver performance, QN8035 provides IMR function. When QN8035 will be tuned to some special channels to receive, there needs to be enable IMR. At these channel points (69.1MHz, 72.9MHz and 84.3MHz), Reg01h[6] should be set high. For other channel points, Reg01h[6] is still low.

<table>
<thead>
<tr>
<th>Frequency</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>69.100000 MHz</td>
<td></td>
</tr>
<tr>
<td>72.900000 MHz</td>
<td></td>
</tr>
<tr>
<td>84.300000 MHz</td>
<td></td>
</tr>
</tbody>
</table>

Audio Mute

<table>
<thead>
<tr>
<th>Mute Enable</th>
<th>Reg14h[7]=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mute Disable</td>
<td>Reg14h[7]=0</td>
</tr>
</tbody>
</table>

!! In QN8035 driver API, it is replaced by Reg4C
Cap-Bank Tuning

To improve the efficiency of antenna for FMR, QN8035 integrates cap-bank block. A 330nH inductor and one 100pF AC coupling capacitor need to be in series on RFI. A tunable internal capacitor with the external 330nH inductor can be adjusted together by software to maximize efficiency at the Resonant Frequency.

Reading RSSI

If Reg1Eh[7]=1, RSSI=Reg03h+9; otherwise RSSI= Reg03h.

RFInput = RSSI-43

Note: All registers address are hex
Solving Pop Noise

Audio Mute (Reg4Ch=0x1b)
1. Power Down Control select
2. Power Down DACR
3. Power Down DACL

Tune to Channel

Audio Un-mute (Reg4Ch=0x10)
1. Enable Control select
2. Enable DACR
3. Enable DACL

End

Note: All registers address are hex

Improving Sensitivity

Refer to QN8035 programming guide

Sensitivity Test

Before

After
Auto Seek (CCA)

1. Enable CCA Hardware Interrupt
   Set Reg[79][70] bit high (optional)

2. Set Start Frequency
   Write desired value to Reg[78][72:71]

3. Set Stop Frequency
   Write desired value to Reg[75][74:70]

4. Set Step: 50kHz, 100kHz or 200kHz
   Write desired value to Reg[70][70]

5. Set CCA threshold
   Write suitable value to Reg[64][60]

6. Set CCA_CH_DIS [Reg[64][0]:0] bit low

7. Set CH bits [Reg[60][11]:11] bit high

8. 20 ms delay

9. Read Reg[60][11] bit

10. Reg[60][11] = 0
    No

11. Read Reg[60][3] bit

12. Reg[60][3] = 0
    No

13. CCA Result is valid and read it
    Read value from Reg[60][15:60][72][70]

14. CCA Result is not valid

End

Note: All registers addresses are hex

Related Registers: Reg00h, Reg01, Reg04h, Reg08h, Reg09h, Reg0Ah and Reg17h
RDS Application

Related Registers: Reg00h, Reg0B to Reg13h and Reg17h

Note: All Registers address are hex
Note: Only 2 blocks for supporting hardware interrupt only
SotfRst 3 sequence, 20ms delay is just one example, new group data will be updated by every 8mcs in theory.
QN8035 EVB

Note: when Xclk is used, R11 should be used by 0 ohm, and R20 is NC.
QN8035 Design Points
QN8035 Design FAQ

Q: How many current after powering up in QN8035?
A: After powering up, QN8035 will stand at standby mode, and then current is about 50uA at room temperature.

Q: How many voltage are VIH, VIL, VOH, VOL?
A: Due to deleting VIO pin in QN8035, VIH and VIL are 1.1V and 0.4V respectively. VOH, VOL are determined by the voltage of external IO. VOH is 0.9*VIO, and VOL is 0.1*VIO.

Q: If i don't add LC series matching network, and just have 100pF capacitor in RFI net same as QN8025, will the performance of QN8035 drop?
A: No, the performance of QN8035 will also same as QN8025. If adding LC series matching network, sensitivity of QN8035 will be improved, and about -114dBm for average.

Q: Does QN8035 directly drive 32ohm headphone?
A: Yes, QN8035 has integrated 320hm load audio driver. THD will arrive at 0.05% even if Vout is 0.9Vpp.
QN8035 Issues

<table>
<thead>
<tr>
<th>Num</th>
<th>Issue Description</th>
<th>End status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Reading or writing I²C will induce SNR dropping from 63 to 52dB</td>
<td>Open</td>
</tr>
<tr>
<td></td>
<td>(Serious)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>The interference rejection at +200KHz is better than -200KHz</td>
<td>Open</td>
</tr>
<tr>
<td>3</td>
<td>Pop noise happen at initialization</td>
<td>Open</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
QN8035 Related Document and Support

- QN8035 Datasheet
- QN8035 Programming Guide
- QN8035 Hardware Application Note
- QN8035 Performance Test Report
QN8035 Related Document and Support

END