Analog Peripherals
24-Bit ADC
- 0.0015% nonlinearity
- Programmable throughput up to 1 ksp
- 8 external inputs; programmable as single-ended or differential
- Programmable amplifier gain: 128, 64, 32, 16, 8, 4, 2, 1
- Data-dependent windowed interrupt generator
- Built-in temperature sensor (±3 °C)

Two 8-Bit Current DACs

Comparator
- 16 Programmable hysteresis values and response time
- Configurable to generate interrupts or reset
- Low current (0.4 µA)

Internal Voltage Reference
VDD Monitor/Brown-out Detector

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz clock
- Expanded interrupt handler

Memory
- 768 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

Digital Peripherals
- 17 port I/O; all 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- 16-bit programmable counter array with three capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Realtime clock mode using PCA or timer and external clock source

Clock Sources
- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- 2x clock multiplier to achieve 50 MHz internal clock
- Can switch between clock sources on-the-fly

Supply Voltage: 2.7 to 3.6 V
- Typical operating current: 17 mA at 50 MHz
  16 µA at 32 kHz
- Typical stop mode current: <0.1 µA

32-Pin LQFP
Temperature Range: –40 to +85 °C
Selected Electrical Specifications

(T_A = –40 to +85 °C, V_DD = AV+ = 3.0 V, V_REF = 2.5 V External, PGA Gain = 1x, MDCLK = 2.4567 MHz, Decimation Ratio = 1920 unless otherwise specified)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>GLOBAL CHARACTERISTICS</td>
<td>Supply Voltage</td>
<td>2.7</td>
<td>3.6</td>
<td>V</td>
<td></td>
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<tr>
<td>Supply Current (CPU active)</td>
<td>Clock = 50 MHz</td>
<td>17</td>
<td>17</td>
<td>mA</td>
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<tr>
<td></td>
<td>Clock = 1 MHz</td>
<td>0.5</td>
<td>0.5</td>
<td>mA</td>
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<tr>
<td></td>
<td>Clock = 32 kHz; V_DD Monitor Enabled</td>
<td>16</td>
<td>16</td>
<td>μA</td>
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<tr>
<td>Supply Current (shutdown)</td>
<td>Oscillator not running; V_DD Monitor Disabled</td>
<td>0.1</td>
<td>0.1</td>
<td>μA</td>
<td></td>
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<tr>
<td>Clock Frequency Range</td>
<td>DC</td>
<td>50</td>
<td>MHz</td>
<td></td>
<td></td>
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<tr>
<td>24-BIT A/D CONVERTER</td>
<td>Resolution</td>
<td>(no missing codes)</td>
<td>24</td>
<td>bits</td>
<td></td>
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<tr>
<td>Integral Nonlinearity</td>
<td>Single-ended Mode</td>
<td>±15</td>
<td>ppm FS</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Differential Mode</td>
<td>±15</td>
<td>ppm FS</td>
<td></td>
<td></td>
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<tr>
<td>Offset Error</td>
<td></td>
<td>±5</td>
<td>ppm</td>
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<tr>
<td>Gain Error</td>
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<td>±0.002</td>
<td>%</td>
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<td>Common Mode Rejection Ratio (CMRR)</td>
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<tr>
<td>Power Supply Rejection, DC</td>
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<td>80</td>
<td>dB</td>
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<tr>
<td>Power Supply Current</td>
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<tr>
<td>8-BIT CURRENT-MODE D/A CONVERTERS</td>
<td>Resolution</td>
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<tr>
<td>Integral Nonlinearity</td>
<td>Guaranteed Monotonic</td>
<td>±0.5</td>
<td>LSB</td>
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<tr>
<td>Differential Nonlinearity</td>
<td>Guaranteed Monotonic</td>
<td>±0.5</td>
<td>±1</td>
<td>LSB</td>
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Package Information

C8051F350DK Development Kit