Dynamic Biasing: a Low Power Linearisation Technique

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Abstract

A highly linear opamp processed in a .25µm 2 V CMOS technology suitable for an Intermediate Frequency (IF) Continuous Time Sigma-Delta Analog-to-Digital Converter (Σ∆ ADC) is presented. Due to an improved technique, called Dynamic Biasing, distortion components in an IF band, typically situated at frequencies from 1 to 10 MHz for a low-IF receiver architecture, are lowered without any signal degradation. The circuit achieves an IIP3 and an IIP5 of more than 20 dBm. The power consumption is limited to 3.4 mW.

1. Introduction

The elaborated analysis and design of a second order analog-to-digital converter with a continuous time loop filter implementation as presented in [1] and [2], has pointed out the most important issues of a continuous time design especially if low power is a main issue. It reveals that the AD loop filter, and especially the opamp of the first filter slice, mainly determines the power consumption of the entire ADC. In fact this filter slice must achieve the Dynamic Range (DR) of the entire converter in order not to degrade the overall resolution. In a continuous time implementation with RC, gmC and gm-RC topologies high, a DR is only attainable with a high resistive degeneration of the transistor which consequently leads to a significant power drain. Because that first filter opamp signifies a “hot spot” in terms of power consumption, an opamp architecture is contrived which can achieve the desired high DR without the need of the traditional power hungry resistive degeneration.

2. Increase the Dynamic Range

While the noise floor sets the lower boundary of the Dynamic Range (DR), the upper limit or maximal input amplitude depends on the maximally tolerable distortion [3] [4], which is given by the required Signal-to-Noise-and-Distortion Ratio (SNDR) specification. A sufficient DR will only be achieved if the distortion components are well controlled.

2.1. Resistive Degeneration

Resistive source or gate degeneration, as shown in figure 1, is a valuable and stable method to improve the linearity of the system. Formula 1 gives the linearity performance in term of HD3 in function of the degenerative resistor value $R_{deg}$ and the transistor current $I_{ds}$ ($v_{p}$ is the input amplitude), if condition 2 is fulfilled.

$$HD3 = \frac{1}{32} \cdot \frac{(V_{gs} - V_{t}) \cdot v_{p}^{2}}{(I_{dc} \cdot R_{deg})^{3}}$$ (1)

$$gm_{rd} \cdot R_{deg} \gg 1 \quad gm_{rd} \gg \frac{gm_{rd}}{1 + gm_{rd} \cdot R_{deg}}$$ (2)

$$gm_{rd} \gg gm_{eq} \approx \frac{1}{R_{deg}}$$ (3)

The reduction of distortion come at the expense of higher current drain which compensates for the loss of the effective transconductance $gm_{eq}$ (formula 3). At first order the power consumption is proportional to the achieved DR.

2.2. An improved proposal to increase the DR

The principle depicted in figure 2 reduces the higher order distortion components without degradation of the transconductance. The input transistor pair is loaded with resistors to obtain a nearly unity gain. As a result the output consists of the inverted input and distortion components of the input pair. The sum of input and output signals consists ideally of only the unwanted higher order harmonics. A negative feedback structure amplifies this sum to modulate dynamically the biasing sources. The distortion components are therefore reduced with the loop gain of the feedback. Resistor $R_{s}$ is
placed between the sources of the input pair to provide a differential voltage swing at the transistor sources necessary for the feedback. Contrary to the $R_{\text{deg}}$ resistor of figure 1, resistor $R_s$ does not induce any signal degradation (formula 4) because it’s conductance value can be chosen even higher than the transistor $gm_{db}$ (formula 5).

\[
gm_{db} \approx gm_{eq} \ll gm_{rd} 
\]

\[
gm_{db}, R_s \lesssim 1
\]

Contrary to previously published cancellation techniques [5], this technique has the big advantage not to degrade only the third order harmonics but all higher order spurious signals which fall into the signal band.

3. Dynamic Biasing in Filter Applications

3.1. Filter and “Dummy” Opamp

Because of the imposed unity gain of the architecture presented in figure 2, the principle would only be useful in highly linear buffer application where no gain is needed. Therefore figure 3 presents a structure composed of a $gmC$ filter opamp and a “dummy” $gmR$ opamp with the same input stage as in figure 2. If the biasing sources of the filter opamp are also dynamically biased, the distortion components are similarly canceled as in the “dummy” opamp. The filter opamp is shown in figure 4 with a folded cascode structure necessary to provide enough gain. The common mode feedback (CMFB) is integrated in the opamp core. Linear transistors in series with the bias current sources ensure the CMFB at low frequencies. At high frequencies, the CMFB is guaranteed by capacitive bypasses.

3.2. Validity

The theory assumes that the input transistor pair is the main source of distortion of the filter (opamp) [6]. If the opamp is charged with a capacitive load, this assumption is valid only for frequencies beyond the BW as the capacitance can be considered as an highly linear load. This condition is fulfilled in case the the opamp is designed as a part of the CT ADC for low-IF receiver applications [1], knowing that only (low level) quantization noise contains spectral power from DC up to the BW.

3.3. The Feedback

Because the linearity improvement is proportional to the feedback loop gain, a cascode topology is chosen to provide sufficient amplification as shown in figure 5. Transistors $M_{tk}$ provide the summing of in- and output voltages of the dummy opamp. A slight resistive degeneration permits proper summing even for high swing input voltages. The summed currents are mirrored towards the cascode stage. Due to the high output capacitive load which consists of the gate capacitance of the input stage biasing transistors, and a moderate loop gain requirement, a one stage cascode is preferred to a Miller opamp. To obtain the necessary 180° phase shift between input and output an inverting current mirror in inserted in the folded cascode. Even though a second pole will appear at the mirror stage, it can be easily shifted towards higher frequencies to prevent stability decrease.

3.4. Matching

To provide a good similar cancellation of the higher order distortion components in both the opamp and the dummy opamp, matching of the two structure is of major importance. Therefore simulations provide the tolerable mismatch of the different transistors in the input and feedback stage, summarized in table 1.

Relying on the technology specifications the minimal tran-
sistor sizes are determined. The need for non-minimal transistor lengths will push up the load of the feedback stage and determines its minimal power.

3.5. Possible Drawbacks

The GBW of the feedback must be at least $A \times f_o$ with $A$ the loop gain, $f_o$ the highest operation frequency. For “low” IF frequencies in the range of 1..10 MHz and the low requirements for the filter GBW in continuous time implementations, limited frequency behavior isn’t an issue. Further, the deviation of the values of the input transconductance and the admittance of the resistive load has no degradation on the distortion reduction. Simulations show that even in the case of major divergence the only effect is a variation of the effective transconductance. However considering the high level design of the ADC, the topology parameters which directly determines the GBW of the different filter opamps are chosen such that an acceptable deviation of these parameters doesn’t lead to a significant SNR degradation. This structure loses its benefits if other major distortion sources exist other than the input transistor pair. As explained previously it’s not the case in this RC or gmC filter implementation.

4. Measurements

In figure 6, a photograph of the entire chip is shown. The chip has been processed in a 0.25 $\mu m$ CMOS technology. Much care has been taken during the layout in order to obtain a low mismatch influence.

The linearity performance of the filter opamp in open loop is measured for frequencies from 1 up to more than 10 MHz, with and without dynamic biasing. The in-band inter-

<table>
<thead>
<tr>
<th>Mbias</th>
<th>2 mV</th>
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<tbody>
<tr>
<td>Ml(Rl)</td>
<td>15 mV</td>
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</table>
modulation distortion is measured by applying an input signal containing two 0 dBm sine waves at 9.6 MHz and 10 MHz. Figure 7 shows the output current spectrum containing both wanted output and inter-modulation distortion components. The distortion products of the opamp without dynamic biasing are drawn in stippled lines. Figure 7 makes clear that with the help of the dynamic biasing feedback, the third order inter-modulation distortion components lower with almost 30 dB and the fifth order with almost 10 dB. All other higher order spurious frequencies lay below these third and fifth order harmonics. Consequently, the input referred third order inter-modulation intercept point (IIP3) as well as the fifth order inter-modulation intercept point (IIP5) are more 20 dBm and its power consumption is less than 3.4 mW.

Due to the duplicated structure the DR improvement will be slightly lower than the linearity improvement due to a higher noise level. Measurements showed an increase of output noise power of almost 3 dB when the dynamic biasing feedback was switched on.

The performance of the linear opamp is summarized in table 2.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>1 - 10 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>IIP3</td>
<td>&gt; 20 dBm</td>
</tr>
<tr>
<td>IIP5</td>
<td>&gt; 20 dBm</td>
</tr>
<tr>
<td>Power</td>
<td>3.4 mW</td>
</tr>
<tr>
<td>Supply</td>
<td>2 V</td>
</tr>
<tr>
<td>Technology</td>
<td>0.25µm CMOS</td>
</tr>
</tbody>
</table>

## 5. Conclusions

An highly linear opamp is presented with a principle to lower the distortion components. Contrary to resistive degeneration which needs a high power consumption to compensate its inevitable signal degeneration, this structure does not affect the transistor transconductance. Starting from a low power highly distorted opamp, a replica of its input stage together with a low power feedback structure provides the necessary distortion cancellation by dynamically biasing the current. Although the higher complexity of this proposal, the entire structure consumes less power because it is made up of low power components. This opamp with dynamic biasing is especially designed as a filter part of an low-IF continuous time sigma-delta analog-to-digital converter which typically copes with signals in the range of 1..10 MHz. Measurements showed that the opamp achieves an IIP3 and IIP5 of more than 20 dBm for a 3.4 mW power consumption.

### 5.1. Acknowledgements

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