High Speed Data and Clock Distribution

Maxim Integrated Products
System Sensing and Interface Products Business Unit

Andreas Mühlschein
Agenda Overview

- High Speed Data and Clock Distribution
  - Design Example
  - Design Challenges

- Clock/Data Path Solutions from Maxim
  - Performance of Maxim CDD Products
  - Interconnect Product Types
  - Product Selection Guide
  - Product Examples

- SERDES Design Examples
  - SERDES Design Considerations
  - SERDES Product Overview
  - Design Examples
Market Examples

- Portable Media Players
- Ethernet Switch / Routers
- Base-Stations
- Network Storage
- DSL, IP-DSLAM Line Cards
- Navigation and Infotainment
- SONET/SDH & Synchronous Ethernet
- Clock/Data Distribution End Equipment
Design Example

Frame Processing
(Eg. CPRI)

Redundant Data Stream to Backhaul network

PLL Jitter Cleaner
164.32MHz

FPGA

D-Buf
C-Buf

Data
Clock

FPGA

DUC DDC CFR DPD

Data
Clock

DAC 1.2Gbps

ADC 1.7Gbps

FPGA

Data
Clock

DAC 1.2Gbps

ADC 1.7Gbps

To RF Card

PLL Synth
52MHz

Clk Splitter

52MHz

** RS-232 interfaces and UART not shown

Maxim Confidential
## Clock/Data Path Design Challenges

<table>
<thead>
<tr>
<th>Design Challenge</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random / Deterministic Jitter</td>
<td>Reduce Jitter Accumulation</td>
</tr>
<tr>
<td>Channel to Channel Skew</td>
<td>Low Skew</td>
</tr>
<tr>
<td>Different I/O Interfaces</td>
<td>Level Translator / Flexible I/O</td>
</tr>
<tr>
<td>Signal Level Attenuation</td>
<td>Buffer</td>
</tr>
<tr>
<td>Signal Rise and Fall Time</td>
<td>High Speed Buffer</td>
</tr>
<tr>
<td>Frequency Dependent Losses</td>
<td>Equalizer / Pre-Emphasis Driver</td>
</tr>
<tr>
<td>Space Limitation for Parallel Interconnects</td>
<td>SERDES</td>
</tr>
</tbody>
</table>
Design Challenges: Different I/O Signal Levels

Voltage [V]

-2
-1
0
1
2
3
4
LVDS
LVPECL
PECL
CML
1.5V HSTL
2.5V LVTTTL/ LVCMOS
3.3V LVTTTL/ LVCMOS
ECL

Maxim Confidential
Design Challenges: Frequency Dependent Losses

[Diagram showing transmission line with different lengths and corresponding signal distortions before and after an equalizer.]
Design Challenges: Frequency Dependent Losses

Pre-Emphasis Generation

1-bit wide FIR (Digital)
- Easy to implement
- Crude approximation

Multi-bit FIR (Digital)
- Better approximation
- More complex

Analog Filter (Maxim)
- Accurate transfer function
- Not an approximation
- Simple
Clock/Data Path Solutions from Maxim
Solutions from Maxim - Performance

- **PECL, ECL, LVPECL - Products**
  - Up to 3.5GHz
  - Down to 0.2ps RMS Jitter
  - Down to <10ps Output-Output Skew
  - 64 Introductions, 38 second sources

- **LVDS – Products**
  - Up to 1.5GHz
  - Down to 0.8ps RMS Jitter
  - Down to <10ps Output-Output Skew
  - Low Power
  - 44 Introductions, 26 Second sources

- **CML - Equalizer/Pre-Emphasis Driver - Products**
  - Up to 12.5Gbps Data Rate
  - Down to 0.8ps RMS Jitter
  - Low Power
  - 16 Introductions
Solutions from Maxim - Interconnect Product Types

Product Types:

Clock/Data Buffer

Clock/Data Fan Out Buffer

Data Driver and Receiver

Level Translator

Cross Point Switch

Multiplexer/Demultiplexer

Serializer/Deserializer

Equalizer/Pre-Emphasis Driver

LVPECL and LVDS are the most popular protocols. LVPECL and LVDS are very well supported.
Choose your ratio of transmit channels to receive channels

<table>
<thead>
<tr>
<th>Tx Channels</th>
<th>2</th>
<th>4</th>
<th>5</th>
<th>5</th>
<th>9</th>
<th>10</th>
<th>14</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rx Channels</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

Fan Out from 1 → 1 to 2 → 15.

Also available:
Multiplexers (2 → 1 to 8 → 1) (used for redundancy)
Demultiplexers 1 → 2 with loop back.
Product Examples: Maxim PECL/ECL Product Family

More than 60 products introduced!

New Devices in Design!

PECL/ECL

Clock Drivers/Repeaters
- 1:2
- 1:5/2X5:1
- 1:10
- 1:15

Level Translators
- PECL/ECL
- ECL to PECL
- PECL to LVDS
- LVDS to PECL

Mux
- 2:1
- 4:1/2x4:1
- 5:1
- 8:1
LVECL/LVPECL

1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

MAX9322

Features

♦ 1.2ps (RMS) Maximum Random Jitter
♦ 300mV Differential Output at 1.0GHz
♦ 900ps Propagation Delay
♦ Selectable Divide-by-1 or Divide-by-2 Frequency Outputs
♦ Multiplexed 2:1 Input Function
♦ LVECL Operation from VEE = -2.375V to -3.8V
♦ LVPECL Operation from VCC = +2.375V to +3.8V
♦ ESD Protection: > 2kV Human Body Model

Applications

Precision Clock Distribution
Low-Jitter Data Repeaters
Central-Office Backplane Clock Distribution
DSLAM Backplane
Base Stations
ATE
MAX9376
2.0 GHz Dual Channel Anything to LVPECL & LVDS Translators

**Pin Configuration**

**Features**
- Guaranteed 2GHz Switching Frequency
- Accepts LVDS/LVPECL/Anything Inputs
- 421ps (typ) Propagation Delays
- 30ps (max) Pulse Skew
- $2\mu$s (max) Random Jitter
- Minimum 100mV Differential Input to Guarantee AC Specifications
- Temperature-Compensated LVPECL Output
- +3.0V to +3.6V Power-Supply Operating Range
- >2kV ESD Protection (Human Body Model)

**Applications**
- Backplane Logic Standard Translation
- LVDS-to-LVPECL, LVPECL-to-LVDS
- Up/Downconverters
- LANs
- WANs
- DSLAMs
- DLCs
Product Examples: Maxim LVDS Product Family

More than 60 products introduced!

New Devices in Design!

LVDS

- Line Drivers
  - 1 Tx
  - 2 Tx
  - 4 Tx

- Line Receivers
  - 1 Rx
  - 2 Rx
  - 4 Rx

- Line Transceivers (Tx/Rx)

- Crosspoint Switches

- Repeaters and Fan-out Buffers

- Serializers

- Deserializers

1 Tx

2 Tx

4 Tx

1 Rx

2 Rx

4 Rx
MAX9390/91

Anything-to-LVDS Dual 2 x 2 Cross point Switches with 1.5GHz switching and 2ps (RMS) maximum random jitter.

The dual 2 x 2 cross point switch perform high-speed, low-power, and low-noise signal distribution. The MAX9390/MAX9391 multiplex one of two differential input pairs to either or both low-voltage differential signaling (LVDS) outputs for each channel. Independent enable inputs turn on or turn off each differential output pair.
Cross Bar Switches (MAX9132/34/35)

Features:

- Support up to 840Mbps data rate per port
- Cross Bar LVDS switch
  - MAX9132 : 3in/2out
  - MAX9134 : 3in/4out
  - MAX9135 : 4in/3out
- Broadcast data signal from an uplink port to all downlink ports
- Not activated ports are in Hi-Z state
- Output ports have pre-emphasis
- 3 approaches for switch routing:
  1. LIN Interface
  2. I2C interface
  3. programmable pins
- High ESD protection: > 25 kV
- Supply voltage: 3.3V
- Packages: TQFP 32 and TQFN 32
- Operation temperature range: -40°C to +105°C
## Product Examples: Equalizer/Pre-Emphasis Driver Portfolio

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Available Speeds</th>
</tr>
</thead>
<tbody>
<tr>
<td>Four-Channel Interface</td>
<td>10Gbase-CX4 6.25Gbps XAUÍ 3.125Gbps XAUÍ</td>
</tr>
<tr>
<td>InfiniBand</td>
<td>5Gbps DDR 2.5Gbps</td>
</tr>
<tr>
<td>Fibre Channel</td>
<td>8.5Gbps 4.25Gbps 2.125Gbps 1.0625Gbps</td>
</tr>
<tr>
<td>Ethernet</td>
<td>10.3Gbps 5Gbps 2.5Gbps 1.25Gbps</td>
</tr>
<tr>
<td>SONET/SDH</td>
<td>9.952Gbps 4.976Gbps 2.488Gbps</td>
</tr>
</tbody>
</table>

- 16 Analog Signal Integrity products available
- 1Gbps -12.5 Gbps
- For Transmit & Receive
- Fixed, Settable, Adaptive, and Passive
- Single and Quad Channel
- For Cable and FR4
MAX3984 Pre-Emphasis Driver for 8G FC and 10 GbE Back Planes

Features

♦ Drives Up to 10m of 24 AWG Cable
♦ Drives Up to 30in of FR-4
♦ Selectable 1000mVp-p or 1200mVp-p Differential Output Swing
♦ Selectable Output Preemphasis
♦ Selectable Input Equalization
♦ LOS Detection with Built-In Squelch
♦ Transmit Disable
♦ Hot Pluggable

Graph: Deterministic Jitter vs. FR-4 Length (10.3Gbps)
MAX3787 12.5-Gbps Passive Equalizer

**Features**

- No Power Supply Required
- Small 1.5mm x 1.5mm Chip-Scale Package
- Passive Equalization Reduces ISI
- Operates from 1Gbps to 12.5Gbps
- Extends Board Link
- Extends Cable Link
- Coding Independent, 8b/10b or Scrambled

8.5Gbps

10.3Gbps

18in FR4 MicroStrip
SERDES Design Examples
SERDES Design Considerations

- Reduce Cable Count in Space Limited Applications
- Minimize Radiation in Sensitive Applications
- Protect Devices for Ground Shifts
- Compensate Frequency Dependent Losses
- Minimize Critical External Components
- Increase Cable Length
- Ensure High ESD Protection
## SERDES Product Overview

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
<th>Switching Frequency (MHz)</th>
<th>$V_{CC}$ (V)</th>
<th>$I_{CC}$ (mA, max)</th>
<th>Random Jitter ($pS_{RMS}$, max)</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX9235/05/07</td>
<td>LVTTL/CMOS</td>
<td>40/66</td>
<td>3.3</td>
<td>45</td>
<td>13</td>
<td>28-SSOP/16-TQFN</td>
</tr>
<tr>
<td>MAX9206/08</td>
<td>LVDS</td>
<td>40/60</td>
<td>3.3</td>
<td>75/100</td>
<td>—</td>
<td>28-SSOP</td>
</tr>
<tr>
<td>MAX9209/13</td>
<td>LVTTL/CMOS</td>
<td>16 to 66</td>
<td>3.3</td>
<td>83/100</td>
<td>—</td>
<td>48-TSSOP/TQFN*</td>
</tr>
<tr>
<td>MAX9210/14/20/22</td>
<td>LVDS</td>
<td>16 to 66</td>
<td>3.3</td>
<td>152/177</td>
<td>—</td>
<td>48-TSSOP/TQFN*</td>
</tr>
<tr>
<td>MAX9217/47</td>
<td>LVTTL/CMOS</td>
<td>2.5 to 42</td>
<td>3.3</td>
<td>—</td>
<td>—</td>
<td>48-TSSOP/TQFN*</td>
</tr>
<tr>
<td>MAX9218/48/50</td>
<td>LVDS</td>
<td>2.5 to 42</td>
<td>3.3</td>
<td>—</td>
<td>—</td>
<td>48-TSSOP/TQFN*</td>
</tr>
<tr>
<td>MAX9223/24</td>
<td>LVDS</td>
<td>5 to 10</td>
<td>2.5/3.3</td>
<td>4/8</td>
<td>—</td>
<td>28-TQFN</td>
</tr>
<tr>
<td>MAX9225/26</td>
<td>LVDS</td>
<td>10 to 20</td>
<td>2.5/3.3</td>
<td>4/8</td>
<td>—</td>
<td>16-TQFN</td>
</tr>
<tr>
<td>MAX9234/36/38</td>
<td>LVDS</td>
<td>16 to 66</td>
<td>3.3</td>
<td>152/177</td>
<td>—</td>
<td>48-TSSOP</td>
</tr>
<tr>
<td>MAX9242/44/46/54</td>
<td>LVDS</td>
<td>6 to 40</td>
<td>3.3</td>
<td>123/145</td>
<td>—</td>
<td>48-TSSOP</td>
</tr>
</tbody>
</table>
SERDES Design Example

MAX9247/MAX9248 27:1 LVDS Serializer/Deserializer for up to 1280x480 Resolution Displays

Up to 30KV ESD Protection
2.5MHz to 42MHz Reference Clock Range
Pre-Emphasis for Cable Length Extension
SERDES Design Example
MAX9257/MAX9258  18:1 LVDS Serializer/Deserializer for Camera, Display and Audio Links

Diagram showing the connection of various components such as Processor, LCD, Clock, DES, SER, Camera, Tx, Rx, µC, and Camera Control Bus.
MAX9257/MAX9258 SERDES

Features:
- Programmable Parallel Interface 10/12/14/16/18
- Spread Spectrum for EMI Reduction
- 5 Level Programmable Pre-Emphasis for Cable Length Extension
- DC-Balance to allow AC Coupling to Protect for Ground Shifts
- Integrated 10Mbps Control Channel for Remote Device Control
- 5MHz to 70MHz Reference Clock Frequency Range
- -40°C to +105°C Operating Temperature Range
Clock Synthesizer

Maxim Integrated Products
Agenda Overview

- Clock Synthesizer
  - Clock Architecture Trends
  - Clock Design Considerations
  - Solutions from Maxim
  - Clock Product Selection Guide
  - Clock Product Overview
  - Clock Product Examples
Market Examples

- Enterprise
- Wireless
- SONET
- Server
- Storage
Clock Trends: Replacing Oscillator Modules with PLL Clock Synthesizer ICs

OLD

High-frequency (>100 MHz) Crystal
- Thin <20um
- Expensive
- Mechanical Failures

NEW

Low-frequency (~25 MHz) Crystal
- Thick ~60um
- Low-cost
- High-reliability

Paper 100um
Clock Trends: Solutions for PLL/VCO Clock Generator ICs

Existing Solution

XO Module using Maxim PLL/VCO IC

Maxim PLL/VCO IC replaces XO module

Maxim PLL/VCO + Fan Out IC

= oscillator module
= oscillator IC
= Maxim fanout IC
= Maxim PLL/VCO IC
Clock Design Considerations

**Design Challenge:**
- Multiple Clock Frequencies
- Clock Fan Out
- Jitter of Reference Clock
- Jitter Generation of Clock Generator
- Jitter Generation of Clock Fan Out
- Power Supply Noise Rejection
- Design to Cost

**Solution:**
- Multiple Clock Generator
- Integrated Fan Out Buffer
- Jitter Filter (Low PLL BW)
- Low Jitter PLL Design
- Reduce Jitter Accumulation
- High PSNR
- High Integrated Solution
## Solutions from Maxim : Jitter and PSNR

<table>
<thead>
<tr>
<th>Part</th>
<th>Integrated Phase Jitter (psrms)</th>
<th>PSNR (dBc)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(12kHz-20MHz)</td>
<td>+100kHz</td>
</tr>
<tr>
<td>MAX3610 PECL (f_c=106.25MHz)</td>
<td>0.72</td>
<td>-54.0</td>
</tr>
<tr>
<td>MAX3622 PECL (f_c=156.25MHz)</td>
<td>0.43</td>
<td>-50.0</td>
</tr>
<tr>
<td>MAX3673 PECL (f_c=125MHz)</td>
<td>0.28</td>
<td>-68</td>
</tr>
<tr>
<td>Competitor A PECL (f_c=106.25MHz)</td>
<td>0.76</td>
<td>-14.6</td>
</tr>
<tr>
<td>Competitor B PECL (f_c=106.25MHz)</td>
<td>0.79</td>
<td>-33.3</td>
</tr>
<tr>
<td>SAW PECL (f_c=106.25MHz)</td>
<td>0.28</td>
<td>-68.0</td>
</tr>
<tr>
<td>3rd overtone PECL (f_c=212.5MHz)</td>
<td>0.22</td>
<td>-71.0</td>
</tr>
</tbody>
</table>

- Jitter matches standalone oscillators
- PSNR 30-60 dB better than competition, matches standalone oscillators.
Solutions from Maxim: Clock Synthesizer ICs with Integrated Fan Out

5x7 Oscillator Module Package
- 6 pins limits # outputs to 1
- Requires separate Fan Out Buffer to drive multiple-output clock trees

Flexible IC packaging
- Various sizes, lots of pins
- Can integrate Fan Out to provide multiple outputs
- Can synthesize multiple clock frequencies from a common crystal

Saves money
Saves power
Saves board space
Reduces accumulated jitter
## Clock Product Selection Guide

### Parametric Search: Clock Generators

<table>
<thead>
<tr>
<th>Applications</th>
<th>( f_N ) (MHz)</th>
<th>( f_O ) (MHz)</th>
<th>Output Levels</th>
<th>Output Jitter (p-p)</th>
<th>( V_{\text{supply}} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ethernet</td>
<td>( \leq 500 )</td>
<td>( \leq 1360 )</td>
<td>1</td>
<td>No</td>
<td>2.5</td>
</tr>
<tr>
<td>Fibre Channel</td>
<td></td>
<td></td>
<td>2</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>GSM</td>
<td></td>
<td></td>
<td>3</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>General Purpose</td>
<td></td>
<td></td>
<td>4</td>
<td>Yes</td>
<td>3.3</td>
</tr>
<tr>
<td>InfiniBand</td>
<td></td>
<td></td>
<td>5</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>PCIe</td>
<td></td>
<td></td>
<td>6</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>SONET/SDH</td>
<td></td>
<td></td>
<td>7</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>T1/E1</td>
<td></td>
<td></td>
<td>8</td>
<td>Yes</td>
<td>3.3</td>
</tr>
<tr>
<td>T3/E3</td>
<td></td>
<td></td>
<td>9</td>
<td>No</td>
<td>3.3</td>
</tr>
</tbody>
</table>

### More Clock Generation & Distribution

<table>
<thead>
<tr>
<th>Application</th>
<th>( f_N ) (MHz)</th>
<th>( f_O ) (MHz)</th>
<th>PLLc</th>
<th>Continuity</th>
<th>Output Jitter (p-p)</th>
<th>( V_{\text{supply}} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ethernet</td>
<td>( \leq 500 )</td>
<td>( \leq 1360 )</td>
<td>1</td>
<td>Fixed</td>
<td>No</td>
<td>2.5</td>
</tr>
<tr>
<td>Fibre Channel</td>
<td></td>
<td></td>
<td>2</td>
<td>Fixed</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>GSM</td>
<td></td>
<td></td>
<td>3</td>
<td>Fixed</td>
<td>Yes</td>
<td>3.3</td>
</tr>
<tr>
<td>General Purpose</td>
<td></td>
<td></td>
<td>4</td>
<td>Fixed</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>InfiniBand</td>
<td></td>
<td></td>
<td>5</td>
<td>Fixed</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>PCIe</td>
<td></td>
<td></td>
<td>6</td>
<td>Fixed</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>SONET/SDH</td>
<td></td>
<td></td>
<td>7</td>
<td>Fixed</td>
<td>Yes</td>
<td>3.3</td>
</tr>
<tr>
<td>T1/E1</td>
<td></td>
<td></td>
<td>8</td>
<td>Fixed</td>
<td>No</td>
<td>3.3</td>
</tr>
<tr>
<td>T3/E3</td>
<td></td>
<td></td>
<td>9</td>
<td>Fixed</td>
<td>Yes</td>
<td>3.3</td>
</tr>
</tbody>
</table>

### Find Part Number in Parametric Database

- Enter Part No.
- Part Search
- Part Details

### Maxim Confidential
# Clock Product Overview: Selection Table-1

## 12K~20MHz

<table>
<thead>
<tr>
<th>Jitter</th>
<th>Part#</th>
<th>Package</th>
<th>Application</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;50psec</td>
<td>MAX9489 ETJ</td>
<td>32TQFN</td>
<td>✓</td>
<td>✓</td>
<td>Xtal</td>
</tr>
<tr>
<td></td>
<td>MAX9492 ETP</td>
<td>20TQFN</td>
<td>✓</td>
<td>✓</td>
<td>Xtal</td>
</tr>
<tr>
<td>&lt;6psec</td>
<td>MAX3674 ECM+</td>
<td>48LQFP</td>
<td>✓</td>
<td>✓</td>
<td>Xtal</td>
</tr>
<tr>
<td></td>
<td>MAX3676 EUG</td>
<td>24TSSOP</td>
<td>✓</td>
<td>✓</td>
<td>Xtal</td>
</tr>
<tr>
<td>0.7psec</td>
<td>MAX3682 EHA+</td>
<td>8TSSOP</td>
<td>✓</td>
<td>✓</td>
<td>Xtal</td>
</tr>
<tr>
<td></td>
<td>MAX3683 EHA+</td>
<td>8TSSOP</td>
<td>✓</td>
<td>✓</td>
<td>Xtal</td>
</tr>
<tr>
<td></td>
<td>MAX3684 EHA+</td>
<td>8TSSOP</td>
<td>✓</td>
<td>✓</td>
<td>Xtal</td>
</tr>
<tr>
<td>Jitter Cleaner</td>
<td>MAX3670 EGJ</td>
<td>32QFN</td>
<td>✓</td>
<td>✓</td>
<td>ref clock</td>
</tr>
<tr>
<td>ext. Crystal</td>
<td>MAX9450 EHJ</td>
<td>32TQFP</td>
<td>✓</td>
<td>✓</td>
<td>ref clock</td>
</tr>
<tr>
<td></td>
<td>MAX9451 EHJ</td>
<td>32TQFP</td>
<td>✓</td>
<td>✓</td>
<td>ref clock</td>
</tr>
<tr>
<td></td>
<td>MAX9452 EHJ</td>
<td>32TQFP</td>
<td>✓</td>
<td>✓</td>
<td>ref clock</td>
</tr>
<tr>
<td>nsec delay Line</td>
<td>MAX3620 AETT</td>
<td>6TDFN</td>
<td>✓</td>
<td>✓</td>
<td>clock</td>
</tr>
</tbody>
</table>
# Clock Product Overview: Selection Table -2

## 12K~20MHz

<table>
<thead>
<tr>
<th>Jitter</th>
<th>Part#</th>
<th>Package</th>
<th>Application</th>
<th>Input</th>
<th>Output</th>
<th>Sample</th>
<th>Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.36psec</td>
<td>MAX3622 CUE+</td>
<td>16TSSOP</td>
<td>Ethernet</td>
<td>✓</td>
<td>✓</td>
<td>Xtal</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>MAX3624 UTJ+</td>
<td>32TQFN</td>
<td>Storage</td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>MAX3625 CUG+</td>
<td>24TSSOP</td>
<td>Wireless</td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>MAX3679 UTJ+</td>
<td>32TQFN</td>
<td>SONET</td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>MAX3697 UTJ+</td>
<td>32TQFN</td>
<td>Controller</td>
<td></td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>MAX3698 UTJ+</td>
<td>32TQFN</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>MAX3629 CUG+</td>
<td>32TQFN</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>MAX3677 UTJ+</td>
<td>32TQFN</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>MAX3626 UTJ+</td>
<td>32TQFN</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>MAX3689 UTJ+</td>
<td>32TQFN</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>MAX3612 ETJ+</td>
<td>32TQFN</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>9 Differential</td>
</tr>
<tr>
<td></td>
<td>MAX3638 UTJ+</td>
<td>32TQFN</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>6 Differential</td>
</tr>
<tr>
<td></td>
<td>MAX3686 UTJ+</td>
<td>32TQFN</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>6 Differential</td>
</tr>
<tr>
<td></td>
<td>MAX3696 UTJ+</td>
<td>32TQFN</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>Xtal/CMOS</td>
<td>6 Differential</td>
</tr>
<tr>
<td>0.25psec</td>
<td>MAX3671 UTE+</td>
<td>56TQFN</td>
<td>ref clock</td>
<td>✓</td>
<td>✓</td>
<td>ref clock</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>MAX3673 UTE+</td>
<td>56TQFN</td>
<td>ref clock</td>
<td>✓</td>
<td>✓</td>
<td>ref clock</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>MAX3678 UTE+</td>
<td>56TQFN</td>
<td>ref clock</td>
<td>✓</td>
<td>✓</td>
<td>ref clock</td>
<td>9</td>
</tr>
</tbody>
</table>
Clock Product Examples
Features:
• 2 banks of outputs:
  – Bank 1 = 1 LVPECL + 1 LVCMOS
  – Bank 2 = 2 LVPECL
• Ethernet, Fibre Channel, and SONET/SDH frequencies
• Very low Jitter:
  – 0.36 ps rms, 12 kHz – 20 MHz
  – 0.14 ps rms 1.875 MHz – 20 MHz
• Excellent PSNR: -57 dBc @ 100 kHz
• 5mm x 5 mm 32 TQFN

Applications:
• Enterprise (Ethernet) Switches
• Aggregation cards on SONET/SDH Systems
• Fibre Channel Switches
• BPON/GPON OLTs
# MAX3624 Frequency Table

## Table 1. Output Frequency Determination Chart

<table>
<thead>
<tr>
<th>XO OR CMOS INPUT FREQUENCY (MHz)</th>
<th>FEEDBACK DIVIDER, M</th>
<th>VCO FREQUENCY (MHz)</th>
<th>OUTPUT DIVIDER, NA AND NB</th>
<th>OUTPUT FREQUENCY (MHz)</th>
<th>APPLICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>25</td>
<td>625</td>
<td>2</td>
<td>312.5</td>
<td>Ethernet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>156.25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>125</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>78.125</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>62.5</td>
<td></td>
</tr>
<tr>
<td>25.78125</td>
<td>25</td>
<td>644.53125</td>
<td>4</td>
<td>161.132812</td>
<td>10Gbps Ethernet</td>
</tr>
<tr>
<td>26.04166</td>
<td>24</td>
<td>625</td>
<td>2</td>
<td>312.5</td>
<td>Ethernet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>156.25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>125</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>78.125</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>62.5</td>
<td></td>
</tr>
<tr>
<td>26.5625</td>
<td>24</td>
<td>637.5</td>
<td>3</td>
<td>212.5</td>
<td>Fiber Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>159.375</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>6</td>
<td>106.25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>12</td>
<td>53.125</td>
<td></td>
</tr>
<tr>
<td>19.44</td>
<td>32</td>
<td>622.08</td>
<td>2</td>
<td>311.04</td>
<td>SONET/SDH</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>155.52</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>77.75</td>
<td></td>
</tr>
<tr>
<td>38.88 (CMOS input)</td>
<td>16</td>
<td>622.08</td>
<td>2</td>
<td>311.04</td>
<td>SONET/SDH</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>155.52</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>77.75</td>
<td></td>
</tr>
</tbody>
</table>
MAX3671/3/8 Hitless Clock

One reference clock lost by Broken, Disconnect, Plug out
Detect
Lock to other reference clock

400ppm Frequency drift 0.02%/cycle Phase drift

MAX3671 : Ethernet
62.5, 125, 250, 312.5Mhz

MAX3673 : UMTS base Station
61.44, 122.88, 245.76, 307.2MHz

MAX3678 : Server/Storage clock
66.67, 133.33, 266.67, 333.33MHz
MAX3671/3/8 Measured Phase Noise

Output Frequency = 312.5 MHz
PLL Loop bandwidth = 40 kHz
Reference = external signal source (Agilent BERT + Agilent Frequency Synthesizer)

Integrated Phase Jitter = 0.25 ps rms from 12 kHz to 20 MHz
MAX3674 Programmable Frequency Synthesizer IC
Any Frequency from 21-1360 MHz

Features
- Very Low Jitter: 1.6ps RMS Cycle-to-Cycle, 0.9ps RMS Period
- Pin-Programmable Frequency from 21.25MHz to 1360MHz; Override Using I²C-Compatible Interface
- 7mm x 7mm, 48-Pin LQFP Package

Applications
- Frequency Margining for System ASICs
- Dynamic Power Management

Pin-for-Pin compatible to MPC92432 but with better Performance:
- 2-10x lower jitter
- 15 dB better PSNR
- 10% lower power
High Speed Data Converter

Maxim Integrated Products
Agenda Overview

• High Speed Data Converter
  – Maxim HS-Converter Product Families
  – HS-ADC/DAC Product Selection

• HS-ADC Design Considerations
  – Base Band Sampling versus IF Sampling
  – High Density Portable Application

• Design Solutions with HS-DACs
  – Cable Infrastructure Application
  – Wireless Infrastructure Application
Market Examples

- Base Stations
- Pt-2-Pt Microwave
- Satellite
- Cable Headends
- Ultrasound
- BWA Handsets
- Instrumentation ATE
- Military
Maxim HS-Converter Product Families

SSIP (High Speed Products)

High Frequency Signal Conditioning (RF)

High-Speed Data Converters

High-Speed ADC
- 6 to 16 Bits
- 5 Msps to 2.2Gsp
- Singles, Duals, Quads, Octals
- LVDS, CMOS, and Serial Interfaces

High-Speed DAC
- 8 to 16 Bits
- 40Msps to 4.3Gsp
- Singles, Duals
- LVDS, CMOS Interfaces

Analog Front End
- 8 to 10 Bits
- High-Speed ADC & DACs
- Integrated Auxiliary ADC & DACs
- Ultra-Low Power & Small Size
HS-ADC/DAC Product Selection: Parametric Search

HS- Converter = 1 Msps to 4.3 Gsps

- 82 introduced HS- ADCs
- 44 introduced HS- DACs
HS-ADC/DAC Product Selection : Solutions Finder

Example : Solutions for Wireless Infrastructure

Click on any block to drive down to greater detail...

Quick View Rider Redirects
✓ Component Overviews / Key Specs
✓ Data Sheets
✓ Apps Information
✓ Ordering Information
HS-ADC Design Considerations
Base Band Sampling vs. IF Sampling
Conventional Solution

Second Mixer (MAX2451) required to generate Base Band Signal
AD-Converter with low analog BW can be implemented (Low Power)
Base Band Sampling vs. IF Sampling
Advanced Solution

Without second Mixer the Signal is centered around IF-Frequency (higher Nyquist zones) requiring AD-Converter with higher input BW

IF signal is aliased back into baseband by sampling at fs.
Design Solution 1: High-IF Sampling Receiver

MAX12553/4/5: 14-Bit, 65/80/95Msps ADC
BEST HIGH IF DYNAMIC PERFORMANCE AT LOW POWER

Fs=65 Msps Fin=70 MHz

Performance Summary

<table>
<thead>
<tr>
<th></th>
<th>dBC</th>
<th>dBFS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>73.71</td>
<td>74.26</td>
</tr>
<tr>
<td>SFDR1</td>
<td>86.74</td>
<td>87.30</td>
</tr>
<tr>
<td>SFDR2</td>
<td>94.95</td>
<td>95.50</td>
</tr>
<tr>
<td>SINAD</td>
<td>73.31</td>
<td>73.86</td>
</tr>
<tr>
<td>THD</td>
<td>83.87</td>
<td>84.42</td>
</tr>
</tbody>
</table>
Design Solution 2: High-IF Sampling Receiver

MAX1213N/4N/15N: 170/210/250 Msps ADC

Excellent SNR/SFDR flatness over wide frequency range!
High Density Portable Application
Example: Medical Ultrasonic Design

N = up to 256!

http://www.maxim-ic.com/ejs/
(Engr. Journal Vol 60)
# High Density Portable Design Challenges

<table>
<thead>
<tr>
<th>Design Challenge</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Channel Count</td>
<td>Multiple Channel per Device</td>
</tr>
<tr>
<td>Limited Space</td>
<td>Serial Interconnects</td>
</tr>
<tr>
<td>Power Consumption Limitations</td>
<td>Low Power per Channel</td>
</tr>
<tr>
<td>Channel Cross Talk</td>
<td>High Isolation</td>
</tr>
</tbody>
</table>
Solution: MAX1434-1438 (ADCs for Ultrasound)

OCTAL 12-BIT 40/50/65 MSPS ADC WITH ULTRA-LOW POWER

Outstanding Dynamic Performance
- 69.6dB SNR at f_{IN} = 20MHz
- 90dBc SFDR at f_{IN} = 20MHz
- -95dB Crosstalk

20% to 50% Lower Power than the Competition
- 93mW per Channel (MAX1436)
- 96mW per Channel (MAX1437)

<table>
<thead>
<tr>
<th>Part</th>
<th>No. of Channels</th>
<th>Resolution (Bits)</th>
<th>Speed (MSPs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX1127</td>
<td>4</td>
<td>12</td>
<td>65</td>
</tr>
<tr>
<td>MAX1126</td>
<td>4</td>
<td>12</td>
<td>50</td>
</tr>
<tr>
<td>MAX1438*</td>
<td>8</td>
<td>12</td>
<td>65</td>
</tr>
<tr>
<td>MAX1437</td>
<td>8</td>
<td>12</td>
<td>50</td>
</tr>
<tr>
<td>MAX1436</td>
<td>8</td>
<td>12</td>
<td>40</td>
</tr>
<tr>
<td>MAX1434</td>
<td>8</td>
<td>10</td>
<td>50</td>
</tr>
</tbody>
</table>

Less than 100mW per channel

SERIAL LVDS REDUCES ROUTING AND PIN REQUIREMENTS BY MORE THAN 4x
Design Solutions with HS-DACs
Cable Infrastructure Application Example

1) Baseband Synthesis
   - FPGA or ASIC
   - 14/16-Bit DAC
   - MAX5895/8 MAX5874
   - Clock Synthesizer
   - f_CLKR

2) Up-Conversion
   - MAX2021/2/3
   - Frequency Synthesizer
   - Fixed LO
   - f_LO1
   - f_LO1 + f_IF

3) Down-Conversion
   - Agile LO
   - f_LO2
   - Frequency Synthesizer
   - Upstream
   - Downstream
   - 50 – 1000 MHz RF

PA
FILTER BANK
ATTN.
MAX5881: 12-Bit 4.3 Gsps DAC for Cable Infrastructure

- Industry-leading dynamic performance
- Supports up to four 6MHz+ QAM channels
- ACP2 = -67dBc at f_{OUT} = 1000MHz (6MHz offset)
- ACP3 = -68dBc at f_{OUT} = 1000MHz (12MHz offset)
- ACP4 = -69dBc at f_{OUT} = 1000MHz (18MHz offset)
- Data source (FPGA) board available

- 4.3Gsps output-update rate
- Direct RF synthesis: 50MHz to 1000MHz
- Low power: 1.2W at 4.0Gsps
- 4:1 multiplexed LVDS inputs
- 11mm x 11mm, 169-pin CSBGA package
- Evaluation kit available
Wireless Infrastructure Application Example

Zero-IF Transmitter (DAC) & High-IF Transmitter (DAC)
Zero-IF (ZIF) Transmitter

MAX5873-8: Dual 16/14/12-Bit 200/250Msps DACs
MAX5893-8: Dual 16/14/12-Bit 500Msps Interpolating DACs

INDUSTRY LEADING DYNAMIC PERFORMANCE AT LOW POWER
High-IF Injection Transmitter

MAX5889/90/91: 12/14/16-Bit 600 Msps DACs

- Outstanding Dynamic Performance
  - SFDR = 84dBc at f_{OUT} = 16MHz
  - Two-Tone IMD = -94dBc at f_{OUT} = 30MHz
  - Noise Density = -163dBFS/Hz at f_{OUT} = 36MHz
  - ACLR = 73dB at f_{OUT} = 123MHz

- Low-Power Operation: 298mW at 600Msps
- Pin-Compatible 12-/14-/16-Bit Versions
- LVDS and CMOS Input Interface Options
- Evaluation Kits Available

<table>
<thead>
<tr>
<th>Part</th>
<th>Resolution (Bits)</th>
<th>Update Rate (Msps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX5861</td>
<td>16</td>
<td>600</td>
</tr>
<tr>
<td>MAX5860</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>MAX5869</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>MAX5868</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>MAX5867</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>MAX5866</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>MAX5865</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>MAX5864</td>
<td>14</td>
<td>500</td>
</tr>
<tr>
<td>MAX5863</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>MAX5863</td>
<td>12</td>
<td>200</td>
</tr>
</tbody>
</table>
Thank you!