Using an I/Q interface in radio transceivers

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This article introduces the use of digital demodulators for data communications. Conventional FM receivers use an analog demodulator, such as a phase-locked-loop or, more commonly, a limiter-discriminator.

Digital schemes replace these with digital processors. This article discusses the general issues surrounding digital demodulators, using a marine Automatic Identification System (AIS) as an example.

The AIS technology is a data signaling system that uses a version of the time-division multiple access (TDMA) scheme known as self-organizing TDMA. The modulation used is Gaussian-filtered minimum-shift keying (GMSK)/Gaussian frequency-shift keying (GFSK) at a data rate of 9.6Kbps in 12.5kHz or 25kHz channels.

The transmitter modulation can be developed by either a digital modulator or traditional analog methods (Figure 1). It can also be used to generate MSK, but this relies on the VCO gain constant to be precisely known and invariant. Hence, MSK modulation in analog implementations of this scheme is not practical.

This modulation scheme has much in common with traditional FM modulation used for voice communication. This suggests that the same type of receiver structures may be used for this data system as in conventional FM receivers. The classic limiter-discriminator architecture has been adopted in a number of AIS designs.

Receiver architectures for wireless data systems can be broadly classified as digital and analog, depending on what means are used to perform FM demodulation.

The analog demodulator approach uses a classic limiter-discriminator (Figure 2). In this scheme, the received signal is amplified such that any amplitude variation caused by the RF path is removed. The resulting signal is delayed and mixed with the original signal to render a different signal output—this represents the frequency/phase modulation in the incoming signal. This is called differential detection and the circuit is known as a discriminator.

Following the discriminator, the modulation looks like an analog data stream. To recover data, the bit-timing must be determined and a decision must be made on whether the signal, at any particular instant, represents a “1” or a “0.” Data recovery is done by some method of “data-slicing,” followed by a timing recovery circuit. The data recovery mechanism is critical, as the output of the analog discriminator can sit on a varying DC level.

The analog scheme is well-proven, but it also has two drawbacks. The first is the need to deal with DC drift in the demodulated output. The second, and probably more significant, is the need to implement all receiver filtering prior to the limiter using analog filters, with obvious trade-offs in size and cost.

The digital demodulator converts the analog signal into a digital representation prior to demodulation. Two common approaches to implement this would be to sample at a low IF (e.g. about 455kHz), or to mix the signal down to baseband, where in-phase (I) and quadrature (Q) components are required to retain all the information in the signal. Both IF sam-
These filters are relatively large and expensive. Furthermore, the filters require careful matching to ensure that optimum characteristics are achieved. Temperature and aging can cause the filter response to vary, affecting the receiver’s overall performance.

A study of filter responses shows that it is difficult to achieve the AIS-specified adjacent channel rejection with crystal filters alone. The problem is that the roll off is just not fast enough to remove the power in the part of the adjacent channel closest to the required. To achieve this, rejection ceramic filters are generally used in a second IF (e.g. 455kHz).

Both crystal and ceramic filters exhibit significant group-delay ripple, as can be seen in various plots. In analog voice systems, this can be tolerated without any problem, but in digital systems, this will distort the digital signal and result in a higher error-rate in the receiver.

Consider the received signal prior to data slicing, but after the data filter. This signal, when displayed (e.g. on an oscilloscope), is known as an eye diagram. Figure 4 shows the results from a receiver without a crystal filter showing a clean “eye” with well-defined zero crossings. Figure 5 shows results from the same receiver with the same input signal, but with a crystal filter added. The phase distortion introduced by the filter causes both a closing of the “eye” and significant jitter on the zero crossings.

The group-delay variation caused by analog filters can be avoided using a digital filter. The FIR filter implemented in the CML AIS baseband processor chip (CMX910) has a constant group delay, resulting in a linear phase response (Figure 6). When the AIS received data is passed through this filter, there is no degradation of the sensitivity or jitter introduced in the zero crossings. The FIR filter also provides excellent rejection of the adjacent-channel signal and greater than 60dB is achieved. This rejection means that the IF ceramic filters are not required. Typically, however, a crystal filter would still be used in the first IF stages to limit the dynamic range presented to the ADC; however, rejection requirements are relaxed. By minimizing the analog filtering requirements, the digital approach can save PCB area, reduce material costs and improve sensitivity and co-channel performance. The improvement in co-channel performance is a result of the improved group delay.

**Filter design**

To optimize the receiver filtering, it is necessary to consider the amount of rejection required from each filtering stage. With a digital interferer, it is necessary to calculate the rejection of that signal by applying the filter response to the modulation spectrum. An example is shown in Figure 7 for the rejection of a digital interferer with a constant group delay.
Digital receivers often use digital filters attenuation using C4FM modulation passed through analog filters (crystal) and then digital filters (using CMX981).

The analog filter is relatively wide and thus provides little degradation of passband characteristics. The attenuation achieved is enough to limit the dynamic range of the signal so that minimum power consumption is required for I/Q downconverters. This limits the dynamic range required on the ADC, thus reducing the need for AGC and improving SNR margins. Good adjacent channel rejection is achieved in the FIR and it is clear how the two filters are complementary.

**Dynamic range partition**

In a digital demodulator, the received signal is sampled by an ADC. Figure 1 shows an example of a dynamic range partition based on an ADC with 85dB range and a maximum input signal of 600mVrms (+8.6dBm assuming a 50° input impedance for convenience). A typical design methodology is to consider the range at the top and bottom, leaving an operating window in the middle.

The bottom of the dynamic range is the minimum signal level that the ADC can quantize. Hence, to prevent quantization-noise that degrades overall receiver performance—the signal should be well above this level. A 10dB margin between thermal and quantization noise is typical. To calculate the minimum signal level, the SNR of the receiver must be added to the thermal noise.

A further margin can be added to allow for variation in SNR with, for example, frequency offsets and filter variations. In Figure 8, this results in a minimum input signal to the ADC of -53.4dBm.

The maximum operating signal level is set by the level of filtering that the baseband FIR filters must perform. In the example, we assume that we wish to attenuate a signal 35dB above the target. It is also prudent to allow some margin on the maximum signal. This sets an upper limit on a wanted signal that can be presented when an adjacent channel interferer is expected.

Given the partition shown in Figure 8, the total receiver gain can now be calculated.

![P25 C4FM modulation filter attenuation](image)

Note that units of dBm are used for simplicity in these calculations, although the actual impedance at the ADC input will not be 50°. Using the power equivalent in 50° means that gains through the receiver chain can be evaluated independently of impedance. The following assumptions are used in this calculation:

- Interferer measurements are at 3dB above sensitivity limit;
- Best-case receiver sensitivity is -120dBm;
- Worst-case receiver sensitivity is -110dBm.

Minimum gain can be calculated as:

- Minimum operating point of ADC = -53.4dBm;
- Minimum input level (maximum sensitivity) = -120dBm;
- Maximum Rx path (voltage) gain = 66.6dB.

Maximum gain can be calculated as:

- Maximum operating point of ADC = -29.4dBm;
- Maximum input signal level at sensitivity = -110dBm;
- Degradation measurement level = 3dB;
- Maximum Rx path (voltage) gain = 77.6dB.

This leaves an 11dB window in which to set the nominal gain of the receiver. A nominal value may, for example, be 72dB.

Digital receivers often use AGC to ensure a wide linear dynamic range. This is essential for linear modulations where amplitude is a component of the signal. For GFSK/GMSK systems, this is not strictly necessary, as these are phase/frequency modulations and no information is contained in the amplitude. As a result, the AGC stage in Figure 3 is not strictly necessary. In this case, the RF designer should pay careful attention to the levels through the receiver and ensure that compression and limiting occur at an appropriate point. It is essential to ensure that the ADC does not over-range and so compression in an analog stage should be arranged to prevent such problems.

The filtering achieved by an FIR filter in the receiver is only usable if the ADC can sample a wanted signal and interferer such that attenuation can be applied. It should be pointed out that the filter will typically reject the wanted signal by more than the given headroom in the dynamic range partition.

Consider the CMX910 (AIS processor) filter response in Figure 6. This shows that the FIR will reject an interferer at 25kHz offset by more than 70dB. If the dynamic range partition is used with this filter and the AIS-specified interferer at 60dB above the wanted is applied, the ADC will be driven into saturation and the targeted data will likely be destroyed.

Correct operation of the system would be to limit the signal applied to the ADC to 35dB above the wanted signal (by using filtering in the first IF). The digital filter will now reject the adjacent signal to about 35dB below the target, allowing the demodulator to recover the wanted signal correctly.

Note that the operating window (Figure 8) gives a range over which the full adjacent channel rejection of the receiver can be maintained, and AGC can be used to maintain the signal within this win-
However, adjacent channel selectivity is typically only tested close to sensitivity. Thus, the signal can be allowed to rise up the converter range, degrading adjacent channel rejection in relative terms, although the absolute level of any interferer remains the same.

DC offsets can cause problems within I/Q digital architectures, so steps are required to prevent such problems. As the signal is mixed to baseband, some DC will be present, which will be captured by the ADC as the signal is converted to the digital domain. As the received signal may be small, perhaps just a few mV, and any level of DC needs to be well below the signal level, it is clear that the tolerable DC offset is generally very small. Such small levels are easily generated by any imperfection, even in the best-designed analog mixers and amplifiers.

To remove the DC offset, a number of techniques can be used. Averaging the received signal and removing the DC can be an effective solution. However, great care is needed with such a scheme, as the modulation content of the received signal can affect the result. Averaging over a very long time can also be problematic. DC offset removal is therefore best considered when details of the signal to be received are known.

If initial DC calibration can be performed in the presence of noise (no signal), then averaging can be much faster, as the potential DC content of the data can be ignored. This allows a rapid measurement of the DC offset. To ensure that no signal is present, it is often beneficial to arrange that some sections of the RF circuitry be isolated or powered down. Clearly, it is essential that circuits that may contribute to the DC offset are undisturbed.

An example of this scheme is shown in Figure 9. As will be seen, this particular circuit can be put into an I/Q DC offset-acquire mode during which the first stages of the receiver are disabled. The IF and I/Q circuits remain powered and a rapid measurement of DC offset is made. When normal operation is enabled, the measured DC offset is automatically subtracted from the data, resulting in effective DC offset removal.

**AC coupling**

One simple solution to DC offset problems is to AC couple the baseband signal to the ADC. The problem with this action is that long sequences of 1’s or 0’s could be corrupted due to the data decaying with the time constant associated with the coupling capacitor. For the AIS system, bit stuffing is used to limit the maximum run length in the data, thus, it would appear that AC coupling is a practical solution.

Unfortunately, things are not that straightforward. In the case of AIS data (and many other TDMA systems), the signal is bursty in nature and a strong signal received in one time slot can be followed by a much weaker one in the next. With AC coupling, the large signal may still be decaying when the weaker signal arrives, causing a DC slope that is difficult to remove.