A High-Speed Variable Phase Accumulator for an ADPLL Architecture

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Abstract—This paper presents a high-speed topology for the variable phase accumulator (VPA) in an all digital phase-locked loop (ADPLL) architecture. The topology increases the speed of the VPA, which is a digital block running at the highest frequency in the ADPLL. The high-speed feature of the topology is achieved by exploiting the fact that the VPA output is used in the reference frequency domain while the circuit needs to handle the RF signal from the ADPLL output. The new topology minimizes the timing critical path and reduces the logic in the highest frequency domain to a shift register. As demonstrated in a 65-nm CMOS process, it allows the VPA to have a speed increase of about 60% without penalty in power dissipation or silicon area.

I. INTRODUCTION

There has been a trend for over a decade to implement RF functions in integrated circuits (IC) in a way that is compatible with digital IC technology. This is very desirable not only to enable higher integration level when analog functions can be combined with digital ones but also to cope with the steady scaling of the device dimensions and supply voltage.

A particularly successful approach for implementing a frequency synthesizer in a digital way was recently introduced in [1] [2], which is based on an all digital phase-locked loop (ADPLL) as shown in Fig. 1. In the ADPLL, the digital input to the digitally controlled oscillator (DCO) determines its output frequency. The phase information of the DCO output is then digitized and fed back to the loop control circuitry, which tunes the digital input to the DCO to eliminate the phase error. The digitization of the DCO phase information is accomplished with the variable phase accumulator (VPA) keeping track of the full RF cycles and the time-to-digital converter (TDC) adding sub-cycle resolution. Analog blocks in a conventional PLL such as the phase/frequency detector, the charge pump and the loop filter are replaced with digital circuits in the ADPLL architecture.

The digital approach makes the ADPLL architecture fully compatible with digital IC technology, offering many advantages such as small silicon area, possibility for adaptive loop filtering and wideband frequency modulation. However, digital circuits synthesized using standard cell libraries are usually weaker in dealing with high frequency signals than analog counterparts using custom design. High-speed circuit techniques often available for a custom design are usually not accessible from a standard digital flow. Consequently, convenient applications of the ADPLL architecture have so far been limited to the lower part of RF range, while conventional PLLs can be designed to synthesize frequency up to tens of gigahertz [4].

The highest operating frequency in the ADPLL architecture is at the output of the DCO, where the TDC, the retimer and the VPA have to work with the RF signal. In order for the ADPLL to produces high frequency signal, these circuit blocks must be capable of high-speed operation. Circuit techniques and topological methods with semi-custom design as proposed in [3] allow the TDC to work with almost any high frequency that can be produced by the oscillator. The frequency reference retimer, which can be simply a D-flip-flop, also has little difficulty working at a relatively high frequency. The VPA in contrast has been the weakest block for high frequency operation, as it has more complexity than the retimer block and at the same time it needs be synthesized as part of the digital loop circuitry using standard digital flow to facilitate the ADPLL implementation. Therefore, any improvements introduced to increase the VPA speed will make the ADPLL more robust for high frequency operation and potentially lead to its higher frequency applications.

In this paper, we present a topology that allows the VPA to work at substantially higher frequency. It takes the advantage of relatively low sampling frequency at the VPA output to minimize the timing critical path in the high frequency domain. First, a review of previous work done on the VPA design is given in section II. Then the proposed topology is described in section III.

II. PREVIOUS WORK

The VPA can be realized using a modulo binary incrementer (counter) followed by a sampling register [2]. The basic topology is shown in Fig. 2, where CKV is the RF output
Fig. 2. A basic topology of the VPA

Fig. 3. Incrementer with separate logic for higher and lower order bits

The high-speed signal CKV is used to clock the incrementer so that the increment occurs for each cycle of the high-speed clock. The sampling register is run by the relatively low-speed clock CKR, which means the incrementer content is presented at the VPA output once every cycle of the low-speed clock. The VPA output is an unsigned binary word, as is needed by the subsequent digital circuit in the ADPLL loop.

As indicated in [5], if the carry-ripple structure is used for an 8-bit modulo incrementer, the timing critical path would be a chain of seven half-adders and an inverter. Based on the well-defined pattern of an incrementer output sequence, circuit techniques have been explored in [5] to shorten the timing critical path and thus speed up the incrementer. First, the increment logic is divided into two parts respectively for lower and higher order bits, which transforms the binary incrementer into two smaller sub-incrementers as shown in Fig. 3. The higher-order sub-incrementer is triggered when the lower-order sub-incrementer output reaches its maximum value “11”, which allows its operation to take four clock cycles of CKV. To further speed up the incrementer, the increment trigger path is split into two clock cycles with due adjustment of the logic as shown in Fig. 4.

Depending on implementation, the new timing critical path can be one of the following.

1) from the register output back to the register input through the half adder in the lower order sub-incrementer,

2) from the register output in the lower order sub-incrementer to the flip-flop input in the increment trigger path, and

3) from the flip-flop output in the increment trigger path to the register input in the higher order sub-incrementer.

These paths are shorter than the one in the 8-bit carry-ripple structure, which allows the incrementer to operate faster. However, for a high frequency operation, the extra logic and parasitic capacitance in these paths still takes significant toll in delay and limits the clock rate of CKV in circuit implementations.

A number of different designs exist for a binary incrementer (counter) [7] [8]. However, not specialized for the VPA application, they do not provide further substantial speed improvement.

III. PROPOSED TOPOLOGY

A. Topology Overview

The new topology is shown in Fig. 5 for an 8-bit VPA. It comprises a 6-bit binary incrementer clocked by CKVD4, a shift register clocked by CKV, sampling registers clocked by CKR, and a combinatorial 4-to-2 encoder following the sampling register. The CKVD4 is a divide-by-4 clock from CKV.

The 6-bit binary incrementer and the shift register in combination can be considered as a segmented incrementer. The incrementer output is a concatenation of a binary part for the higher order bits and a non-binary part for the lower order bits. The non-binary part is then transformed into binary form using the encoder following the sampling register so that the whole VPA output is a binary word.

In the high frequency clock domain of CKV, the circuitry is now reduced to a shift register with no extra logic between the flip-flops. The clock rate of CKV is therefore limited only by the time required for loading a flip-flop. As CKR is a low frequency clock, the 4-to-2 encoder in this clock domain is no concern in terms of operation speed.
B. Logic Description

Suppose the sampling registers is removed from the VPA. We would obtain a circuit as shown in Fig. 6. This circuit resembles the 8-bit incrementer in Fig. 4 in that it is also partitioned into two parts. By comparison, it can be shown that it is actually an 8-bit incrementer.

First, the upper block is a simple incrementor clocked by CKVD4, which means the increment occurs every four cycles of CKV. Therefore, its output is equivalent to the six higher order bits of an 8-bit incrementer clocked by CKV. This is the same function performed by the corresponding higher order sub-incrementer as shown in Fig. 4, where the sub-incrementer is clocked by CKV but with the increment operation triggered only for every four cycles.

The serial-in parallel-out shift register in the lower part of the circuit is reminiscent of a special category of non-binary counters, shift register counters. The LSB of the 6-bit higher order incrementer, \( R[i][2] \), toggles every four clock cycle of CKV. If we look at \( R[i][2] \), we see a sequence as shown in Fig. 7 updated every cycle of CKV. It can be recognized that the sequence pattern is the same as the one from a 4-bit Johnson counter. Therefore, from functional perspective, the shifter register along with its input bit forms a non-binary sub-incrementer (counter) that is aligned with the higher order sub-incrementer. The non-binary sub-incrementer is comparable to the lower order sub-incrementer in Fig. 4 with difference only in the coding format. The task for the encoder is thus to convert the output of the non-binary sub-incrementer into binary form. The encoding logic can be easily derived by just checking the corresponding lower order bits output sequence of a general incrementer and comparing it to the sequence in Fig. 7. Alternatively, we can consider the 8-bit incrementer as shown in Fig. 3, where the higher order increment is triggered when the lower order sub-incrementer output reaches the state of “11”. Table I is the truth table for the encoding logic, which can be synthesized in a straightforward way using any hardware description language.

From above, we see that the circuit as shown in Fig. 6 is an 8-bit incrementer formed by two sub-incrementers. However, if we were to sample its output directly to construct a VPA, the 4-to-2 encoder would work in the CKV clock domain and its delay would limit the CKV frequency. Fortunately, there is no feedback from the encoder output to any part of the incrementer, and the output is hence only needed at the relatively low frequency of the sampling clock CKR. This allows us to place the encoder after the sampling registers and leads to the proposed VPA topology.

The clock signal CKVD4 in the proposed VPA topology can be generated from CKV with a simple divide-by-4 circuit (Fig. 8). Meanwhile, as a frequency divider is also needed for...
DCO capacitance dithering in the ADPLL architecture, it is possible for CKVD4 to be generated by the same frequency divider. As a result, the proposed VPA topology in many cases does not require an extra frequency divider.

![Fig. 8. A digital divide-by-4 circuit](image)

It should be noted that though an 8-bit VPA has been used as an example for illustration, the proposed VPA topology imposes no restriction on the word length. We may also change the size of the higher-order sub-incrementer with the length of the shift register changed accordingly. Take the 8-bit VPA for instance. We may use a 5-bit higher order sub-incrementer running at a divide-by-8 clock from CKV. Then the shift register for the lower order bits will consist of seven flip-flops and an 8-to-3 encoder will be needed. In addition, the topology does not rule out use of other techniques in the higher-order sub-incrementer. When necessary, the higher-order sub-incrementer can be constructed in a way like the 8-bit incrementer shown in Fig. 4.

C. Performance Study

In our work, two VPAs, one of previous work (Fig. 4) and one of the proposed topology (Fig. 5), were first coded using VHDL and then synthesized with Synopsys Design Compiler using standard cell libraries with a 65-nm CMOS technology. The design using the proposed topology was able to be synthesized for a CKV of 3.7 GHz without timing violation, while the one of previous work can only be synthesized for a CKV of 2.3 GHz. At operating frequency of 2.3 GHz, the design using the proposed topology has a power dissipation of 148 μW, while the one of previous work consumes 304 μW. Also, the design using the proposed topology has a cell area of 226 μm², while the one of previous work 254 μm². The results are summarized in Table II.

The worst case delay introduced by the 4-to-2 encoder was found in the synthesis to be about 0.17 ns. This delay is negligible considering one period of CKR at a typical frequency 26 MHz is about 40 ns. Moreover, the output from the TDC in the ADPLL architecture has much larger delay, which means that the critical path in the CKR domain are among those from TDC output and the delay introduced by the encoder is therefore not a concern in terms of timing budget.

It is expected that both of the VPAs could potentially work at a higher frequency if custom design flow were to be employed instead of the standard cell synthesis. However, the one using the proposed topology should have larger room for improvement, considering that the speed limitation now mainly comes from setup time and output delay of a flip-flop, and custom design can utilize well-known techniques to speed up the flip-flop reducing both setup time and output delay.

IV. Conclusion

We have presented a high-speed topology for the VPA used in an ADPLL architecture. With the proposed VPA topology, the logic in the highest frequency domain is reduced to a shift register. Synthesized using standard cell libraries from a 65-nm technology, a VPA using the proposed topology showed a speed improvement by 60% over previous work, with reduced power consumption and no penalty in silicon area.

One drawback of the proposed topology is that it needs an extra derived clock signal like CKVD4 in the example. Nonetheless, it can be easily realized with a simple clock divider capable of fast operation. Moreover, such a clock divider is also needed in some other part of the ADPLL architecture and it can be shared by the VPA, therefore the proposed topology does not require an additional clock divider in most cases.

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