PERFORMANCE ANALYSIS OF THE GARDNER TIMING DETECTOR
OVER $\pi/4$-DQPSK MODULATION

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ABSTRACT
This paper presents the simulation performance of the all-digital symbol timing recovery using the Gardner Timing Error Detector over $\pi/4$-DQPSK modulation. The open loop statistics, the S-curve and the normalized timing error variance, were investigated to show the stable tracking performance of the system. The symbol timing recovery has a second order loop transfer function, which was able to track down phase, and frequency offsets. Modulation was observed to have a performance of 2 dB lower from the theoretical BER curve.

1. INTRODUCTION
Symbol Timing Recovery (STR) or Clock Synchronization is the process of recovering the optimum sampling time that corresponds to the maximum opening of the eye diagram. This process is often overlooked but it is in fact the most critical in the design of digital communication systems: its failure has devastating effects in the receiver data [1]. The inherent problem of clock synchronization is that sampling clock of the receiver, $T_s$, is not synchronized to the strobes of the transmitter, $T_i$ [2]. This paper presents the simulation of the all-digital symbol timing recovery proposed by Gardner on the $\pi/4$-DQPSK modulation using the Intermediate Frequency (IF) signal. The performance and the feasibility of the symbol timing recovery shall be assessed by examining its open loop and closed loop characteristics. In addition, the synchronization performance under an Additive White Gaussian Noise (AWGN) channel will be presented.

2. BASEBAND MODULATION AND DEMODULATION
The $\pi/4$-DQPSK is a differentially encoded modulation [3]. The information contained in the phase transition

$$\Delta \theta_n = \theta_n - \theta_{n-1}$$ (1)
rather than the phase itself as in M-PSK. The block diagram of baseband modulation and demodulation is shown in Figures 1 and 2 respectively. The pseudo-random bit stream is converted from serial to parallel to form a dibit stream $A_nB_n$. The Gray-coded dibits are differentially encoded in Figure 3.

![Figure 1. Baseband Modulation](image1)
![Figure 2. Baseband Modulation](image2)
![Figure 3. Gray-coded Differential Encoding](image3)
\[ I_n + jQ_n = \exp(j2\pi n/8) \quad 0 \leq n \leq 7 \] (3)

The in-phase and quadrature phase components were pulse-shaped at \(N=4\) samples per symbol using a 32-tapped Nyquist’s root raised cosine filter \(g_r(t)\) with a roll-off factor, \(\alpha = 0.35\), to minimize the Intersymbol Interference (ISI) [5]. The pulse-shaped complex envelope of the signal is thereby represented by [6]

\[ X(t) = \sum_{n=-\infty}^{\infty} (I_n + jQ_n) \cdot g_r(t - nT) \] (4)

where \(T\) is the symbol period. The transmitted samples are simulated over an AWGN channel.

The receiver samples on the other hand were filtered using the same Nyquist filter \(g_r(t)\) to match \(g_r(t)\) [4]. The cascaded filter response is a Nyquist raised cosine filter with a response

\[ g(t) = g_r(t) \ast g_r(t) = \frac{\sin(\pi t/T)}{\pi t/T} \cdot \cos(\pi \alpha t/T) \frac{1}{1 - 4\alpha^2 t^2/T^2} \] (5)

The differential detection equations [7] are solved from (3)

\[ \hat{i}_n = \cos \theta_n = \frac{Q_n I_{n+1} + I_n I_{n-1}}{I_{n-1}^2 + Q_{n-1}^2} \]
\[ \hat{q}_n = \sin \theta_n = \frac{Q_n I_{n+1} - I_n I_{n-1}}{I_{n-1}^2 + Q_{n-1}^2} \] (6)

since \(I_{n+1}^2 + Q_{n-1}^2 > 0\) is common to both sides, then we assign

\[ U_n = Q_n I_{n-1} + I_n I_{n-1} \]
\[ V_n = Q_n I_{n-1} - I_n I_{n-1} \] (7)

the dibit stream \(\hat{A}_n\hat{B}_n\) is recovered and finally converted from parallel to serial according to the following decision rule

\[ \hat{A}_n = \text{sgn}(-U_n) \]
\[ \hat{B}_n = \text{sgn}(-V_n) \] (8)

where \(\text{sgn}(t)\) is the hard-limiter signum function.

3. SYMBOL TIMING RECOVERY

The loop shown in Figure 4 is an asynchronous, non-data aided, all-digital symbol timing recovery proposed by Gardner [2]. It consists of an Interpolator, Timing Error Detector (TED), Digital Loop Filter, and a Numerically Controlled Oscillator (NCO). Its algorithmic structure of the all-digital STR paves its way in its implementation at the baseband level using Discrete-time (Digital) Signal Processing (DSP) [8]. The all-digital symbol timing recovery is a feedback timing error synchronizer that can be characterized as a Phase-Locked Loop (PLL) [9], [10]. The loop parameters are designed based on the linearized model of the PLL.

![Figure 4. All-Digital Symbol Timing Recovery](image)

3.1. Interpolator

The interpolator computes the intermediate values between the adjacent signal samples \(Y(kT)\) [9]. Polynomial Interpolators, which can be derived using Lagrange’s interpolation formula [11], has an advantage that it can be designed easily using time-varying Finite Impulse Response (FIR) filters [12]. The simplest yet robust polynomial interpolator is a linear interpolator [9]

\[ Z(kT) = Y(m(k)T) + \mu(k) \left[ Y((m(k)+1)T) - Y(m(k)T) \right] \] (9)

where \(m(k)\) is called the basepoint index and \(\mu(k)\) is called the fractional index.

3.2. Timing Error Detector

The TED compares received waveform with the locally generated signal in every symbol period. Gardner proposed a non-data aided TED known as the Gardner detector (GAD) based on the Maximum-Likelihood (ML) estimation [13], [14]

\[ V_d(k) = \text{Re} \left\{ Z(kT) - \frac{T}{2} \left[ Z(kT) + Z(kT + T) \right] \right\} \]

(10)

3.3. Loop Filter

For most practical systems, phase and frequency offsets occur. Frequency offsets are caused by the difference in the sampling rate of the transmitter and the receiver [9], [15] or for wireless application, caused by Doppler shift [15], [16]. Thus, the loop filter should be able to track out phase errors and frequency errors. An appropriate loop filter is a proportional plus integral (PI) configuration [17]. The closed loop transfer function, which has a stable second-degree transfer function, can track out phase and frequency offsets.

3.4. Numerically Controlled Oscillator

The NCO controls the estimated timing of the loop. The control word \(V_0\) is updated every symbol period with the following algorithm [9]

\[ V_0(rN) = V_0((r-1)N) + K_r V_d(rN) \] (11)
where $K_0$ is the NCO constant and $r$ is a positive integer. The basepoint index and the fractional index are updated with the following algorithm [9]

$$m(k + 1) = m(k) + \left\lfloor \mu(k) + V_o(k) \right\rfloor$$

$$\mu(k + 1) = \text{mod}(\mu(k) + V_o(k), L)$$

which is fed to the time-variant FIR linear interpolator.

4. OPEN LOOP SIMULATION

The open loop simulation is critical in determining the tracking performance of a timing error detector over a modulation scheme. Open loop characteristics under investigation are the S-curve and the Normalized Timing Error Variance.

4.1. The S-Curve

The S-curve is a measure of expectation error for a given normalized timing offset of the TED, which is expressed as [14]

$$S(\hat{\tau}) = E[V_o(\hat{\tau})]$$

The simulated S-curve in Figure 5 shows that for zero timing offset $\hat{\tau} = 0$, the S-curve is at the origin. For small timing offsets on the S-curve and thereby, the linear model can be applied. The S-curve plot in Figure 5 signifies that the Gardner TED is feasible for π/4-DQPSK Modulation.

4.2. Normalized Timing Error Variance

The normalized timing error variance $\sigma^2$ is plotted in Figure 6 as a function of the normalized loop noise bandwidth $B_L T$ over an AWGN channel. There are two observations that can be inferred in the graph.

First, the normalized variance is much less than unity, $\sigma^2 << 1$ in the practical range of $B_L T \in [10^{-4}, 10^{-1}]$, and thereby the timing jitter is manageable. The trade-off in reducing $B_L T$ will improve the loop SNR, however this will result to a decrease in the natural frequency $\omega_n$, which will slow down the transient response as well as decrease lock-in range, $\Delta\omega_L$.[18].

Second, variance starts to settle at around $E_b/N_0 = 15$ dB. The settling of variance at higher $E_b/N_0$ indicates the inherent self-noise generated by the Gardner TED [14]. The self-noise generated by the TED shall be exhibited in the closed loop simulation of the STR.

5. CLOSED LOOP SIMULATION

The closed loop all-digital symbol timing recovery is simulated over a phase step and a frequency step. The loop is designed with a loop bandwidth $B_L T = 1.5 \times 10^{-3}$. The fluctuations in the graph manifests the self-noise produced by the TED.

5.1. Phase Step

The phase step simulation was set with a timing offset of $\hat{\tau} = -0.500 T_s = -0.125 T$. Figure 7 shows the steady state error from its maximum at the start of the simulation and settling down to zero. Hence, the symbol timing recovery was able to track out phase offsets. The control word plot in Figure 8 has pulled back in order to compensate the phase offset before settling into the steady state. The plots in Figures 7 and 9 show that the phase offset are eliminated within 500 samples. The fractional steady-state index response fluctuates yet settles at $\mu = 0.5$. 

![Figure 5. S-curve plot](image)

![Figure 6. Normalized Timing Error plot](image)
5.2. Frequency Step

The frequency step is simulated by resampling the IF signal at 1.001 of the original sampling frequency or a frequency step 1/1000 of the sampling frequency. Figure 10 shows that the steady state error settles down to zero, and hence the symbol timing recovery was able to track frequency offsets. The transient response in Figure 11 showed the frequency acquisition in the STR. Interpolation takes place every \( T_i = 1.001T_s \) at steady state form \( T_i = T_s \). As consequence of frequency shift, the shift in sampling from four samples per symbol to five samples per symbol occurs once in 250 samples as shown in Figure 12. The straight line shows, the steady state value \( V_{\text{e}(k)} = 1.001 \).

5.3. Performance Under AWGN Channel

The comparative Bit Error Rate (BER) curve over the AWGN channel using \( 1 \times 10^5 \) bits is shown in Figure 13. The approximate BER for \( \pi/4\)DQPSK [19] is based on the equation (15)

\[
P_b = \sqrt{\frac{2(2 - \sqrt{2}) E_b}{N_0}}
\]  

The simulated BER curve has a degradation performance of around 2 dB due to the non-idealities of the STR. Synchronization failure is empirically expressed in terms of probabilities. The conditional probability, \( P[\text{unlock} | \tau = 0] \) during the first \( 1 \times 10^4 \) bits is empirically plotted in Figure 14.
The probability of synchronization failure below 3 dB is practically unity attributed by excessive noise, thus reliable BER performance cannot be performed. Above 8 dB, the probability of synchronization failure is practically zero. 8–10 dB of $E_b/N_0$ is recommended to achieve safe locking of the synchronizer. The simulation achieved a BER of $10^{-4}$ at 13 dB.

6. CONCLUSION

The open loop simulation has shown that the Gardner TED over $\pi/4$-DQPSK modulation has a stable tracking performance thus it can be used for the closed loop symbol timing recovery. Furthermore, the Gardner TED symbol timing recovery was able to track down phase and frequency offsets attributed by the stable second order transfer function of the closed loop. In addition, it has shown a satisfactory BER performance of $10^{-4}$ at $E_b/N_0=13$ dB over the AWGN channel. Therefore, the all-digital symbol timing recovery proposed by Gardner can be used over the $\pi/4$-DQPSK modulation in the clock synchronization of the receiver.

REFERENCES