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1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320F2810 and TMS320F2812 digital signal processors, silicon revisions 0 and A. The updates are applicable to:

- TMS320F2812 (179-ball MicroStar BGA™, GHH suffix)
- TMS320F2812 (176-pin low-profile quad flatpack [LQFP], PGF suffix)
- TMS320F2810 (128-pin LQFP, PBK suffix)

1.1 Quality and Reliability Conditions

**TMX Definition**

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device was tested over a particular temperature range and voltage range should not, in any way, be construed as a warranty of performance.

**TMP Definition**

TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

**TMS Definition**

Fully-qualified production device.

MicroStar BGA is a trademark of Texas Instruments. Other trademarks are the property of their respective owners.
1.2 Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package. The locations of the lot trace codes for the GHH and PGF packages are shown in Figure 1. The location of the lot trace code for the PBK package is shown in Figure 2. Table 1 shows how to determine the silicon revision from the lot trace code.

Table 1. Determining Silicon Revision From Lot Trace Code

<table>
<thead>
<tr>
<th>Second Letter in Prefix of Lot Trace Code</th>
<th>Silicon Revision</th>
<th>Revision ID (0x0883)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blank (no second letter in prefix)</td>
<td>Indicates Revision 0</td>
<td>0x0000</td>
<td>This silicon revision is available as TMX only.</td>
</tr>
<tr>
<td>A</td>
<td>Indicates Revision A</td>
<td>0x0001</td>
<td>This silicon revision is available as TMX only.</td>
</tr>
</tbody>
</table>
2 Known Design Marginality/Exceptions to Functional Specifications

### Advisory

**XINTF – XREADY Signal is not Sampled Properly When Using Asynchronous Sampling Mode**

**Revision(s) Affected:** 0 and A

**Details:**
In case of Asynchronous Ready mode, if the XREADY signal is high within the Lead period, then access will complete in the number of cycles programmed in LEAD + ACTIVE + TRAIL counters even if XREADY goes low before the start of the ACTIVE period. In this case, XREADY is not being used properly to extend the access.

**Workaround:**
Try one of the following possible workarounds:

- Ensure that the XREADY signal is not low at the start of an access when using Asynchronous sampling mode. If the XINTF sees the XREADY signal low from the start of an access, then the ACTIVE period will be extended as desired.
- Use the XTIMING register wait-state values to extend the access such that timings are met without using XREADY.
- Use the Synchronous XREADY sampling mode. This problem is not observed in Synchronous mode.

This issue will be fixed in the next revision of the silicon.

### Advisory

**ADC – Device Has Higher Gain Error Than the Design Goal of 1% FSR on All of the B0–B7 Channels**

**Revision(s) Affected:** 0 and A

**Details:**
The device has a higher Gain error than the design goal of 1% FSR on all of the B0–B7 channels. The gain error varies across channels A0–A7 and B0–B7.

Based on the current data obtained on B group channels, all B group channels show a uniform gain error as high as 2 to 3%.

**Workaround:**
The channel-to-channel Gain error data across channels are listed in Table 2. This should help in calibrating in software or hardware until the next revision of the silicon.

**CAUTION:**

The data provided are typical values only. These values are obtained from bench characterization at room temperature on a few devices.

TMX samples are not fully screened for all ADC parameters. If there are devices that have worse performance than suggested issues/values, it is recommended that the part be replaced.
ADC – Device Has Higher Offset Error Than the Design Goal (0.5 to 1%) on Some Channels

Revision(s) Affected: 0 and A

Details: Based on the current data obtained on all channels, some channels show an offset error as high as 1%.

Workaround: The channel-to-channel Offset error data across channels are listed in Table 2. This should help in calibrating in software or hardware until the next revision of the silicon.

Table 2. Channel-to-Channel Offset Error Data Across Channels (176-Pin PGF)

<table>
<thead>
<tr>
<th>ADC Channels</th>
<th>A0</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
<th>A6</th>
<th>A7</th>
<th>B0</th>
<th>B1</th>
<th>B2</th>
<th>B3</th>
<th>B4</th>
<th>B5</th>
<th>B6</th>
<th>B7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain Error in %</td>
<td>0.20</td>
<td>0.18</td>
<td>0.52</td>
<td>0.53</td>
<td>0.53</td>
<td>0.55</td>
<td>0.54</td>
<td>0.54</td>
<td>2.92</td>
<td>2.92</td>
<td>2.92</td>
<td>2.93</td>
<td>2.93</td>
<td>2.93</td>
<td>2.97</td>
<td></td>
</tr>
</tbody>
</table>

CAUTION:

The data provided are typical values only. These values are obtained from bench characterization at room temperature on a few devices.

TMX samples are not fully screened for all ADC parameters. If there are devices that have worse performance than suggested issues/values, it is recommended that the part be replaced.
**Advisory**

**ADC – Device Has Higher Non-Linearity Than the Design Goal of 2 LSBs**

**Revision(s) Affected:** 0 and A

**Details:**

Based on the current data obtained on all channels, some channels show non-linearity as high as 12 LSBs in the mid-scale range. That is, the mid-range conversions will be off by about 12 LSB counts.

**Workaround:**

This issue will be corrected in the next revision of the silicon. Until then, the following option could be used to correct for INL errors only for the TMX Revision A silicon.

INL issue is across all channels. Use the ADC results only for 9-bit data accuracy on this revision of the silicon and ignore the rest of the bits. This will mitigate the INL effect in the application provided the algorithm can tolerate 9-bit accuracy.

**CAUTION:**

The data provided are typical values only. These values are obtained from bench characterization at room temperature on a few devices.

TMX samples are not fully screened for all ADC parameters. If there are devices that have worse performance than suggested issues/values, it is recommended that the part be replaced.

**Advisory**

**A Low Output on GPIOF14 Can Disable the PLL and Watchdog if the Watchdog Fires a Reset**

**Revision(s) Affected:** 0 and A

**Details:**

If, during program execution, the XF_XPLLDIS/GPIOF14 signal is changed to either of the following:

- a general-purpose output and driven low
- the XF functionality and driven low

and a watchdog reset occurs, then the low output state of the XF_XPLLDIS/GPIOF14 pin will be latched into the XPLLDIS signal. The result of this is that the PLL and the reset function of the watchdog will be disabled. The watchdog itself is not disabled.

**Workaround:**

One of the following workarounds can be used:

- Do not toggle XF/GPIOF14 in user code. Instead, use another GPIO signal for status.
- Set the Watchdog to fire an interrupt instead of reset.

This will be fixed in the next revision of the silicon.
Advisory

**OTP Memory**

**Revision(s) Affected:** 0 and A  
**Details:** The 1K-word OTP memory is not available.  
**Workaround:** This will be fixed in the next revision of the silicon.

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Advisory

**Set Device Emulation Register Bits for On-Chip RAM Performance**

**Revision(s) Affected:** 0 and A  
**Details:** To get the best performance of on-chip RAM blocks M0/M1/L0/L1/H0, the internal control register bits have to be enabled. The bits are in the Device Emulation Registers.  
**Workaround:** All device initialization code should include the following register updates. These are EALLOW-protected registers.

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x950</td>
<td>0x0300</td>
</tr>
<tr>
<td>0x951</td>
<td>0x0300</td>
</tr>
<tr>
<td>0x952</td>
<td>0x0300</td>
</tr>
<tr>
<td>0x953</td>
<td>0x0300</td>
</tr>
<tr>
<td>0x954</td>
<td>0x0300</td>
</tr>
</tbody>
</table>

**Code Example:**

```
EALLOW
MOVL XAR1,#0x0950
MOVL XAR2,#0x0300
MOV *XAR1++,AR2
MOV *XAR1++,AR2
MOV *XAR1++,AR2
MOV *XAR1++,AR2
EDIS
```

The Code Composer GEL init files will initialize these for emulation and debug environment. From the next silicon revision onward, this initialization is automatically done upon reset.
**Advisory**

**Logic-High Level for XCLKIN Pin**

**Revision(s) Affected:** 0 and A

**Details:** This advisory is applicable only when an external oscillator is used to clock the device. The X1/XCLKIN pin is referenced to the device 1.8-V power supply (V_DD), rather than the 3.3-V I/O supply (V_DDIO). Therefore, the logic-high level for the input clock should not exceed 1.8 V. This requirement remains the same for future silicon revisions as well.

**Workaround:** A clamping diode may be used to clamp a buffered clock signal to ensure that the logic-high level does not exceed 1.8 V.

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**Advisory**

**PLL – PLL x4 and x8 Multiplier Ratios**

**Revision(s) Affected:** 0 and A

**Details:** When the PLL multiplier is set to x4 or x8 (by writing 0004 or 0008, respectively, in the PLLCR register), the watchdog is re-enabled and resets the device upon a WD overflow. With noisy board conditions, this problem may be observed with other PLL multipliers as well.

**Workaround:** Do not use these multiplier values for these revisions. This will be fixed in the next revision of the silicon.

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**Advisory**

**Low-Power Modes – STANDBY Mode**

**Revision(s) Affected:** 0 and A

**Details:** When the device is put into STANDBY mode, the watchdog is re-enabled and resets the device upon a WD overflow.

**Workaround:** Do not use the STANDBY mode for these revisions. This will be fixed in the next revision of the silicon.
3 Silicon Updates

In addition to the bug fixes, the following changes will be implemented in the next revision of the silicon.

3.1 PLL Lock Time

The PLL lock time is being changed from 4096 XCLKIN cycles (as implemented in revisions 0 and A) to 131072 XCLKIN cycles in the next revision of the silicon.

3.2 Drive Strength of Pins

The drive strength of the following pins is being changed from 8 mA to 4 mA in the next revision of the silicon: GPIOA0–GPIOA15 and GPIOD0.

3.3 PARTID Register

The 16-bit PARTID register (location 0x882) will not be supported in future revisions of the silicon.

3.4 Effect of XPLLDIS Pin on Watchdog Reset

Starting with the next revision of the silicon, watchdog reset will no longer be disabled when the XPLLDIS pin is sensed low at a reset.
4 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: http://www.ti.com

To access documentation on the web site:

1. Go to http://www.ti.com
2. Click on DSP Product Tree
3. Click on the C2000 tab
4. Click on TMS320C28x DSP Generation
5. Click on a device name and then click on the documentation type you prefer.

For further information regarding the TMS320F2810 and TMS320F2812, please refer to the following publication:

• TMS320F2810, TMS320F2812 Digital Signal Processors data manual (literature number SPRS174)
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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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