1 Introduction

The MSP430 was designed with a power-conserving, yet flexible microcontroller (MCU) architecture that is ideal for a broad range of ultra low-power measurement applications. Power-conserving applications such as energy meters, portable instrumentation and personal consumer products are often required to operate for extended periods of time without replacing the battery. The three key attributes of the MSP430 are:

- Lowest power consumption
- Mixed-signal system on-chip (SoC) solution
- Usable with modern programming techniques

Since the introduction of the MSP430, over 30,000 developers have adopted the architecture across a wide range of applications from thermostats and electricity meters to lifestyle-changing blood glucose monitors that are used by millions of diabetes patients around the world. With such a wide range of applications the need to provide greater variety of silicon features has become important. Engineers are increasingly being tasked with designing cost-effective systems with the conflicting requirements of higher performance, lower power and robust operation often under harsh operating conditions.

To address these design challenges, the new MSP430F2xx family was designed with enhancements that reduce system cost and improve reliability both in low-power and general purpose applications. At under one-micro-amp stand-by current with the ability to switch to fully synchronized 16 million instructions per second (MIPS) operating in less than one micro second, the new MSP430F2xx family provides twice the processing performance at half the power consumption compared to earlier MSP430F1xx devices.
2 Device Enhancements

2.1 Zero Power Brownout Reset

All members of the new MSP430F2xx include a zero-power brownout reset (BOR) function. The BOR function detects when the supply voltage is below a minimum level safe for code execution and forces the device into reset when such a condition exists. This BOR function prevents erratic device behavior. Brownout can be particularly problematic and difficult to isolate. For example, brownout can be introduced with the simple act of replacing a battery. Battery replacement can cause random and difficult to detect transients to the supply voltage. The zero-power BOR function on the MSP430F2xx was introduced on the MSP430F4xx family and is also available on a few MSP430F1xx derivatives.

- The inclusion of BOR assures more robust operation in harsh environments where supply voltage is unstable.
- The MSP430 BOR function is zero power and always on. This compares to competitive implementations that require more than 10µA making them not well suited for low power applications.

2.2 Clock Agility

To support the lowest power consumption and performance on-demand, the new enhanced basic clock system (BCS+) on the MSP430F2xx (like all other MSP430 clock systems) typically provides two clocks. A low frequency auxiliary clock (ACLK) is sourced directly from a common 32 kHz watch crystal with no external components and is used for always-on low power peripherals. A high speed clock is generated on-chip from an instant-on digitally controlled oscillator (DCO). The DCO is used by the CPU and other peripherals only when needed. To save power an application’s interrupt events steer the usage of the DCO only when required. The majority of the application life is spent in standby with high-performance available on-demand and only when required. The BCS+ is compatible with the earlier MSP430F1xx clock system adding new features that further reduce power consumption, improve robustness and lower system cost.

- Reduced standby power consumption - Standby mode (also known as real-time clock mode) current has been reduced to less than 1 micro amp at 3V compared to approximately 1.6 micro amps in the MSP430F1xx family. This mode is known as low power mode three (LPM3) and has only a watch crystal ACLK, a timer, memory and interrupts active. The reduced LPM3 current has decided benefits in metering, instrumentation and personal medical applications that by nature spend the bulk of the application life in a standby mode maintaining time and waiting to service events. For example, an application such as a thermostat or heat allocator measures temperature once every few seconds. LPM3 is the mode of operation greater than 99% of the time. Reducing LPM3 current has the largest impact on overall power consumption and increasing battery life.

- Programmable on-chip crystal load capacitors - This addition allows the use of a wider range of crystals and elimination of external components used typically to stabilize oscillation. On the MSP430F1xx family only fixed 12pf capacitors were available.
• Failsafe crystal oscillator - A crystal failure can trigger a non-maskable interrupt and start the on-chip oscillator for failsafe operation. This feature is always available with no additional power consumption in both high-frequency and low frequency modes. The failsafe crystal oscillator allows more robust operation in harsh environments and was previously available only in high-frequency mode on the MSP430F1xx family.

• Crystal input de-glitch filters - This feature reduces the possibility of externally introduced high frequency system noise and improves reliability.

• Crystal range select in high-frequency mode - This provides better stability and support the use of higher ESR, lower cost crystals.

• Improved on-chip digitally controlled oscillator (DCO) - The new DCO on in the BCS+ offers a sub 1 micro second start with ±2.5% accuracies and 16MHz operation over temperature and voltage. The DCO accuracy improvements allow the elimination of an external crystal and in most cases reduces cost. It is important to note that the DCO starts immediately to the programmed frequency with no time required for stabilization. This is important in applications that require instant access to a known and stable clock such as UART communication. Without stability, a fast starting clock is not useful.

2.3 Improved Embedded Flash

With Flash costs approaching that of read only memory (ROM) and the inherent flexibility provided by in-system programmable (ISP), Flash has become the choice for most new MCU designs. The majority of MSP430 designs now use flash for both prototypes and full production. Code changes can be implemented and tested instantly during development to the day a product ships from the factory. Field and customer upgrades are readily supported. Combining ISP Flash with embedded emulation also allows a system to be developed with the final chip soldered in the exact system that will be used for production and subjected to the exact and final operating conditions.

All MSP430 Flash supports the full operating speed, voltage range and ultra-low power capabilities of a given device. The MSP430F2xx introduces an improved Flash technology with the following enhancements:

• Programming/erase reduced from 2.7V to 2.2V - This 0.5V reduction has a significant impact on an application that is powered by two common alkaline batteries with a useful operating range from 3.3V-1.8V. Considering that the alkaline discharge is almost perfectly linear, an ISP reduction from 2.7V to 2.2V represents almost a 50% increase in the application time ISP and can be useful.

• The programming time has been reduced to as little as 17us per byte and the mass erase time reduced to 20ms. Faster programming/erase combined with smaller 64 byte information segments and interruptible ISP allows embedded Flash to replace external EEPROM in most cases. This capability saves cost and board real estate.
2.4 Greater Code Security

The bootstrap loader (BSL) allows access to an MSP430 using a common UART protocol. The primary intent of the BSL is to program the Flash memory. BSL access is protected with a 256-bit password which is the contents of the sixteen 16 bit interrupt vectors. On a blank device the vectors are known to be 0xFFFF, but in this state the device does not have useful code information. After the device has been programmed, only the programmer knows the contents of the interrupt vectors and thus the 256-bit BSL password. Code security has been improved on the MSP430F2xx with a more hack-proof BSL adding the following features.

- To reduce the possibility of code piracy, the MSP430F2xx BSL executes a mass erase after receiving a single incorrect 256 bit password. This compares to a simple access denial with earlier BSL versions.

- To reduce the possibility that errant software could inadvertently evoke the BSL, only with a proper startup sequence the BSL will enable the erase and programming of the Flash by clearing the LOCK bit in a control register. This makes an accidental programming of the flash via the BSL almost impossible because the flash can be programmed or erased only if the BSL was started properly and received a legal command afterwards.

2.5 Enhanced Watchdog Timer

The existing MSP430 watchdog timer (WDT) provides the basic feature of issuing a system reset in the event a time interval expires without software service. The enhanced watchdog timer (WDT+) on the MSP430F2xx family was first introduced on the MSP430FE42x electricity meter device to catch a wider range of software problems. The following are the new features added to the WDT+ to improve system reliability:

- A failsafe clocking feature was added that prevents the clock to the WDT+ from being disabled while in watchdog mode. For example if a failing crystal is selected as the clock source for the WDT+, the failsafe features will automatically select the internal oscillator to be sourced to the WDT+ providing failsafe operation.

- Software can not disable a clock if this clock is used by an active WDT+. The benefit of this can be seen within an interrupt service routine (ISR) in which the contents of the status register (SR) are saved to the stack. In the unlikely event that software inadvertently modifies the contents of the saved SR on the stack such that all clocks are disabled. In this situation on return from interrupt the clocked watchdog function, would be permanently disabled. The WDT+ prevents this condition.

- Code execution from the peripheral module address space is prohibited. As a Von Neuman architecture implementation, the MSP430 shares one memory map for code and peripherals. Despite a common memory map, there is no useful reason that a program fetch should ever occur from the peripheral address range (0x0000 to 0x01FF). If this condition should inadvertently occur, the WDT+ module will reset the system.
2.6 Additional Features

The MSP430F2xx includes many additional features. The pins of port 1 and port 2 now have user selectable internal pull up/down resistors. Using the internal pull up/down resistors can eliminate the need for external resistors saving space and reducing cost. This space savings is particularly important in portable applications. Considering the 4mm x 4mm footprint of the 24-pin QFN package available, the MSP430F21x1 device is equivalent in size to just two 1206 style resistors. In many applications the space consumed by external components can quickly surpass that of the MCU itself.

In 20/28-pin MSP430F2xx devices the crystal oscillator’s XIN/XOUT pins are now shared with port 2 pins P2.6 and P2.7, which were previously unavailable. This means in applications that do not require an external crystal, two additional port pins are available.

The comparator module in the MSP430F2xx family has an extended input multiplexer. This allows additional external analog signals to be measured.

3 MSP430 CPU Architecture

In addition to the new features, the MSP430F2xx maintains compatibility with previous MSP430s and utilizes the same powerful MSP430 16-bit RISC-like CPU core. The MSP430 CPU was designed from a clean sheet of paper and architected specifically to address modern programming requirements. The MSP430 CPU is intended to be transparent – that is, the highest code density would be realized without valuable time spent handcrafting software functions. Effectiveness in native C is a key requirement as more and more firmware engineers prefer to develop code only in C to promote portability.

Why is code effectiveness so important? Consider that a modern core like the MSP430 is quite compact and implemented in approximately 4K logic gates – roughly equivalent to 4KB of embedded Flash. So as onchip memory grows to 32KB and beyond to support increasingly complex system functionality, the chip size and cost can become dominated just by memory. With this in mind the architecture with the highest code density (uses the least amount of memory for a given function) has the most significant impact reducing the overall chip cost. Since the MSP430 is focused on power conservation, a code-effective architecture also reduces power by reducing instruction fetches and cycle counts. The MSP430 achieves the highest code density with a twofold approach, intelligent peripherals and a modern RISC-like core.

- Intelligent peripherals - All MSP430 peripherals are designed to require the least amount of software service. For example the analog-to-digital converters all have automatic input channel scanning, hardware start-of-conversion triggers and often DMA data transfer mechanisms. These hardware features allow the CPU resources to focus more on differentiated application-specific features and less on basic data handling. This means that lower cost systems can be implemented using less software and little power.

- A modern RISC-like core that delivers the highest high-level code efficiency, by design. This is covered below in detail.
To achieve the highest C code efficiency, first consider what a compiler likes. Compilers prefer instruction set orthogonality and many registers that operate identically to be free to allocate resources without restrictions. Compilers also use the stack for passing parameters and for storing temporary variables. With these facts and guidelines, the MSP430 architecture was developed as follows:

- Complete orthogonal instruction set – Although the MSP430 architecture implements only 27 instructions, every instruction is usable with every addressing mode throughout the entire memory map. This enables a very compact instruction set to implement a very large feature set with a strongly simplified, lower cost and lower power CPU.

- High register count - In addition to the program counter and stack pointer, twelve identical general purpose 16-bit CPU registers are available. Any register can be used identically for data or as a pointer with single-cycle register to register instruction execution. The single working file or accumulator bottleneck often experienced when using other MCUs, does not exist in the MSP430.

- Page free - The 16-bit architecture of the MSP430 allows the direct addressing of the entire 64kB memory address space. Direct access to integrated peripherals such as 16-bit data converters is an easy and straight forward task. These features simplify the development of software.

- Stack processing - The stack pointer has the full addressing capabilities of a general purpose register which allows any needed manipulation of data on the RAM-based stack. The compiler is free to pass and manipulate parameters on the stack to the extent of available RAM without restriction.

- Usability of jumps - Inspection of normal code shows that up to 10% of the code is conditional jumping. To support the requirements eight single word conditional jumps with a large \(+512\) reach are implemented.

- In embedded applications, approximately 20% of the code simply reads, modifies and writes back an operand. In a typical RISC architecture, such an operation yields poor code density because the operand must always pass through a CPU register with the used register saved and restored. Therefore, three addressing modes (symbolic, absolute and immediate) allow fully atomic memory-to-memory operations with the complete instruction set. These addressing modes drive significant code savings and superior performance.

- Byte and word processing - Any instruction can be used with 16-bit word or 8-bit byte data type. This feature is especially useful for table processing allowing the use of the most code efficient data type.

- Constant generator - One of the reasons for the high code efficiency of the MSP430 is the constant generator. The constant generator automatically generates the six most used immediate constants in hardware. A dedicated CPU register is used automatically for constant generation. As the constants are generated from the CPU no operand is fetched from memory, saving code and increasing speed. The constant generator function is automatic and completely transparent to the user.
4 Development

Development support for the MSP430F2xx family is fully-compatible with the existing MSP430F1xx family. Dedicated emulation logic is embedded on the device itself and accessed using standard IEEE 1149 JTAG signaling. The MSP430s embedded emulation capabilities provide full speed, single step, hardware breakpoint and clock control with dedicated logic – no application resources are used. The fact that development is conducted in-system with the exact device and under the final product conditions eliminates the dreaded “it worked on the emulator” scenario.

Embedded emulation is especially important in small form factor and analog-intensive applications where the effects of an external emulator and associated cabling prevent realistic emulation. In addition to development, the JTAG signaling is also reused for in system production programming, and if required, field-programmable upgrades.

5 Summary

The MSP430F2xx provides twice the processing performance at half the stand-by consumption compared to earlier MSP430F1xx devices. In addition, the MSP430F2xx family incorporates enhancements that reduce overall system cost and improve reliability making these new devices an ideal solution for existing low power MSP430 designs or as a launch point for a variety of new applications.
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