Faraday MPEG4 Codec Platform SoC
FIC8120

Key Features

Architecture
- AMBA-AHB bus based for high speed devices
- AMBA-APB bus based for low power devices

Embedded Processor
- Faraday FA526
- ARM based 32-bit RISC
- MMU
- Up to 190 MHz
- I-8K, D-8K

External Bus Interface
- SDRAM (400M bytes/sec)
- Asynchronous SRAM / ROM / Flash
- Clock / PLL
  - 32.768 KHz and 22.1184 MHz oscillators
  - Programmable Frequency Core PLL for main clock
  - Programmable Frequency Core PLL for audio main clock

Power Management
- Frequency change control
- Clock gating control
- Normal operation

AHB Bus Components
- SDRAM Controller
- Static Memory Controller
- Display Controller
- DMA Controller
- USB2.0 OTG Controller
- Capture
- MPEG-4/JPEG CODEC
- Ethernet MAC controller
- PCI bridge
- IDE controller

APB Bus Components
- Timer
- Watch Dog Timer
- Real Time Clock
- Interrupt Controller
- GPIO
- PC
- PS/AC97
- UART x 4
- Multimedia Card / Secure Digital Host Controller

MPEG-4/JPEG CODEC
- Support MPEG-4 Simple Profile encoding up to D1 @ 30 fps with codec clock speed under 70 MHz
- Power consumption: Less than 1.2 mW/MHz on 0.18 µm process

Embedded Analog Device
- USB2.0 OTG PHY
- PLL x 2
- DLL x 1

Operating Frequency
- AMBA AHB bus: up to 90 MHz
- AMBA APB bus: up to 45 MHz

Operating Voltage
- 1.8V for Core
- 3.3V for Input / Output with 5V tolerance

Process
- 0.18 µm

Package
- 353-pin PBGA

General Description

FIC8120 video chip provides an easy development system to accelerate image and video related applications such as MPEG-4 and JPEG to end products. It provides a cost-effective and high performance solution for video application integration and verification in early development stage. The FIC8120 system platform includes a wide range of basic peripherals, including FA526 CPU Core, MPEG-4/JPEG CODEC engine, USB2.0 OTG Controller, USB2.0 PHY, Display Controller, DMA Controller, Capture, PCI Bridge, IDE Controller, Ethernet MAC Controller, a Three-Metal Programmable Cell Array (3MPCA) body, and AMBA Bus Framework. The 3MPCA body allows users to integrate their designs to expand the specific application.

Applications

- (Wireless LAN) Internet Surveillance Camera
- Digital Video Recorder
- (Wireless LAN) Digital Media Adaptor
- Portable Media Player
- (IP) Set-Top Box
- Media Gateway
- (Wireless LAN) Network Attached Storage
- TV Captured Card

Functional Blocks
Block Descriptions

FA526
FA526 is a general-purpose 32-bit embedded RISC processor. It includes a CPU core, separated instruction / data caches (8K bytes each, 2-way set-associated), a write buffer (8 words for data / address each), a memory management unit, and an ICE interface.

The CPU core is a Harvard architecture design with a six-stage pipeline consisting of Fetch, Decode, Shift, Execute, Memory and Write stages. In order to reduce the branch penalties, FA526 contains a Branch Target Buffer (BTB) to improve the overall performance. FA526 MMU implements an enhanced ARM architecture, V4 MMU, to provide translation and access permission checks for the instruction and data address ports of the FA526 core. FA526 can operate at speeds up to 190 MHz with low operating power.

Peripheral Components
The peripheral components consist of three (3) parts: System Bus Peripherals, Core APBs, and DMA APBs.

System Bus Peripherals

- **AHB Controller (AHBC)**
  The main purpose of an AHB Controller is to support a mechanism to control the user rights for the Advanced High-performance Bus (AHB). This mechanism supports an arbiter and a decoder that are highly configurable and provides a flexibly programmable model to ease SoC integration efforts. The mechanism contains the following three (3) components: Arbiter, Decoder and Multiplexer. The AHBC features include:
    - AMBA 2.0 compliant
    - Multi-level arbitration
    - Round-robin arbitration

- **SDRAM Controller (SDRAMC)**
  The SDRAM memory controller supports four 8-, 16- and 32-bit-wide banks. The SDRAM controller performs auto-refreshing (CBR) during normal operation, and supports SDRAM self-refreshing during Sleep mode. SDRAMC shares the address/data bus with Static Memory Controller (SMC). The SDRAMC features include:
    - Zero-wait-state write
    - Support rich types of SDRAM
    - Support a programmable refresh controller
    - Support a programmable refresh scheme (staggered / non-staggered)
    - Support five (5) AHB channels
    - Support 16-word data FIFO
    - Support four (4) chip selects

- **Static Memory Controller (SMC)**
  The SMC supports Flash memory, SRAM, or ROM. Each chip select can be individually configured to an 8-, 16- or 32-bit-wide data bus. SMC shares the address / data bus with SDRAMC. The SMC features include:
    - Support four (4) chip selects
    - Support a 512 K x 8 bit EPROM
    - Support two (2) 16 M x 16 bit Intel asynchronous flashes
○ Support programmable / jumper settings for external memory bus width (8-, 16-, 32-bit)
○ Shadow first bank with other banks

- **Direct Memory Access Controller (DMAC)**

  The DMAC is provided to enhance system performance. System efficiency is improved with high-speed data transfer among the system and devices and by reducing processor-interrupt generation. The DMAC provides up to 7 channels for memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers with the shared buffers. The DMAC features include:
  ○ Up to seven (7) DMA channels
  ○ Provide memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers
  ○ Group Round Robin arbitration scheme with four (4) priority levels
  ○ Support chain transfer
  ○ Support 8/16/32-bit data width transfer

- **USB 2.0 OTG Controller**

  The universal serial bus (USB) 2.0 On-The-Go (OTG) controller can play a dual-role as a host and peripheral controller. As a host, it contains a USB host controller that supports all speed transactions. Without software intervention, the host controller can deal with a transaction-based data structure to offload CPU and automatically transmit and receive data on the USB bus. As a peripheral, each endpoint, except endpoint 0, accepts programmable HS / FS transfer types to provide a flexibility that is suitable for all kinds of applications. In addition, complying with OTG standards means both Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) are supported. The transceiver interface is UTMI+ level 2, which supports HS / FS / LS transfers without a hub. The USB 2.0 OTG controller features include:
  ○ Compliant with USB specification revision 2.0
  ○ Compliant with On-The-Go Supplement to USB 2.0 specification revision 1.0
  ○ Support UTMI+ level 2 compliant transceiver
  ○ Compatible with EHCI 1.0
  ○ Support OTG SRP and HNP
  ○ Support point-to-point communications with one HS / FS / LS device
  ○ Endpoints hardware configurable as HS / FS devices
  ○ Both host and device support isochronous / interrupt / control / bulk transfers
  ○ Compatible with EHCI data structures
  ○ Embedded DMA access to FIFO
  ○ SRAM interface for FIFO
  ○ Support suspend mode, remote wake-up and resume
  ○ Completely synchronous design
  ○ USB OTG software subsystem

- **MPEG-4/JPEG Engine (FTMCP100)**

  The MPEG-4/JPEG engine is an AHB based CODEC. This CODEC includes some hardware engines to accelerate computation intensive tasks such as Motion Estimation, DCT / IDCT, Quantization / Inverse Quantization and Motion Compensation. The FTMCP100 is controlled by CPU through AHB slave interface. By initializing the control registers of the CODEC, the motion estimation calculation task for an entire 16x16 or 8x8 block can be done automatically by the FTMCP100. The DCT / Quantization, IDCT / Inverse Quantization, AC/DC prediction, Zigzag scan and VLC / VLD calculation task can also be done automatically for a macro-block by the FTMCP100. Thus CPU can be released from timing critical tasks in video encoding. The standard-cell based approach of the FTMCP100 allows users to quickly integrate the FTMCP100 into their SoC designs. The MPEG-4/JPEG Engine features include:
○ Compliant with MPEG-4 (ISO/IEC 14496-2) simple profile L0 ~ L3 standard, with resolutions including subQCIF, QCIF, CIF, VGA and 4CIF @ 30 fps, with a step of 16
○ Compliant with JPEG (ISO/IEC 10918-1) base-line standard
○ Include hardware engines for Motion Estimation / Motion Compensation, DCT / IDCT, Quantization / Inverse Quantization, AC / DC prediction and Variable Length Coding / Decoding
○ A local memory controller to control local memory shared by CPU, FTMCP100 and DMA master
○ A DMA controller to control data transfers between system memory and local memory
○ Automatic power down mechanism to reduce power consumption
○ Motion Estimation search range: -16 ~ +15.5 (optionally -32 ~ +31) with half-pel accuracy
○ Support 4MV and unrestricted MV
○ Rate control: constant bit rate control and variable bit rate control

○ Error resilient tools: encoder supports resynchronization marker and header extension code; decoder supports resynchronization marker, header extension code, data partition and RVLC
○ Support short video header (H.263 baseline)
○ Support H.263/MPEG/JPEG quantization methods
○ JPEG supported features:
  ○ support 4 user-defined Huffman tables (2AC and 2DC)
  ○ support 4 programmable quantization tables
  ○ support interleave and non-interleave scans
  ○ support YUV 4:4:4, 4:2:2 and 4:2:0 formats
  ○ support image size up to 64k × 64k
○ Support full-duplex operation (e.g. video phone and video conference) by s/w switching encoding and decoding task on the same h/w

• Capture

The video capture interface performs the task of transferring video data streams from video decoder to the system memory. The video capture interface comprises an AMBA AHB compatible master interface for transferring video data to the system memory, a size configurable asynchronous FIFO for buffering and switching the data from the capture clock domain to the host bus clock domain, an AMBA AHB compatible slave interface for accessing the control registers of the video capture interface, and a controller for controlling the data transfer operation. The Capture features include:
○ Support ITU 656 YUV 4:2:2 NTSC / PAL video input format
○ Support ITU 656 YUV 4:2:2 CMOS VGA input format
○ Support D1, CIF and QCIF size YUV 4:2:2 and YUV 4:2:0 separated video output format
○ Equipped with AHB host interface (master / slave)
○ Support skip page control
○ Support H/V sync. error detection
○ Support separated YUV buffering
○ 128/256/512/1024/2048 bytes

• IDE Controller

The Faraday ATA controller incorporates an IDE hardware interface in compliance with the ATA-7 Rev. 1 (T13 1532D Vol. 1 & 2 Working Draft dated August 25, 2002) specification. On the internal side the Faraday ATA controller provides an AHB slave interface which is in conformance with AMBA V2.0. To maximize the data throughput and minimize the bus bandwidth, the Faraday ATA controller incorporates three FIFOs – a command FIFO holding the ATA commands, a read FIFO and a write FIFO for data transfer to/from the external device. The Faraday ATA also provides DMA support with several request triggers to support multitasking and real-time systems. The IDE controller features include:
One IDE channel (master and slave)
- ATA 7 Rev 1 compliant
- Register transfer mode 0 – 4
- PIO mode 0 – 4 (max transfer rate: 16 MB)
- Ultra DMA mode 0 – 6 (max transfer rate: 133 MB)
- Little endian–big endian conversion
- DMA interface

- Display Controller
  The Display controller transforms the processed video data into CCIR-656 format which can be sent to external TV encoder for displaying on TV or LCD screen.

- Ethernet Controller (MAC)
  The MAC is a high quality 10 / 100 Ethernet controller with DMA function. It includes AHB wrapper, DMA engine, on-chip memory (TX FIFO and RX FIFO), MAC, and MII interface.

  MAC is an Ethernet controller that provides AHB master capability and full compliance with IEEE 802.3 100 Mb/s and 10 Mb/s specification with MII interface. MAC DMA controller handles all data transfers between system memory and on-chip memory. With the DMA engine, it can reduce CPU loading, maximize performance and minimize FIFO size. MAC has on-chip memory for buffering, so external local buffer memory is not needed. The MII interface can support two specific data rates, 10Mb/s and 100Mb/s. The functionality is identical at both data rates, as are the signal timing relationships. The only difference between 10Mb/s and 100 Mb/s operation is the nominal clock frequency. The MAC features include:
  - Support a DMA engine for transmitting and receiving packets
  - Support a programmable AHB burst size
  - Support transmit and receive interrupt mitigation
  - Contain 2 independent TX/RX FIFO (2K bytes each)
  - Support half and full duplex modes
  - Support flow control for full duplex and backpressure for half duplex
  - Support MII interface

- PCI Bridge Interface
  The PCI Bridge interface is a high performance, easy to use AHB to PCI Bridge. It provides a PCI master to issue a command to the AHB bus or an AHB master to issue a command to the PCI bus through the bridge. To improve performance, the bridge uses six asynchronous FIFOs to process AHB master read / write or PCI master read / write. PCI master write cycle and slave read cycle support pre-read logic that can guarantee PCI setup timing. The PCI Bus provides operating frequencies up to 66 MHz. The operating frequency of the AHB bus depends on system requirement. Features of the PCI Bridge interface are as follows.
  - Compliant with PCI 2.2 specification
  - PCI bus clock rate up to 66 MHz
  - PCI bus supports 32-bit data bus transaction
  - PCI bus master supports I/O read / write, memory read / write, configuration read / write command
  - PCI bus slave supports memory read / write command
  - PCI bus supports all disconnect types (Master-Abort, Target-Abort, Target-Retry, Disconnect with data, Disconnect without data)
  - PCI master supports Latency Timer
  - PCI slave supports Initiate Latency Timer and Wait-State Latency Timer
  - PCI slave supports delay transaction
  - Support bus transaction ordering
**AHB-to-APB Bridge**

An AMBA APB implementation typically contains a single APB bridge that is required to convert AHB transfer into a suitable format for the slave devices on the APB. The bridge provides latching of all address, data and control signals, as well as a second level of decoding to generate slave select signals for the APB peripherals. The APB bridge is the only bus master on the AMBA APB. In addition, the APB bridge is a slave on the higher-level system bus. Otherwise, the APB bridge provides a DMA function to enhance the performance of data transfer. The AHB-to-APB Bridge features include:

- Support 4 sets of independent DMA Channel for APB-to-AHB, AHB-to-APB, AHB-to-AHB or APB-to-APB transfer
- Support up to 14 sets of APB Device.

**Core APB**

The core APB contains the Faraday peripheral IP blocks that are needed for the basic functions of the OS.

- **Timer**
  
  Faraday’s Timer provides 3 independent sets of sub-timer. Each sub-timer can use system clock (OSC) for increment or decrement counting. Two match registers are provided for each sub-timer. Whenever any value of the match registers becomes equal to any one of the sub-timers, timer interrupt is triggered immediately. The issuance of timer interrupt can be decided by register setting when overflow occurs. The Timer features include:
  
  - Three (3) independent 32-bit timer programming models
  - Interrupts can be issued upon overflow and time-up
  - Each sub-timer has two match registers
  - Programmable decrementing/incrementing mode on the counter

- **Watch Dog Timer (WDT)**
  
  The WDT is used to prevent system from infinite looping if the software becomes trapped in deadlock. In normal operation, the user restarts the WDT at regular intervals before the counter counts down to zero. The WDT generates one or a combination of the following signals: reset, interrupt, or an external interrupt signal. The WDT features include:
  
  - 32-bit down counter
  - Upon timeout, WDT outputs one or a combination of: System Reset / System Interrupt / External Interrupt
  - Variable timeout period of reset
  - Access protection

- **Real Time Clock (RTC)**
  
  The RTC provides a basic alarm function or a long-time-based counter. The RTC is set to be 1 Hz output and is utilized as a system timekeeper. It also serves as an alarm that generates an interrupt signal or a wakeup event when the RTC output clock increments to a preset time. All the registers in the RTC are reset by power-on reset only.
  
  The RTC accepts two clock sources -- APB bus clock (PCLK) and 1 HZ clock (CLK1HZ). When the system is in sleep mode, the PCLK clock can be gated while the RTC keeps on counting. This mechanism promises the lowest power consumption when the system is in sleep mode. The RTC features include:
  
  - Separated second, minute, hour and day counters to reduce power consumption and software complexity
  - Programmable daily alarm with interrupt
  - Once-per-second, once-per-minute, once-per-hour, and once-per-day interrupts
  - 6-bit second counter, 6-bit minute counter, 5-bit hour counter, and 16-bit day counter
• Interrupt Controller (INTC)
  The Interrupt Controller provides both FIQ and IRQ modes to microprocessor. It also determines whether the interrupts cause an IRQ or an FIQ and masks the interrupts. The INTC features include:
  ○ Support up to thirty-two (32) fast interrupt (FIQ) inputs
  ○ Support up to thirty-two (32) standard interrupt (IRQ) inputs
  ○ Interrupts can be routed to either IRQ or FIQ
  ○ Provide both edge and level triggered interrupt sources with positive and negative directions
  ○ Support de-bounce circuits for interrupt input sources
  ○ Independently enable or disable any interrupt source

• GPIO
  GPIOs are used to input / output data from system and device. Each GPIO can be programmed as an input or an output, or as an interrupt input. The GPIO supports rising edge, falling edge, both-edge, and high level / low level interrupt sense types. The GPIO features include:
  ○ Each port can separately trigger the GPIO interrupt
  ○ Each port interrupt generation can be triggered by rising / falling edge, both edges or high / low level
  ○ Each port can be pulled high or pulled low
  ○ Each port provides de-bounce function
  ○ Output data bit can be set or cleared separately
  ○ All ports are set to input mode at hardware reset

• I²C
  The I²C is a two-wire bidirectional serial bus that provides a simple and efficient method of data exchange while minimizing the interconnection between devices. The I²C bus interface controller allows the host processor to serve as a master or slave residing on the I²C bus. Data are transmitted to and received from the I²C bus via a buffered interface. The I²C features include:
  ○ Support standard and fast modes through programming the clock division register
  ○ Support 7-bit, 10-bit and general call addressing modes
  ○ Glitch suppression throughout the de-bounce circuits
  ○ Programmable slave address
  ○ Support Master-transmit, Master-receive, Slave-transmit and Slave-receive modes
  ○ Slave mode general call address detection

• Power Management Unit (PMU)
  The PMU module generates the whole system clock / reset / operating mode control signals. The clocks that are derived from a 22.1184 MHz crystal and an optional 32.768 KHz crystal are used to drive the FIC8120 functional blocks. The 22.1184 MHz crystal drives a core Phase-Locked Loop (PLL) and a Peripheral PLL for generating all audio clocks. The PLLs produce desired clock frequencies to particular functional blocks. The 32.768 KHz crystal provides an optional clock source that must be selected after a hard reset. The supported modes include:
  ○ Normal mode: Normal full function mode
  ○ FCS mode: Frequency Change Sequence (FCS) mode allows users to change the core PLL settings, such that the system can operate at different frequencies
DMA APB

The following peripherals can be accessed by the DMA controller for efficient data transfer.

- **I²S/AC97 Controller**
  
  The I²S/AC97 Controller is a full-duplex synchronous serial interface that can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom Codecs, touch panel control chips, and other devices that use serial protocols for transferring data. The serial data formats may range from four (4) to thirty-two (32) bits in length. The I²S/AC97 features include:
  
  - Independent clock to ease bit clock generation
  - Master or slave mode
  - Internally or externally controlled serial bit clock
  - Internally or externally controlled frame / sync
  - Programmable frame / sync polarity
  - Programmable serial bit clock polarity, phase and frequency
  - Programmable serial bit data sequence (MSB or LSB first)
  - Programmable threshold interrupt of transmit / receive FIFO
  - Independently programmable interrupt enable / disable
  - Provide 16-word transmit FIFO and 16-word receive FIFO
  - Support DMA REQ/ACK for large data transfers
  - Programmable I²S format (including zero bits padding and right or left justification)

- **UART**

  UART Controller is a serial communications element that is backward compatible to the 16550 to support existing communications software. The UART controller features include:
  
  - High-speed NS 16C550A-compatible UART
  - Programmable baud rates up to 1152 Kbps
  - Ability to add or delete standard asynchronous communications bits (start, stop, and parity) in serial data
  - Programmable baud rate generator that allows the internal clock to be divided by 1 to \(2^{16} - 1\) to generate an internal16X clock
  - Fully programmable serial interface:
    - 5-, 6-, 7-, or 8-bit characters
    - Even, odd, and no parity detection
    - 1, 1.5, or 2 stop bit generation
  - Complete status reporting capability
  - Ability to generate and detect line breaks
  - Fully prioritized interrupt system controls
  - Separate DMA requests for data transmission and reception services
  - Break, parity, overrun, and framing error simulation for UART mode
• Secure Digital Card Controller (SDC)
  The SDC supports both SD and MMC interface protocols. It also supports hot insertion/removal detection. For SD, it provides write-protect and 1-bit or 4-bit bus width for large data transfer without CPU intervention. The SDC features include:
  ○ Support SD memory card protocol version 1.0
  ○ Support SD/MMC bus protocol
  ○ Support 4-bit width for SD data bus
  ○ Support 4-word Data FIFO depth
  ○ Built-in generation and checks for 7- and 16-bit CRC data
  ○ Variable clock rate: 0 ~ 25 MHz for memory card
  ○ Hot insertion / removal
  ○ Write-protect for SD card
  ○ Support single or multiple block access to the card for read, write, or erase operations
  ○ Support DMA REQ/ACK for large data transfers

• Three-Metal Programmable Cell Array (3MPCA)
  The MPCA block delivers cell-based, ASIC-like performance, density, and power consumption. It is an extremely flexible, fast, and low-NRE way of customizing application specific packet processing engines because users need only change 5 mask layers instead of a total of 26 to 28 layers as in a 0.18 µm standard logic process. The MPCA gate count is 100K. The MPCA interface could support 4 AHB masters, 5 AHB slaves, 6 APB slaves, 6 DMA control signals, 6 interrupt signals, one CCIR656 input and one CCIR656 output. The MPCA has pin-mux function with 16 GPIO pins.

Software Architecture of FIC8120
FIC8120

Developing Board

Basic Parts
- FIC8120 main board for video application
- FA5 ICE (USB Interface)
- RS-232 cable for debug console
- Power supply adapter
- MediaCreative CD (Drivers, BSP)

Extension Parts
- Sensor Module
- LCD Module

Software Design Kit
- Linux Kernel 2.4.19
- MPEG4 Driver
- 10/100 Ethernet driver
- USB2.0 OTG driver
- IDE controller driver
- ADPCM/MP3/WMA
- FFmpeg
- JPEG

Tool Chain
- arm-elf-gcc 2.95.3: GNU C compiler for embedded Linux
- glibc 2.2.3: GNU C library for embedded Linux
- binutil 2.11.2: GNU Binary image builder utility